RCA

Linear Integrated Circuits

Contents

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This Manual, like its preceding editions, has been prepared to provide an understanding of the basic principles involved in the design and application of linear integrated circuits. It may be used as a guide by circuit and system designers in determining optimum design specifications with regard to integrated-circuit capabilities and system requirements. It is also helpful to educators, technicians, and others who have a basic understanding of solid-state devices and circuits. The basic fabrication, packaging, mounting, and interconnection techniques are explained, and the fundamental building-block elements for linear monolithic integrated circuit are analyzed. Descriptive data and application information are then provided on RCA integrated circuits designed for a broad range of general- and special-purpose linear applications.

This edition has been extensively revised and expanded to cover the latest innovations in integrated-circuit technology and to provide broader, more detailed information on fabrication, design, and applications. Information has been added on many new types of linear integrated circuits. The Manual also features a new **Application Guide** that indicates circuit types recommended for specific applications and **Technical Data** and **Outlines** Sections that provide ratings, characteristics, and package details for RCA linear integrated circuits.

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The **hybrid integrated circuit** is also becoming increasingly popular, particularly for certain specialized types of custom applications. Hybrid (i.e., multichip) circuits are complete electronic circuits in which a multiplicity of separately manufactured components are arrayed on a suitable passive substrate (e.g., ceramic) and interconnected by metallization patterns and/or very fine wires. A hybrid may be defined succinctly as any combination of two or more of the following: discrete components, an active-substrate integrated circuit, and a passive-substrate integrated circuit. Currently, individual discrete transistors are used in most hybrid integrated circuits as the active electronic elements; passive components frequently take the form of discrete resistors or capacitors, although thick-film and thin-film passive components are also being used. A hybrid integrated circuit may also consist of one or more monolithic integrated-circuit chips housed in a single package with assorted ancillary components. Future hybrid designs will undoubtedly employ pluralities of monolithic integrated-circuit chips as the prime electronic constituents.

The monolithic integrated circuit usually offers economic advantages over hybrid devices. On the other hand, hybrid designs enjoy advantages in custom design flexibility and the freedom to intermix an assemblage of electronic components which are impractical, impossible, or uneconomic for production with the monolithic technology of today. The information contained in this Manual is limited to that which is pertinent to silicon monolithic integrated circuits.

PROCESSING AND ASSEMBLY OF MONOLITHIC CIRCUITS

Fig. 1 shows the schematic diagram of an FM subsystem that is

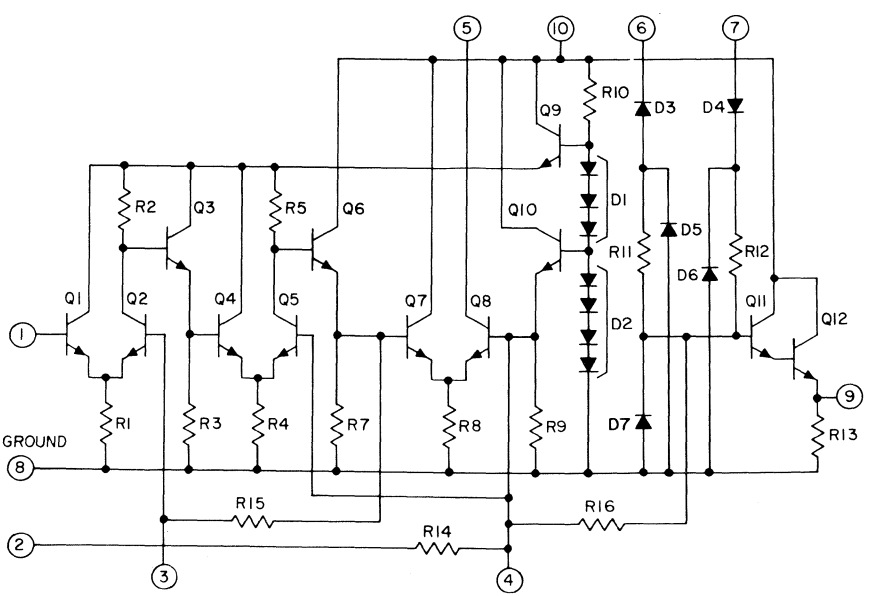


Fig. 1 — Schematic diagram of an integrated circuit for FM subsystem applications.

typical of the complex electronic circuitry that can be integrated on a single silicon chip. This circuit, which can be used as the major portion of the circuitry required for the sound function in a television receiver, employs 12 transistors, 12 diodes, and 15 resistors. Fig. 2 shows the integrated-circuit chip for this subsystem, complete with the metallic wiring used to interconnect the various components. The numbers shown on the chip diagram identify terminal connections (called pads)

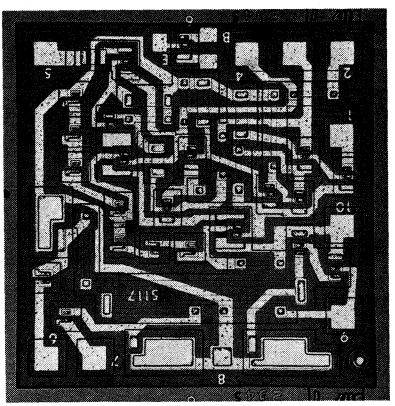


Fig. 2 — Integrated-circuit "chip" (0.060 inch by 0.064 inch) for FM subsystem circuit.

for 1.5-mil-diameter aluminum wires which are used to connect the integrated-circuit chip to its case terminals, as shown in Fig. 3. Although the circuit shown in Figs. 1 and 2 is not the most complex being produced today, it is typical of integrated circuits which are in mass production and being supplied in volume quantities at a reasonable cost per device. This circuit illustrates the cost savings that monolithic integrated circuits make possible for many types of electronic equipment.

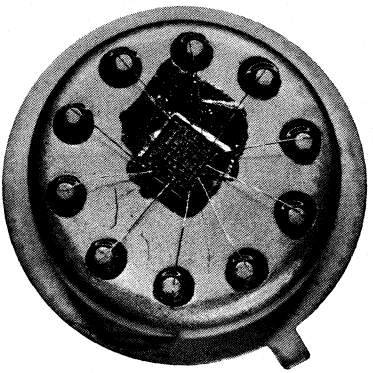


Fig. 3 — Integrated-circuit chip mounted in TO-5-style package assembly.

The manufacture of silicon monolithic integrated circuits involves a series of highly critical operations in which silicon is subjected to carefully controlled, high-temperature chemical processes. The lateral physical dimensions of the chemical reactions in the silicon are controlled by photolithographic techniques. High-precision photomasks represent the assembly tools, jigs, and fixtures employed in the manufacture of monolithic integrated-circuit wafers. The practices employed in packaging of integrated-circuit chips are, to a considerable degree, merely extensions of methods used in packaging of discrete transistors. Electrical testing of monolithic integrated circuits is highly automated and produces large quantities of data for use in computer-aided analyses of the effectiveness with which the chemical processes are being controlled.

Wafer Processing

Monolithic integrated circuits are not fabricated singly, but rather "by the wafer" as a minimum "batch."

Individual silicon wafers about 10 mils thick are cut from a silicon ingot into slices, as shown in Fig. 4. Each wafer (about 1.5 to 2 inches in diameter) is then polished to a mirror finish by acid etching. Circuit complexity determines the size of the chip for a particular design. Circuits being produced today use chip sizes ranging from about 15 mils to 100 mils square. For this range of chip sizes, the number of chips produced per wafer varies from the order of 1,000 down to about 250.

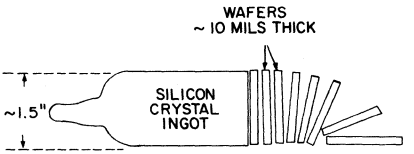


Fig. 4 — Integrated-circuit wafers being cut from silicon ingot.

Because the cost of processing a wafer is the same regardless of the number of chips it produces, it is evident that small chip area reduces the cost of the individual chips. In addition, failure modes tend to be random in nature; as a result, the probability of a defect is larger for a large chip area than for a small one. For example, a truly random failure mode that provides a 75-percent yield for a 40-mil-square chip would provide zero yield for an 80-mil-square chip. Thus, a smaller chip area increases processing yields and further reduces costs.

The first major step in processing the mirror-finished wafer involves the formation of a silicon dioxide layer (about 0.025 mil thick) on the surface of the wafer, as shown in Fig. 5. This thin layer of silicon dioxide protects the silicon surface of the finished integrated circuit, acts as a barrier to dopants during the semiconductor junction-forming processes, and provides an insulating substrate for the interconnection metals. Silicon dioxide is formed on the silicon wafer by heating it to a temperature of 1000 to 1300°C and passing oxygen over the surface. The silicon dioxide layer also serves as a "pattern mask" in determining the area through which "dopant" atoms may pass freely into the silicon substrate to form regions of either n-type or p-type silicon (depending on the type of dopant material used).

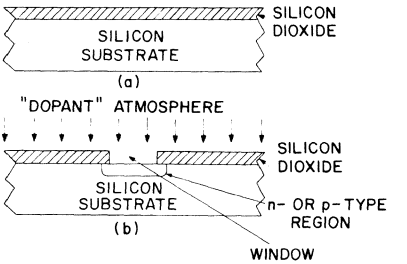


Fig. 5 — Silicon dioxide as a "mask".

The ability to control the procedures by which "windows" are formed selectively in the silicon dioxide layer is one of the most crucial in integrated-circuit manufacturing. In some instances, the windows may be in the order of only 0.1 mil square. The windows in the silicon dioxide define the geometrical areas in which chemical diffusion reactions are localized. These windows are mechanically positioned and dimensioned by the use of photomasks and photochemical procedures, a system of processing which is dependent on the photosensitive properties of a type of lacquer called photoresist.

Fig 6(a) illustrates the manner in which an oxide-coated silicon wafer is covered with a layer of photoresist lacquer several thousand angstroms thick. A photomask, in this case a glass plate having a pattern of black spots on it, is placed against the photoresist and the system is exposed to ultraviolet light.

Illuminated areas of the photoresist tend to harden (polymerize), while the areas under the black spots of the photomask remain soft and are removed during a subsequent "photo-development" operation. Fig. 6(b) shows the "exposed" patterns of the windows in the photoresist following the "photo-development" operation. The wafer is then subjected to

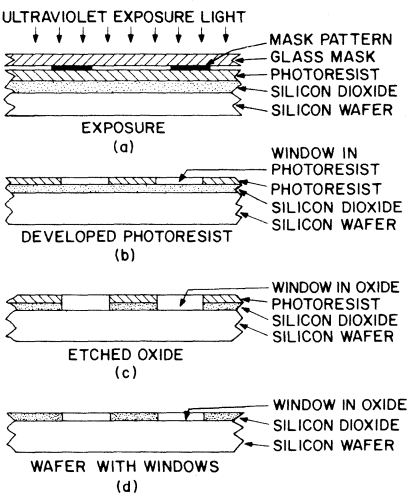


Fig. 6 — Photoresist processing of monolithic integrated-circuit wafer.

a chemical etchant (such as diluted hydrofluoric acid), which dissolves the silicon oxide in the photoresist windows without attacking the silicon underneath. The desired windows in the silicon oxide are thus produced, as shown in Fig. 6(c). The remaining photoresist is removed chemically; the resultant wafer is shown in Fig. 6(d). This "cleaned" wafer with windows in its oxide coating is then ready for chemical doping procedures in diffusion furnaces to produce regions with either n-type or p-type electrical characteristics in the areas beneath the windows.

Chemical diffusion processes are used to introduce the semiconductor junction-forming dopants into the bulk silicon. A series of these diffusion cycles is performed in processing of integrated-circuit wafers. Fig. 7 shows an elementary chemical diffusion system. In such a system, a coil of electrically heated wire radiates heat to raise the silicon wafers to the desired temperature (e.g., 1000 to 1300°C). A gas, such as nitrogen, is saturated by passing it through a bubble system as shown.

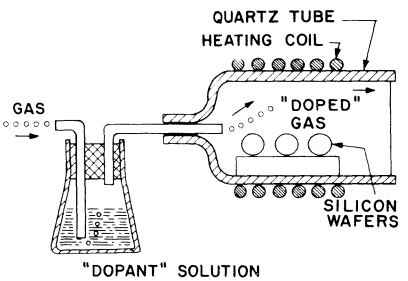


Fig. 7 — Elementary chemical diffusion system.

A solution of boron nitride can be used to supply the boron doping needed for the production of p-type material; phosphorus oxychloride is a typical source of n-type dopant.

Formation of Circuit Components

The starting material (substrate) for a monolithic integrated circuit consists of a uniform single crystal of p-type or n-type silicon. An oppositely doped (n-type or p-type) epitaxial layer is grown onto the substrate material, and a very thin film of silicon-dioxide insulation is formed on the surface of the epitaxial layer. Fig. 8 shows the resultant wafer structure when a p-type starting material is used. Diffusion processing techniques permit introduction of doping impurities to de-

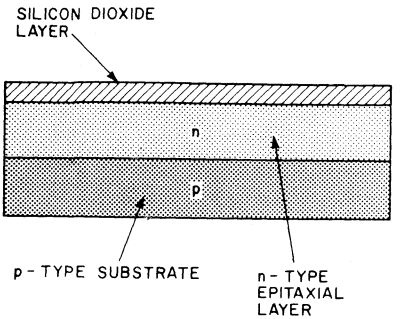


Fig. 8 — Basic integrated-circuit wafer.

sired depths and widths in the starting material to form the desired circuit components. Vertical penetration of the impurities is controlled by the diffusion temperature and time, and lateral control of the diffusion is made possible by combination of the masking properties of silicon dioxide with photochemical techniques. The silicon-dioxide insulating material on the surface of the epitaxial layer is selectively opened (i.e., windows are formed) for each diffusion step. This insulation is subsequently replaced except in metal-contact areas.

The following paragraphs summarize the basic processes involved in the formation and interconnection of electronic components on a basic integrated-circuit wafer of the type shown in Fig. 8. The fabrication of a simple series circuit, which includes an n-p-n transistor, a resistor, and a capacitor, is described. The resistor employed in this circuit is formed by a p-type diffusion, and the capacitor is a metal-oxide-semiconductor (MOS) type. Other types of resistors and capacitors may also be employed in monolithic integrated circuits, as discussed subsequently in the section on **Effects of Monolithic Fabrication on Circuit Design.**

As the initial step in the formation of electronic components, p-type material is diffused vertically into the n-type epitaxial layer to form isolated n-type circuit nodes in the regions in which the components are to be located, as shown in Fig. 9. The diode junctions formed by the n-type nodes and the p-type material provide electrical isolation between the nodes. Low-resistance n^+-type pockets (shown in Fig. 9) are diffused into the p-type substrate immediately under the isolated n-type

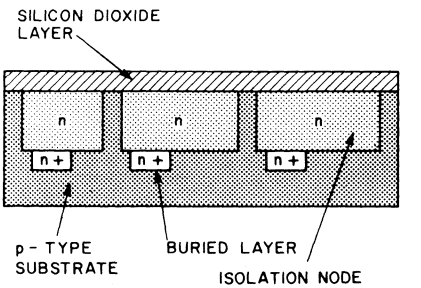


Fig. 9 — Diffusion of p-type material into n-type epitaxial layer to provide isolated n-type circuit nodes.

nodes. The n-type epitaxial material is used for the collectors of the integrated-circuit transistors, and the n^+-type pockets, referred to as "buried layers," reduce the resistance of the collector structures.

Additional p-type and n^+-type regions are diffused within the isolated n-type nodes to form a transistor, as shown in Fig. 10. The n^+-type diffusion is the emitter, the p-type diffusion is the base, and the n-type epitaxial material is the collector.

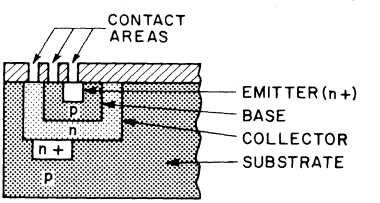


Fig. 10 — Diffusion of additional p-type and n-type regions to form transistors.

Fig. 11 shows that the process used in the formation of a p-type diffused resistor is identical to that employed for a transistor, with the exception that the n^+-type emitter

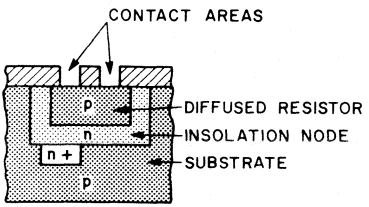


Fig. 11 — Diffusion of p-type region to form integrated resistor.

diffusion is omitted. Except that length and width are determined by the value of resistance required, the p-type diffusion used for the monolithic resistor is identical and is formed simultaneously with the p-type diffusion used for the base of the transistor. Openings are provided in the silicon-dioxide insulation to allow the deposition of the metal contacts for the transistor and the resistor, as indicated in Figs. 10 and 11.

The silicon-dioxide insulating layer is used as the dielectric for MOS capacitors. As shown in Fig. 12, a metal deposition on the surface

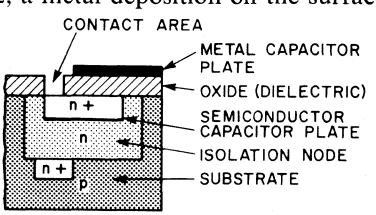


Fig. 12 — Use of oxide as a dielectric to form integrated capacitor.

of the oxide layer forms one conducting surface of the capacitor, and an n^+-type region is diffused into the n-type epitaxial layer to form the other conducting surface. Fig. 13 shows a cross section of the integrated-circuit wafer after deposition

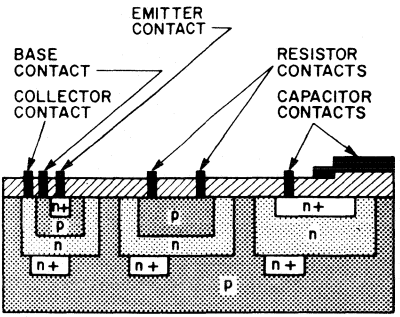


Fig. 13 — Addition of metallized contacts to circuit elements.

of the metal contacts for the transistor, the resistor, and the capacitor. Fig. 14 shows the additional metallization required to interconnect the various components and the electrical-circuit diagram of the resultant structure.

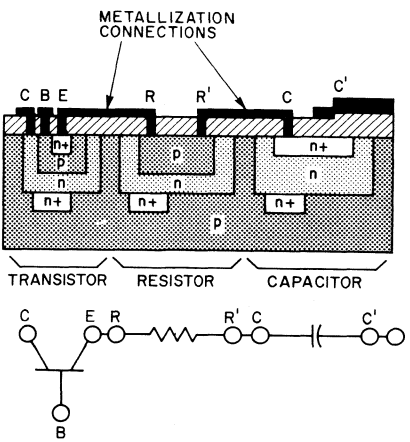


Fig. 14 — Completed silicon chip containing transistor, resistor, and capacitor and electrical-circuit diagram of the interconnected elements.

Metallization

The series of oxidation and diffusion operations culminates in an integrated-circuit wafer that contains the desired electronic elements, e.g., transistors and resistors. High-con-

ductivity metallic paths are then needed to interconnect these elements. The metallic interconnections terminate at the edges of the integrated-circuit chip as pads to which tiny wires are subsequently bonded to make connections to the package terminals (as shown in Figs. 2 and 3). Aluminum is most frequently used as a metallization material.

The metallization process is comprised of three facets: metal deposition, interconnection pattern delineation, and alloying. Metal deposition is performed by placing the processed wafer in a vacuum of about 10^{-6} torr. The source material (e.g., aluminum), also in the vacuum chamber, is then heated above its vaporization point by means of induction, resistance, or electron-beam heating techniques. As a result, metal is released by vaporization and condensed on the integrated-circuit wafer, coating it completely to a controlled thickness. The metal-coated wafer is then subjected to photolithographic procedures, including application of photoresist lacquer, exposure to ultraviolet light through a photomask having the desired pattern, and the removal of unwanted metal by acid etching. The resulting interconnection patterns are similar to that shown in Fig. 2. Finally, in order to assure excellent electrical contact between the aluminum and the electronic elements, the metallized wafers are heated in a furnace for a controlled period to permit a slight alloying of the aluminum with the semiconductor junctions.

Probe Testing

Elaborate automatic equipment has been developed to test chips while they are constituents of a complete wafer. The test procedure is frequently called "wafer-probing." A large number of needle-tipped probes make simultaneous electrical contact with the aluminum electrode pads on each chip. The probing equipment is designed so that the wafer is indexed automatically, with the probes contacting the individual chips sequentially. Once the wafer is set up mechanically, it can be completely tested automatically. A wafer containing 800 chips might produce 30,000 parameter readings, all of which are condensed into a comprehensible summary so that wafer-processing procedures can be accurately monitored. Various forms of data logging and computers accomplish this chore.

Assembly and Final Testing

After the probe testing of the wafer is completed, the individual circuit chips must be separated and assembled into integrated-circuit packages. The packaged devices are then subjected to hermeticity, environmental, and final electrical testing. (Integrated circuits supplied in plastic packages are not hermetically sealed and, therefore, are not subjected to hermeticity tests.) The sequence of events employed for these operations is as follows:

Scribe, Dice, Sort, and Inspect— The individual chips in a wafer are separated by a technique similar to that used in glass cutting. A fine diamond point is used to "scribe" the wafer with its constituent chip pattern. The actual separation into chips is accomplished by an operation called "dicing," which is simply a system of mechanical fixturing by which stress is applied to the wafer in such a manner that mechanical separations occur along the scribed lines. "Sorting" is the rejection of chips which were found to be defective in wafer-probing or dicing operations. Microscopic inspection of each

chip is performed to cull out circuits with visible imperfections.

Chip Bonding—In this procedure, the chip is mounted in the package. The actual bonding agent is frequently an epoxy, although some circuits are soldered to the package with gold alloys at temperatures of 300 to 400°C in a process referred to as eutectic bonding.

Lead Bonding—After the chip is firmly affixed in the package, electrical connections to the terminal-post leads must be made. Aluminum wires of about 1.5-mil diameter are commonly used to make these connections. Ultrasonic bonding apparatus is frequently used to attach the wire to both the metallization pad on the chip and the package terminal post. Thermocompression bonding may also be used to connect the leads between the bonding pads and the package terminals. Fig. 3 shows the chip after the lead-bonding operation.

Capping and Sealing—The lead-bonded header is usually subjected to cleaning and vacuum bake-out operations prior to sealing. Actual sealing is accomplished by a variety of means, depending to some extent on the package design. Local application of heat (e.g., welding) is used to seal the cap to the package header. This step is conducted in an atmosphere of dry gas, such as nitrogen. This gas then becomes the ambient atmosphere within the integrated-circuit package. In the case of non-hermetic packages like plastic, the lead-bonded chip assembly is encapsulated in plastic or epoxy materials.

Hermeticity and Environmental Tests—Hermeticity testing is used to confirm the leak resistance of the package. The helium leak-detection technique is frequently used. In this method, completed packages are placed in an atmosphere of helium pressure for a period of time. Helium is able to penetrate through imperfections into the package. After removal from the helium pressurization chambers, sensitive mass-spectrograph leak detectors are used to detect helium "oozing" out of any imperfection in the package. Mechanical shock, vibration, acceleration, and thermal shock testing are useful techniques to screen out devices which have inadequate margins against anticipated stresses for the particular class of service in which the integrated circuit is to be applied.

Final Electrical Testing—Wafer-probing of integrated-circuit chips is usually limited to static parameter tests because the length of probe leads and other factors prevent meaningful ac, rf, or pulse testing. Consequently, final electrical testing is performed on packaged units. Integrated-circuit test equipment is almost entirely automated. Most of the test equipment contains provisions for data logging (e.g., on magnetic tape or punched cards) so that computer analyses may be conducted for the purposes of process control and surveillance. Management of integrated-circuit test data is a difficult task because the material is so voluminous. It is not unusual to test, record, and monitor a hundred parameters on each integrated-circuit chip.

PACKAGE CONFIGURATIONS AND THERMAL CAPABILITIES

Integrated circuits are currently packaged in three distinct configurations: the TO-5-style glass-metal package, the ceramic flat pack, and

the dual-in-line package. The dual-in-line package may be either ceramic or plastic. The TO-5-style package may be supplied with 8, 10, or 12 leads; the flat pack has 14 leads; and the dual-in-line packages have 14 or 16 leads. Fig. 15 shows the different types of integrated-circuit packages. Detailed dimensional outlines and the JEDEC type number designations for the basic integrated-circuit packages and for variations of the basic packages are shown in the **Outlines** section of this manual.

Ceramic packages, whether flat-pack or dual-in-line types, have excellent hermeticity and package integrity, but their cost is high because of the complexity of their fabrication process. At present, dual-in-line plastic packages are achieving rapid popularity in the industry. Molded packages of this type are less costly than ceramic packages.

The basic thermal considerations for monolithic silicon integrated circuits do not differ significantly from those of discrete-component circuits. The heat dissipated by the circuit components must be transferred to the outside of the package without the temperature at any point on the circuit chip becoming excessive.

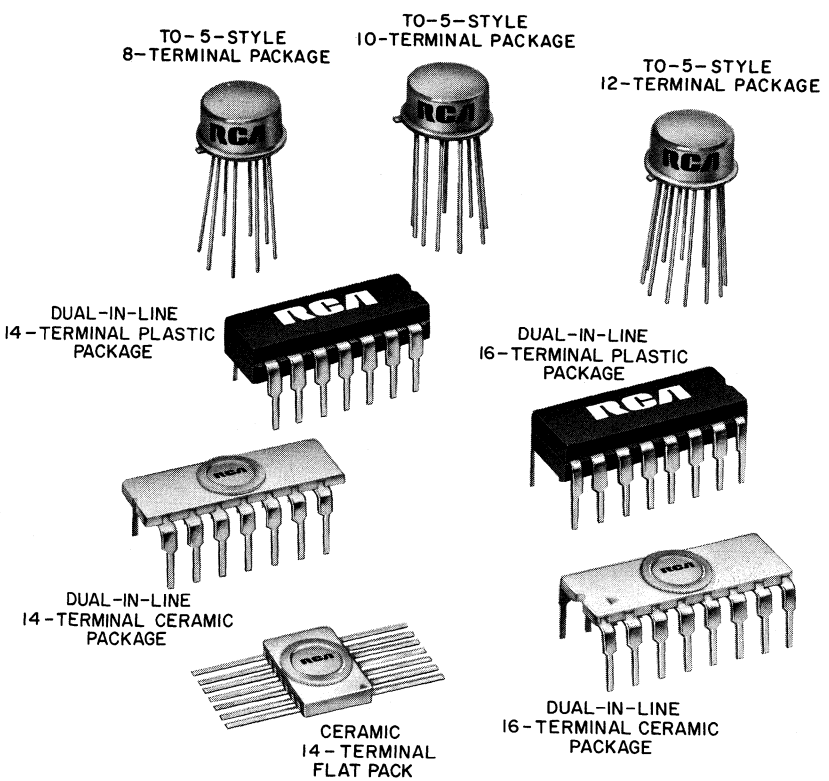


Fig. 15 — RCA integrated-circuit packages.

In an integrated circuit, all the heat is dissipated by active and passive components on top of the silicon chip. The heat sources, therefore, are highly localized, with the exact distribution determined by the circuit layout. Because the silicon chip mounted on a metal header is a good heat conductor, the heat rapidly diffuses throughout the chip, and the entire chip may be considered essentially isothermal. It is more meaningful, therefore, to examine the dissipation capability of the over-all chip than to determine the limits of each of the various localized regions. The dissipation capability of a monolithic silicon circuit chip is determined primarily by the encapsulation material, the chip mount, the terminating leads, and the volume and area of the integrated-circuit package.

The predominant mode of heat transfer in an integrated circuit is conduction through the silicon chip and through the case; the effects of internal free convection and radiation and lead conduction are small and may be neglected. The **thermal resistance** from pellet to case depends upon the pellet dimensions, the package configuration, and the location of the selected case reference point.

The **maximum allowable power dissipation** P_d in an integrated circuit is a function of the maximum storage temperature T_S, the maximum ambient temperature T_A, and the thermal resistance from pellet to case $\theta_{P\text{-}C}$ [i.e., $P_d = (T_S - T_A)/\theta_{P\text{-}C}$]. These parameters are usually specified in the manufacturer's published data on the integrated circuit.

For an RCA ceramic flat pack, the thermal resistance is typically 140°C per watt, the recommended maximum storage temperature is 150°C, and the recommended maximum ambient operating temperature is 125°C. For integrated circuits in TO-5-style packages, the thermal resistance is typically 140°C per watt, the recommended maximum storage temperature is 150°C, and the recommended maximum ambient temperature is 125°C. For dual-in-line packages, the thermal resistance is typically 70°C per watt for ceramic types and 150°C per watt for plastic types. The recommended maximum storage and ambient temperatures are, respectively, 85°C and 70°C for plastic packages, and 150°C and 125°C for ceramic packages.

MOUNTING AND CONNECTION TECHNIQUES

The selection of a particular method for mounting and connection of integrated circuits in equipment depends on the type of integrated-circuit package involved; on the equipment available for mounting and interconnection; on the connection method used (soldered, welded, crimped, etc.); on the size, shape, and weight of the equipment package; on the degree of reliability and maintainability (ease of replacement) required; and, of course, on cost considerations. The configuration, dimensions, and terminal arrangement for each type of RCA integrated-circuit package are shown in the **Outlines** section of this Manual.

The sizes and shapes of the solder-pad terminations for 14-lead flat-pack integrated circuits depend on whether "in-line" or "quad-formed" terminal configurations are used. The sizes and shapes of pads for TO-5-style circuits will depend on the effective lead-circle diameter. In all cases the minimum permissible diameter for lead holes (after plat-

ing) is 20 mils; the maximum permissible diameter depends on the sizes and shapes of the associated pads.

For applications in which speed and facility of installation and removal are major considerations (for example, in laboratory and testing applications), devices can be mounted in commercially available sockets. Table I lists and provides a brief description of some commercially available sockets for integrated circuits by manfacturers' and/or suppliers' parts numbers. This list is based on manufacturers' and/or suppliers' published information and is not necessarily complete. Sockets having mechanical and electrical characteristics comparable with those of the devices listed may also be available from other manufacturers and/or suppliers of electronic components.

Table I — *Integrated-Circuit Sockets*

Type of Integrated-Circuit Package	Manufacturer or Supplier•	Mfr's. or Supplier's Part No.	Description
	Augat, Inc.	316-AG1A	For printed-circuit boards
		316-AG3A	For chassis mounting
		116-AG3A	High-Temperature Teflon,* for printed-circuit boards
		116-AG3B	High-temperature Teflon, for chassis mounting
16-Lead dual-in-line (plastic or ceramic)	Barnes Corp.	029-275-02	For printed-circuit boards (maintains factory-lead taper)
		029-275-12	For chassis mounting (maintains factory-lead taper)
	Cinch Mfg. Co.	133-51-92-008	Gold-plated contacts { diallyl } for printed-
		133-51-92-002	Electro-tin contacts { phthalate } circuit boards
		133-51-02-007	Gold-plated contacts { GP black } or chassis
		133-51-02-006	Electro-tin contacts { phenolic } mounting
	Eby Sales Co.	IC-16LL	For printed-circuit boards
		IC-17LL	For chassis mounting
	AMP Inc.	583109 (0 thru 7)	Header (requires crimping machine)
		583110 (0 thru 7)	Receptacle
	Azimuth Electronics	5100-2	For use at temperatures up to 200°C
14-Lead flat pack	Barnes Corp.	MD-55	For use at temperatures up to 125°C
		MD-75	For use at temperatures up to 200°C
	Jettron Products, Inc.	71-062	———
		71-005	Plug-in printed-circuit card
14-Lead flat pack in RCA carrier	Barnes Corp.	029-001	For production batch testing
		029-090	For laboratory or environmental applications
	Augat, Inc.	314-AG10	For printed-circuit boards
		314-AG3A	For chassis mounting
		114-AG1B	High-temperature Teflon, for chassis mounting
		114-AG1A	High-temperature Teflon, for printed-circuit boards
14-Lead dual-in-line (plastic or ceramic)	Barnes Corp.	029-275-01	For printed-circuit boards (maintains factory-lead taper)
		029-275-11	For chassis mounting (maintains factory-lead taper)
		029-271-01	Contactor for accepting device in 029-240 carrier for automatic testing

Table I — *Integrated-Circuit Sockets (cont.)*

Type of Integrated Circuit Package	Manufacturer or Supplier•	Mfr's. or Supplier's Part No.	Description
	Cinch Mfg. Co.	133-51-92-005	Gold-plated contacts } diallyl } for printed
		133-51-92-001	Electro-tin contacts { phthalate { circuit boards
		133-51-02-003	Gold-plated contacts } GP black { or chassis
		133-51-02-004	Electro-tin contacts { phenolic } mounting
	Eby Sales Co.	IC-14LL	For printed-circuit boards
		IC-15LL	For chassis mounting
	Augat, Inc.	8058-1G19	Miniature, Teflon, for chassis mounting
		8058-39G3	Miniature, Teflon, for printed-circuit boards
	Barnes Corp.	MG-802	Miniature, Teflon, press-fit type
		MGR-81	Miniature, Teflon, for printed-circuit boards
8-Lead TO-5-style		MF-02-8	For chassis mounting chamfered-lead entrance
		MF-03-8	For printed-circuit boards, chamfered-lead entrance
	Cinch Mfg. Co.	133-98-92-061	Miniature, diallyl phthalate, for printed-circuit boards
	Augat, Inc.	8058-1G22	Miniature, Teflon, for chassis mounting
		8058-2HG1	Miniature, Teflon, for printed-circuit boards
	Barnes Corp.	MG-1002	Miniature,Teflon, press-fit type
		MGR-102	Miniature, Teflon, for printed-circuit boards
10-Lead TO-5-style		MF-02-10	For chassis mounting, chamfered-lead entrance
		MF-03-10	For printed-circuit boards, chamfered-lead entrance
	Cinch Mfg. Co.	133-99-92-054	Miniature, diallyl phthalate, for printed-circuit boards
	Sealectro Corp.	Series 60	Press-fit type, Teflon
	Barnes Corp.	MG-1201	Miniature, Teflon, press-fit type
		MGR-121	Miniature, Teflon, for printed-circuit boards
		MF-02-12	For chassis mounting, chamfered-lead entrance
12-Lead TO-5-style		MF-03-12	For printed-circuit boards, chamfered-lead entrance
	Sealectro Corp.	Series 60	Press-fit type, Teflon

• **Manufacturers' and/or Suppliers' Addresses:**
AMP Inc., Harrisburg, Pennsylvania 17105; Augat Inc., 33 Perry Avenue, Attleboro, Massachusetts 02703; Azimuth Electronics, Denville, N. J. 07834; Barnes Corporation, Lansdowne, Pennsylvania 19050; Cinch Mfg. Co., 1501 Morse Avenue E1, Grove Village, Ill. 60007; Eby Sales Co. of N. Y., 148-05 Archer Ave., Jamaica, N. Y. 11435; Jettron Products, Inc., 56 Route 10, Hanover, N. J. 07936; Sealectro Corp., 225 Hoyt Street, Mamaroneck, N. Y. 10543.

* Registered Trade Mark, E. I. DuPont DeNemours & Co.

Ceramic Flat Packs

The RCA 14-lead ceramic flat-pack integrated circuits may be interconnected with other circuit elements by a variety of soldering or welding techniques in any one of three basic mounting arrangements. These various techniques are described and the relative merits of each type are discussed in the following paragraphs:

Soldering Techniques—Figs. 16 through 20 show five methods for making soldered connections to RCA integrated circuits in 14-lead flat packs. In the **straight-through** method, shown in Fig. 16, the leads are bent downward at a 90-degree angle and inserted in 24-mil-diameter holes in the printed-circuit board.

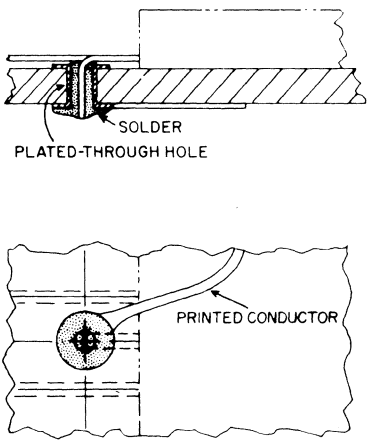


Fig. 16 — Straight-through interconnection method for RCA flat packs.

Connections to all 14 leads may be made simultaneously in a dip-soldering or wave-soldering operation. To assure good solder-fillet formation around the lead ends, the leads should extend approximately 15 to 30 mils below the bottom of the circuit board. To assure that the holes will be filled with solder to form good electrical connections, the holes must be "plated-through." Replacement of the package can be accomplished by melting and removing the solder around each lead by means of a "solder gobbler."

A disadvantage of the straight-through method is that the integrated-circuit package must be held firmly in position during the soldering operation, Another disadvantage is that the clearance between the lead and the hole is critical. Optimum "wicking" in dip- or wave-soldering is achieved when the lead has a circular cross-section and a diameter 6 mils less than the lead hole.

The **clinched-lead full-pad** method shown in Fig. 17 requires an additional operation (clinching of the lead), but has the advantage that the integrated-circuit package does not have to be held in position during the soldering operation. This method also has the following additional advantages over the straight-through method: (1) because the electrical connection is made on the pad, the hole-to-lead diameter ratio is not critical, and the lead holes therefore can be larger—a feature which simplifies insertion of the

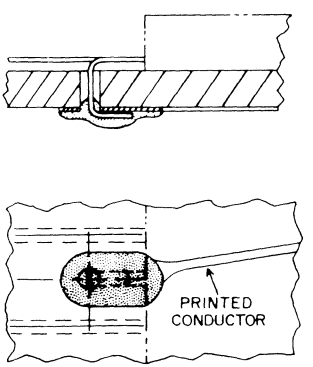


Fig. 17 — Clinched-lead full-pad interconnection method for RCA flat packs.

leads; (2) the solder connections are more reliable (because of the larger wetted area, and better mechanical contact); (3) plating of the holes is neither necessary nor desirable (non-plated holes retain less solder and the integrated circuit may, therefore, be more easily removed if replacement is necessary).

The **clinched-lead offset-pad** method shown in Fig. 18 and the

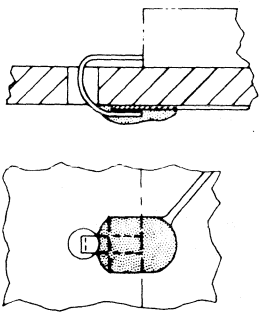


Fig. 18 — Clinched-lead offset-pad interconnection method for RCA flat packs.

clinched-lead half-pad method shown in Fig. 19 are variations of the

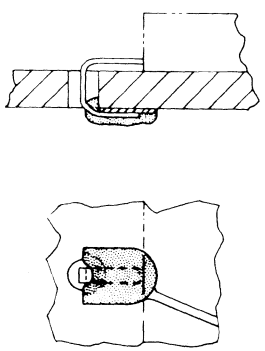


Fig. 19 — Clinched-lead half-pad interconnection method for RCA flat packs.

clinched-lead full-pad method that provide greater maintainability because the lead holes are free of solder and only partially filled with solder, respectively; the device therefore, can be more easily removed if replacement is necessary. The reliability of these connections probably is not as great as that of the clinched-lead full-pad type shown in Fig. 17.

In the **surface-connection** method shown in Fig. 20, the connections are made on the package side of the printed-circuit board. This method has the following advantages: (1) drilling of the circuit board is not required; (2) bending or special forming of the integrated circuit leads is minimized; (3) higher component packing densities are practicable because components may be mounted on both surfaces of the printed-circuit board.

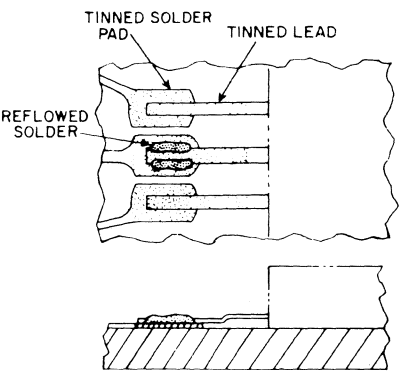
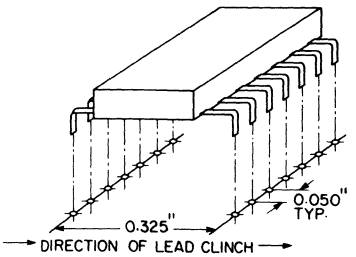
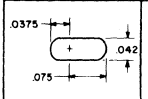
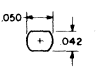


Fig. 20 — Surface interconnection method (reflow soldering) for RCA flat packs.

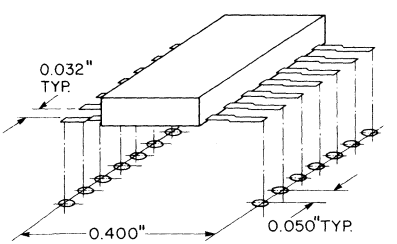
A disadvantage of the surface-connection method is that dip- or wave-soldering cannot be used. However, multi-lead "reflow soldering" systems are available in which all seven leads on one edge of a 14-lead flat package can be soldered simultaneously. Another disadvantage of the surface-connection method is that the integrated-circuit package must be held in position during the soldering operation.

Mounting Patterns—The mounting patterns shown in Fig. 21 employ **in-line** lead and pad arrangements. Although such in-line lead and pad arrangements simplify lead-forming requirements, they result in very close spacing between leads (approximately 32 mils), and require



SUGGESTED MINIMUM PAD SIZES (INCHES)	HOLE DIA. (INCHES) after plating	REMARKS
	.020 min.	For use at points of clinched lead attachment
	.020 min.	For non-adjacent plated through hole terminal areas
	.020 min.	For adjacent terminal areas on .050 centers when clinched lead attachment is not used (shaved .050 dia. pad)

(a)

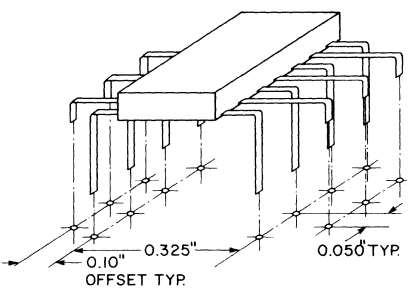


(b)

Fig. 21 — In-line lead and terminal arrangements for RCA 14-terminal flat packs: (a) through-the-board mounting method; (b) surface mounting method.

the use of high-precision manufacturing techniques in both board manufacture and assembly, particularly when the leads must be inserted through holes in the printed-circuit board, as in Figs. 16 through 19. Another disadvantage of the in-line arrangement is the limited space available for routing circuit conductors between adjacent solder pads.

Some of these disadvantages can be overcome by the use of **quad-formed** lead arrangements, as shown in Fig. 22. In these quad-formed arrangements, the lead holes and terminal pads for adjacent leads on the same edge of a flat package are offset by some convenient distance from the in-line axis. Although this staggered lead arrangement requires somewhat more circuit-board area per device than the in-line arrangement, it provides several advantages: (1) tolerances are far less critical,



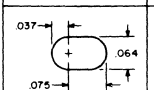
SUGGESTED MINIMUM PAD SIZES (INCHES)	HOLE DIA. (INCHES)	REMARKS
	.030 ± .003	For use at points of clinched lead attachment
	.030 ± .003	For terminal areas not used for clinched lead attachments

Fig. 22 — Quad-formed-lead mounting arrangement for RCA 14-terminal flat packs.

(2) larger terminal pads can be used, (3) even with larger pads more space is available for routing circuit conductors between adjacent terminal connections, and (4) larger lead holes can be used to simplify lead insertion.

In a quad-formed lead arrangement a good compromise between loss of available circuit-board area

and gain in the number of conductors that can be routed between adjacent circular terminal pads can be achieved by the use of a 100-mil offset between adjacent pads. With this combination, standard manufacturing tolerances are applicable, and a 10-mil annular surface (a practicable minimum) is provided on each solder pad.

A quad-formed terminal arrangement can provide great flexibility in circuit wiring configurations. If offset lead holes 30 mils in diameter and circular solder pads 80 mils in diameter are used, at least one 8-mil-wide printed conductor can be routed between adjacent solder pads. If 60-mil-diameter solder pads are used, up to two 8-mil-wide printed conductors can be routed between adjacent pads.

The maximum offset that can be achieved with RCA 14-lead flat-pack integrated circuits is 150 mils, based on a lead length of ¼ inch. When this maximum offset is used, only the straight-through type of connection shown in Fig. 16 is practicable.

Welded Connection Techniques— For some applications of integrated circuits, it may be necessary or desirable to use welded rather than soldered connections to the devices. Figs. 23 through 25 show three methods which may be used for making such welded connections. In general, the mechanical space considerations described above for soldered connections (lead bending, tolerances, etc.) apply equally for welded connections.

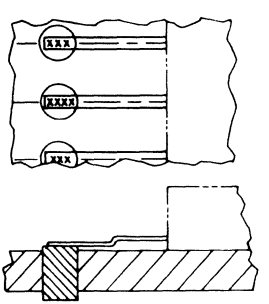


Fig. 23 — Post welding method for RCA flat packs.

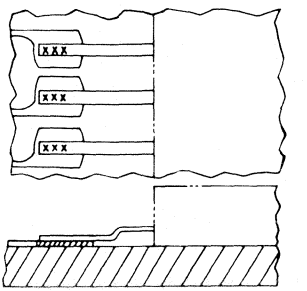


Fig. 24 — Surface-pad welding method for RCA flat packs.

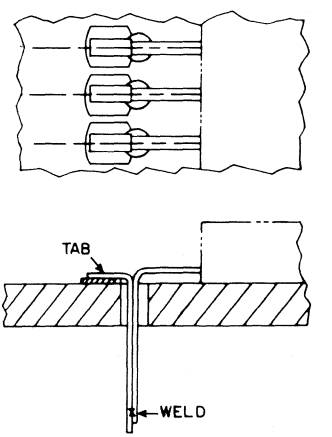


Fig. 25 — Tab welding method for RCA flat packs.

Although for some applications welding may provide more reliable connections than soldering, it has the disadvantage that with conventional welding equipment only one connection can be made at a time.

The "tab" method shown in Fig. 25 provides a high degree of maintainability because the integrated cir-

cuit can be easily removed if replacement becomes necessary. This method employs "cross-wire" resistance welding, in which the weld is made at the ends of the device lead and the terminal tab. The device can thus be removed simply by clipping the leads just above the weld points. This method, however, requires that terminal tabs and solder pads be provided on the printed-circuit board.

TO-5-Style Packages

The most direct method for mounting RCA integrated circuits in 8-lead, 10-lead, and 12-lead TO-5-style packages is shown in Fig. 26. In this method, the leads of the device are simply inserted in the proper plated-through holes in the printed-circuit board and connection is completed by dip- or wave-soldering.

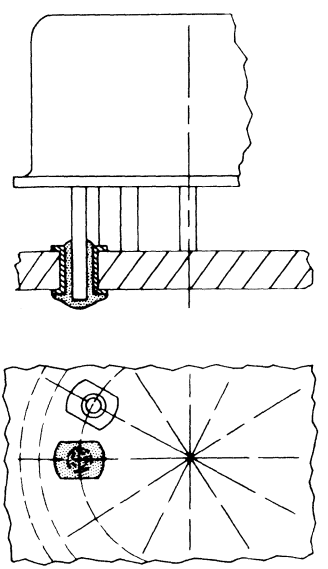


Fig. 26 — Straight-through mounting method for RCA TO-5-style packages.

Although this method of mounting requires minimum handling of the device (trimming of terminal leads to appropriate lengths may be necessary), it does require extremely precise drilling and "through-plating" of the lead holes and preparation of solder pads on a 230-mil-diameter circle. It also has the disadvantages that automatic insertion of the device leads in such limited space can present problems, and that the device must be held in position during the soldering operation.

The in-line method shown in Fig. 26 and the radially-offset method shown in Fig. 27(a) both make it possible to achieve effective "wicking" because they provide a nearly optimum relationship between lead diameter (18 mils) and lead-hole diameter (24 mils).

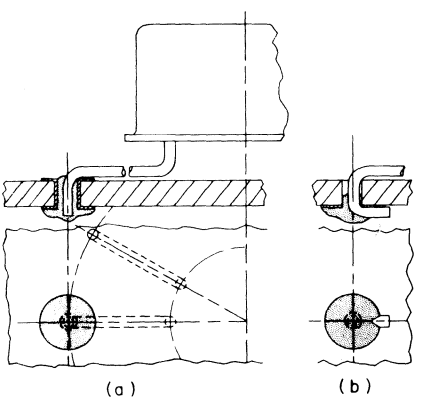


Fig. 27 — Straight-through mounting method for RCA TO-5-style packages: (a) with leads radially offset; (b) with radially offset leads that provide a clinched-lead option.

Fig. 27(b) shows a variation of the method shown in Fig. 27(a), in which the holes are not plated through and the leads are clinched before the soldering operation is performed. Because the electrical connection depends on the solder on the pad and not on the solder in the

hole, the lead-hole diameter can be made larger and, therefore, lead insertion is easier. Furthermore, the clinching of the leads helps to hold the device in position during soldering. Fig. 28 shows the lead-hole arrangement for straight-through mounting of the 10-lead TO-5-style package. This arrangement, using 60-mil-diameter pads, provides only 11 mils clearance between adjacent pads, the smallest clearance practicable without danger of shorting.

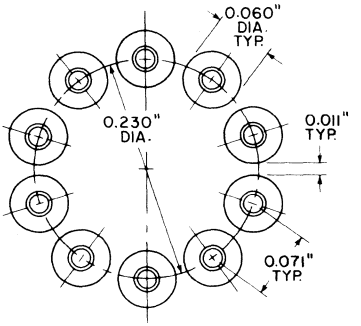


Fig. 28 — Lead-hole circle pattern for RCA 10-terminal TO-5-style package.

This separation is insufficient to accommodate a printed conductor of conventional width. It is evident that with a 12-lead TO-5-style package, the spacing between adjacent pads on a 230-mil circle will be even smaller.

Fig. 29 shows a lead-circle pattern for a 12-lead TO-5-style package in which the leads are formed to increase the effective lead-circle diameter to 530 mils. This configuration permits the use of 80-mil-diameter pads with sufficient spacing between pads to accommodiate three eight-mil-wide printed conductors. This radially offset lead-hole pattern also permits clinched-lead mounting and represents a good compromise from the standpoints of mounting arrangement, reliability, maintainability, and cost.

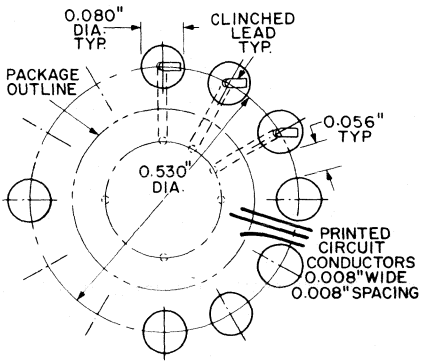


Fig. 29 — Radially offset mounting pattern for RCA 12-terminal TO-5-style package.

Dual-In-Line Packages

Fig. 30 shows the mounting arrangement used for integrated-circuits in dual-in-line packages. Because the package configurations are very similar, the mounting arrangement and terminal-sorting techniques used for these circuits are much the same as those used in the in-line method [shown in Fig. 21(a)] for the flat-pack circuits. The dual-in-line circuit is longer, however, and the soldering operation is made simpler because of the greater spacing provided between lead terminals.

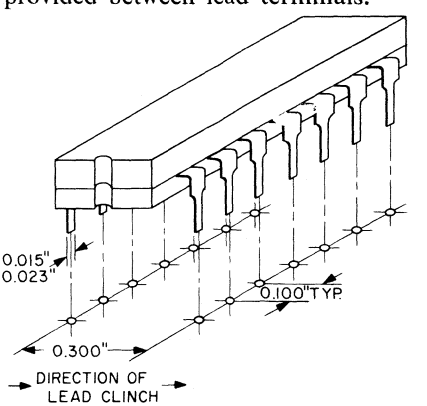


Fig. 30 — Mounting arrangement for RCA dual-in-line packages.

The terminals of the dual-in-line package may be soldered to a printed board by use of any of the through-the-board techniques (shown in Figs. 16 through 20) used for the in-line method of mounting the ceramic flat packs. The terminal leads of the dual-in-line package, however, are larger than those of flat pack. The diameter of the mounting holes drilled through the printed-circuit board must be increased to a minimum value (after plating) of 0.032 inch. The larger-size terminals are advantageous in that the increased rigidity that results enables them to be inserted more easily into the mounting holes in the printed-circuit board, or into an integrated-circuit socket.

Another significant feature of the terminals for the dual-in-line package is the sharp step increase in width near the package end. This step forms a shoulder upon which the package rests when mounted on the board; the package, therefore, is not mounted flush against the board. As a result, it is possible to run printed-circuit wiring directly under the package, convection cooling is increased, and the circuit can be more easily removed if a replacement is required.

Lead-Bending and Forming Considerations

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the leads be supported and clamped between the bend and the seal, and that bending be performed with extreme care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead or, in the case of rectangular leads such as those used in RCA 14-lead flat-pack integrated circuits, less than the lead thickness. It is also extremely important that the ends of the bent leads be perfectly straight and parallel to assure proper insertion through the holes in the printed-circuit board.

Bending, forming, and clinching of integrated-circuit leads produce stresses in the leads and can cause stresses in the seals if precautions are not taken. In addition, wide variations in temperatures during normal use result in stresses in these devices. Tests of 14-lead flat-pack integrated circuits conducted under worst-case conditions, in which the packages were rigidly attached to posts extending from the printed-circuit board, showed that over a temperature swing of 180°C (from −55°C to + 125°C) the stress de-

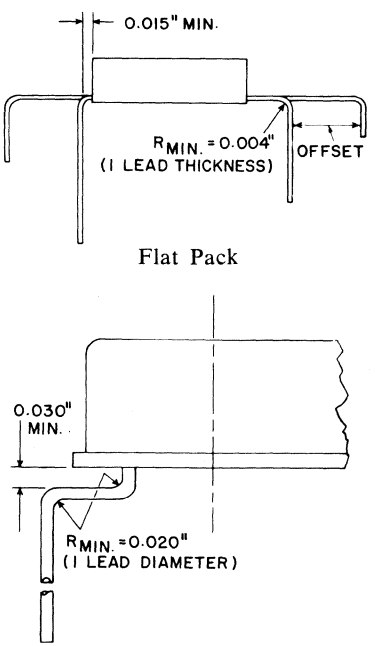


Fig. 31 — Lead-forming requirements for RCA integrated-circuit packages.

veloped in the leads, the tensile pull on the leads, the shear stress introduced in the seal, and the tensile stress developed in the seal were all well within the limits for these materials. The use of thermal stress-relief bends is, therefore, not necessary.

Lead bending and forming requirements for both flat-pack and TO-5-style packages are shown in Fig. 31.

Effects of Monolithic Fabrication on Circuit Design

The design of linear circuits involves selection and interconnection of an optimum combination of active and passive components to accomplish a signal-processing function with maximum efficiency and minimum cost. This general rule is valid whether the components are conventional ones fabricated separately by a variety of processes or integrated components formed simultaneously by a single technology. The new design considerations introduced by the advent of integrated-circuit technology arise not from any differences in the fundamental electronic properties of the components individually, but from the technical and economic implications of simultaneous fabrication and interconnection.

The perfection of monolithic integrated-circuit technology has made possible simple (and economic) reproduction of transistors and diodes with remarkably similar characteristics on the same silicon chip. Resistors with comparatively good similarity can also be fabricated simultaneously on the chip by monolithic processes. In addition, because circuit elements are fabricated from the same materials in close proximity on a single silicon chip, thermal gradients are held to a minimum; therefore, optimum tracking characteristics are inherent in monolithic integrated circuits. These and other factors must be thoroughly understood and used to maximum advantage to realize the full potential of monolithic technology in the design of linear circuits.

COMPARISON OF DISCRETE AND INTEGRATED COMPONENTS

Active and passive components fabricated by diffusion processes on or within a common silicon substrate exhibit unique characteristics that differ significantly from those of corresponding discrete components. In addition, electrical isolation in discrete-component circuits is accomplished by physical separation of individual circuit elements. Because monolithic circuits do not provide a distinct physical separation of the individual circuit elements, other means must be used to provide the required electrical isolation. For example, monolithic transistors are isolated from the common substrate by use of reverse-biased p-n junctions. Adjacent transistors are often electrically blocked from each other by two back-to-back diode junctions. DC isolation in excess of 10 megohms can be achieved

by the junction method. Similar isolation is also required for passive components.

Integrated Transistors

The majority of the transistors used in linear monolithic integrated circuits are bipolar n-p-n types. The cross section of a typical monolithic transistor, shown in Fig. 32, illustrates that these transistors are very similar to discrete transistors fabricated by the silicon planar process.

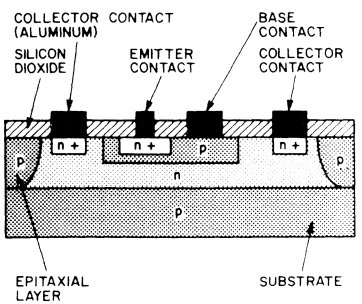


Fig. 32 — Cross section of a typical monolithic transistor.

Monolithic transistors differ from discrete types in that an effective diode (n-p isolation junction) is formed by the n-type collector and the p-type substrate material. This diode junction must always be reverse-biased to assure normal transistor operation. The collector of an n-p-n monolithic transistor, therefore, must be maintained at a positive potential with respect to the integrated-circuit substrate.

It is also important that the collector-base junctions of monolithic n-p-n transistors do not become forward-biased during normal circuit operation. As shown in Fig. 32, the p-type substrate and the collector and base of a monolithic transistor form the structure for an associated (parasitic) p-n-p transistor. In the p-n-p device, the substrate forms the collector, and the collector and base of the n-p-n transistor function, respectively, as the base and emitter. This substrate p-n-p transistor structure can sometimes be used to advantage in the design of complementary n-p-n/p-n-p circuit stages.

During normal circuit operation, the base-collector junction of a monolithic n-p-n transistor should not be forward-biased in excess of 0.6 volt unless the current in the base lead is limited by a relatively large resistance (1000 ohms or more). Otherwise, the parasitic p-n-p transistor is turned on, and high currents can flow into the substrate. Unwanted currents in the substrate can also develop if the collector of the n-p-n transistor is left open because the p-n-p transistor then operates in the V_{CEO} mode.

Because the basic process used in the fabrication of integrated circuits is very similar to the silicon planar process used to fabricate discrete transistors, the characteristics of transistors formed by monolithic technology are very similar to those of comparable discrete types. The major difference is the additional capacitance introduced in monolithic transistors by the reverse-biased substrate isolation diode.

Integrated transistors on the same circuit chip have a number of advantages over discrete units as a result of their proximity. Adjacent transistors receive almost identical processing and thus are closely matched in characteristics. Because of the close spacing, minimum temperature differences occur between components, and this close match is maintained over a wide operating-temperature range. In addition, integrated circuits can contain many more transistors per given area than discrete components. In a typical high-frequency silicon transistor,

less than 10 per cent of the wafer area is used by the active device. The remaining area serves as a support for the bonding pads and as a "handle" for the transistor. Six integrated transistors in a circuit would use less silicon than the single discrete transistor shown in Fig. 33. Therefore, integrated-circuit technology is most efficiently utilized when circuit designs are based on the use of a maximum number of matched active components.

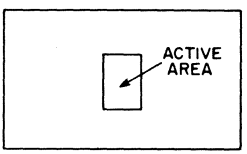


Fig. 33 — Discrete-transistor chip.

Integrated Diodes

Monolithic diodes may be formed by n-type diffusion into the silicon substrate. Such junctions, however, are essentially the same as the emitter-base junctions of monolithic transistors. When it is desirable to match diodes to transistors on the same silicon chip, a monolithic transistor is usually connected to operate as a diode, as shown in Fig. 34. Connection of the collector and base of a monolithic transistor to serve as the anode of the diode provides a two-element device which matches the base-to-emitter voltage characteristics of the normal transistor. The emitter-to-base junction of a monolithic transistor should not be used alone for diode applications if electrical and thermal matching to a transistor is required. The connection shown in Fig. 34 provides a low-voltage diode with low series resistance for general-purpose use as well as for biasing purposes.

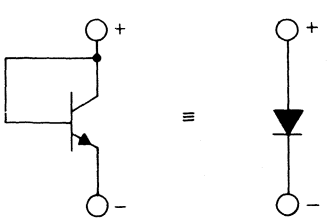


Fig. 34 — Diagram showing use of a transistor as a diode.

Integrated Zener Diodes

The emitter-base junction of a monolithic transistor may be biased in the reverse direction to provide a zener diode. For standard RCA devices, the zener voltage is approximately 7 volts, and the dynamic impedance is between 60 and 100 ohms. In this connection, shown in Fig. 35(a), the diode exhibits a positive coefficient with temperature in the order of 2 millivolts per °C.

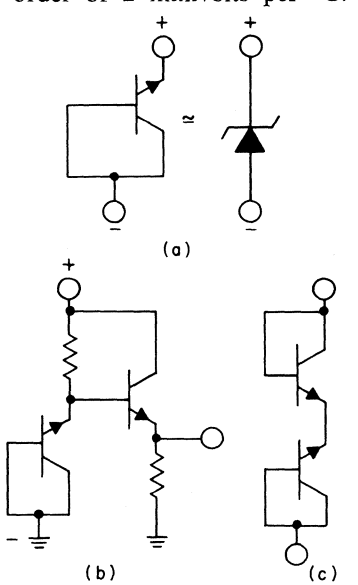


Fig. 35 — Diagrams showing (a) use of a transistor emitter-base junction to provide a zener diode, (b) connection of a transistor emitter-follower to provide lower dynamic impedance, and (c) a temperature-compensated zener diode.

When lower dynamic impedance is desired, a transistor may be used as an emitter follower for the diode, as shown in Fig. 35(b). This configuration provides an equivalent zener voltage of approximately 6.3 volts and a temperature coefficient of +4 millivolts per °C. Fig. 35(c) shows an arrangement for a higher-impedance zener diode which is nearly temperature-compensated; this diode provides a zener voltage of approximately 7.7 volts.

Integrated Resistors

Monolithic resistors are significantly different from discrete types. Discrete resistors are usually made in standard form factors, and different resistance values are obtained by variations in the resistivity of the material. In monolithic integrated circuits, only a few different resistivities can be provided; as a result, incremental values of resistance are determined primarily by the geometry of the resistors.

The **p-type diffused resistor** shown in Fig. 36 is the type most commonly used in monolithic integrated circuits. As explained previously in the section on **Fabrication, Packaging, and Mounting,** this type of resistor is formed by a p-type base diffusion. Such resistors have a **sheet resistivity** of approximately 200 ohms per square. The resistor value R is determined by the product of the sheet resistivity ρ_S and the ratio of length l to width w (i.e., $R = \rho_S \times l/w$). The range of practical values for p-type diffused resistors is approximately 100 to 25,000 ohms.

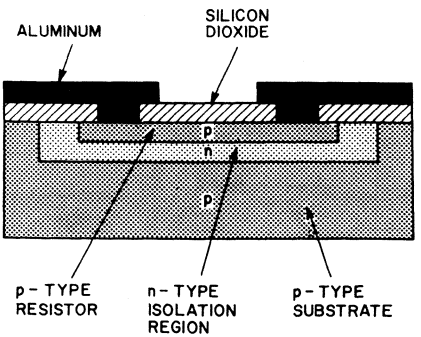


Fig. 36 — Cross section of a p-type diffused resistor.

Higher values for monolithic resistors can be obtained by addition of an n^+-type diffusion on the normal p-type diffused resistor, as shown in Fig. 37. The addition of the n^+-type layer, in effect, reduces the cross-sectional area of the resistor and eliminates the higher-conductivity path near the surface. Resistors of this type, which are called **pinch resistors,** have sheet resistivities in the order of 5000 ohms per square. Practical values for pinch resistors range from approximately 10 kilohms to 500 kilohms.

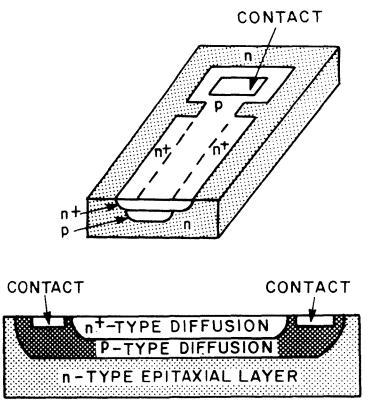


Fig. 37 — Structural views of a pinch resistor.

The epitaxial layer of a monolithic integrated circuit may also be used to form high-value resistors. Fig. 38 shows top and cross-sectional views of this type of resistor. The length and width of **epitaxial resistors** are defined by the isolation diffusion. Depending upon the **bulk**

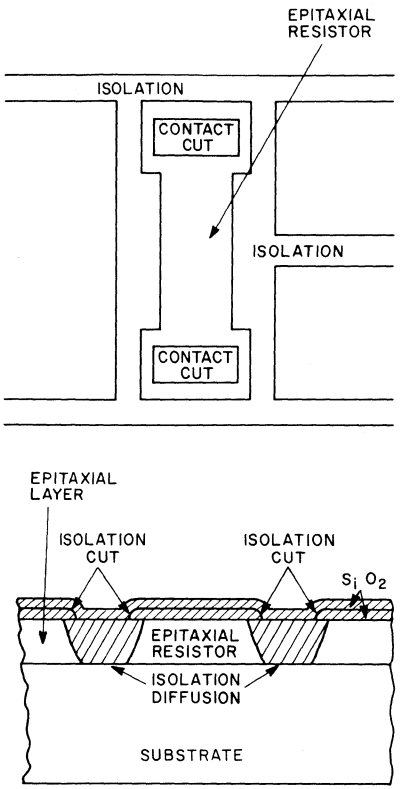


Fig. 38 — Top and cross-sectional views of an epitaxial resistor.

resistivity of the epitaxial material employed, sheet resistivities of 1000 to 5000 ohms per square can be achieved. The practical range of values for epitaxial resistors is approximately 10 kilohms to 500 kilohms. A disadvantage of epitaxial resistors is that they require more chip area for a particular value of resistance than is required for pinch resistors.

Integrated-circuit resistors have several undesirable properties which are not encountered with discrete resistors. Because of variations in diffusions and etchings, the tolerance on nominal resistance values is approximately ±30 per cent for p-type diffused resistors, from −50 to +100 per cent for pinch resistors, and ±50 per cent for epitaxial resistors. The temperature coefficients of monolithic resistors are also relatively large. The temperature coefficient is approximately +0.2 per cent per °C for p-type diffused resistors, approximately +0.5 per cent per °C for pinch resistors, and approximately 19 per cent per °C for epitaxial resistors.

However, the ratio of integrated-circuit resistors of the same type can be closely controlled. For example, the ratios of p-type diffused resistors can be maintained within 2 or 3 per cent. Integrated-circuit designs, therefore, should be made dependent upon ratios rather than absolute values of resistors.

Integrated Capacitors

The capacitors used in monolithic circuits are also vastly different from their discrete counterparts. Monolithic capacitors may be either **diffused-junction types** or **metal-oxide-semiconductor (MOS) types.**

Any reverse-biased semiconductor junction has a depletion region which acts as a dielectric between two conductive surfaces. The capacitances of such junctions, however, vary with the reverse-bias voltage and with the physical size and doping concentration of the junction. For a reverse-bias voltage of 5 volts and the impurity concentration used in a typical monolithic transistor, the capacitance per area is typically 0.07 picofarad per square mil for a collector-substrate junction, 0.10 picofarad per square mil for a base-collector junction, and 0.39 picofarad per square mil for an emitter-base junction.

For MOS types of integrated capacitors, an n^+-type emitter diffusion in a collector region (i.e., in an n-

type node) forms the bottom conductive surface, the silicon-dioxide insulating layer on the surface of the integrated-circuit chip serves as the dielectric, and the metallization acts as the top electrode. The value of this type of integrated capacitor is equal to the product of its area A and the ratio of the dielectric constant E to the thickness d of the silicon-dioxide layer (i.e., $C = A \times E/d$). Because d is maintained constant, capacitor values vary directly with area. Fig. 39 shows a cross section of an MOS capacitor.

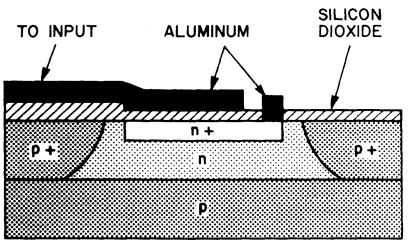


Fig. 39 — Cross section of a typical MOS type of monolithic capacitor.

The relatively large area required for integrated capacitors usually restricts their values to a range of approximately 3 to 30 picofarads. Use of larger values is uneconomical because of the disproportionate amount of chip area required and, therefore, should be avoided.

Simulated Inductors

The fabrication of monolithic inductors is not feasible for any significant values of inductance. Among other factors, circuit losses in monolithic inductors are intolerably high. Use of monolithic amplifier circuits in "active network synthesis" is a technique employed to eliminate the need for inductors which are large, heavy, and expensive. For example, integrated-circuit operational amplifiers are being employed in circuits which obey laws of inductance, but without the need for large coils of wire and metal cores. This type of application is described in the section on the **Operational Transconductance Amplifier.**

MATCHED COMPONENT CHARACTERISTICS

In general, a practical efficient monolithic design takes advantage of the close match in electrical and thermal characteristics of monolithic components that results because of their proximity on the minute silicon chip.

Matched Voltage-Transfer Characteristics

The base-to-emitter voltages of two integrated-circuit transistors operated at the same emitter current typically are matched to within 0.5 millivolt. This match in base-to-emitter voltage, however, is degraded at both high and low current levels. The match in base-to-emitter voltages is also degraded when the transistors are spaced farther apart on the silicon chip. Although the match in base-to-emitter voltage is reasonably predictable, the specification of this parameter for a high-yield product should allow an offset voltage of as much as 5 millivolts.

Matched Current-Transfer Characteristics

The current-transfer characteristics of adjacent transistors typically are matched to within 2 to 3 per cent over a current range of 50 microamperes to 1 milliampere. As with voltage-transfer characteristics, the match in current-transfer characteristic is degraded at lower or higher current levels or with increased separation of the transistors

on the silicon chip. The match in current-transfer characteristic is also adversely affected when the collector-to-emitter voltages of the transistors are substantially different, particularly if this voltage for one of the transistors should approach the breakdown value. A high-yield product specification should permit a maximum mismatch in current-transfer characteristics of 15 per cent.

Matched Thermal Characteristics

If no power were dissipated on the integrated-circuit chip, all transistors on the chip would be at the same temperature. When one or more of the transistors dissipate power, however, thermal gradients are developed on the chip. The magnitude of these gradients depends upon the amount of dissipation, the relative location of the transistors, and the type of package used. Because the characteristics of the transistors are temperature-dependent, it is important to assure the same operating temperature for transistors that are required to exhibit matched characteristics. (A difference in temperature of 0.5°C results in a change in offset voltage of 1 millivolt.) Sensitive transistors should be placed equidistant from dissipating components to assure that they are maintained at the same temperature.

POWER-OUTPUT AND VOLTAGE-GAIN CAPABILITIES

Monolithic integrated circuits are used to optimum advantage in complex small-signal applications because power dissipation problems can become formidable rather suddenly for such devices used in power-circuit applications. A number of monolithic integrated circuits are available, however, that have a power-output capability of 1 watt. The RCA-CA3020A integrated circuit, for example, can provide this level of power output with a voltage gain of 75 dB.

Monolithic integrated circuits offer spectacular voltage-gain capability. Circuits that provide voltage gains in the range from 50 to 95 dB are common. The RCA-CA3035 integrated circuit, for example, provides a voltage gain in excess of 118 dB at 40 kHz for operation from a single dc power supply of 9 volts. The RCA-CA3043 provides a voltage gain greater than 72 dB at 10.7 MHz and, in addition, provides functions of voltage regulation, FM detection, and audio preamplification. Operational amplifiers, which have reached new heights of popularity (and economy) as monolithic integrated circuits, can provide an open-loop voltage gain greater than 90 dB at a power-output level of 0.25 watt.

SUPPLY-VOLTAGE LIMITATIONS

Specifications for the maximum dc supply voltage that can be safely applied to an integrated circuit are given in the manufacturer's published data to ensure that voltage ratings will not be exceeded in any part of the circuit. The most critical voltage rating is usually the collector-to-emitter breakdown voltage $V_{(BR)CEO}$. Although it is anticipated that the continuing efforts to develop improved processing techniques will result in higher breakdown levels in the future, the collector-to-emitter voltage breakdown rating for the conventional n-p-n transistors used in silicon monolithic circuits at present is typically in the range of 15 to 40 volts. This low rating substantially restricts the maximum value of dc voltage that may be safely applied to monolithic integrated circuits.

Supply voltages should be applied to monolithic integrated circuits in the usual polarity required for n-p-n transistor stages. If the polarity is reversed, the normally reverse-biased collector-substrate isolation junction will conduct very heavily and cause a portion of the metallization pattern to be destroyed. In battery-operated circuits, or other circuits in which supply leads could conceivably be reversed, the use of a protective diode in the dc supply line is recommended.

Any length of ribbon or wiring on a printed-circuit board has inductance that can develop significant voltages in response to high-frequency or fast-rise currents. Such voltages are added to the dc supply voltage of an integrated circuit mounted on the board. In addition, the supply-lead metallization of the integrated circuit may develop high-frequency signals as a result of stray internal feedback. Adequate compensation for both effects can be achieved by bypassing the supply leads of high-gain units with small external silver-mica or high-Q ceramic capacitors. The bypassing elements should be located as close to the integrated-circuit supply terminals as possible.

COST FACTORS

Most of the cost of fabricating a monolithic silicon circuit is incurred in processing the silicon wafers through the various epitaxial, diffusion, and photochemistry operations. These costs are the same for any circuit wafer. As a result, the smaller the circuit, the greater the number of circuits that can be obtained on a given size wafer and, consequently, the lower the cost per circuit. Therefore, area minimization is an important consideration. The relative area requirements of different integrated components are as follows:

Component	*Relative Area*
Transistor	1
1000-ohm Resistor	2
10-pF Capacitor	3

These ratios are approximations that will be continually modified as technological advances are made. However, the basic relationships (that transistors use less area than resistors, which in turn are more compact than capacitors) will persist. Because area determines cost, these relationships indicate that economical integrated-circuit designs require minimization of the number of passive components. The requirement is exactly the reverse of the economic design rule for discrete-component circuits.

BASIC DESIGN RULES

Achievement of an optimum design for a monolithic integrated circuit involves the application of techniques and concepts significantly different from those employed in the design of discrete-component circuits. For example, in the design of monolithic circuits, transistors should be used to replace resistors and capacitors whenever possible. This departure from standard practice is a direct result of the importance of surface-area considerations in relation to the fabrication and yield of silicon monolithic integrated circuits. Circuit yield is inversely proportional to the area of silicon required. The area required for a single 100-kilohm p-type diffused resistor or a 150-picofarad capacitor is approximately the same as that required for ten transistors. A 100-kilohm pinch resistor would occupy approximately one-twentieth the space required for the p-type diffused resistor.

Component tolerances assume a new and critical role in the design

of monolithic integrated circuits. As mentioned previously, silicon p-type diffused resistors normally have a tolerance on absolute values of approximately 30 per cent. The ratios of such resistors, however, can be maintained to within 3 per cent. Monolithic integrated circuits, therefore, are designed so that critical parameters are dependent upon resistance ratios rather than absolute resistance values.

The performance of monolithic integrated circuits is also enhanced when the designs take advantage of the close match in the thermal and electrical characteristics of circuit components. As mentioned previously, because of the close juxtaposition of components that are produced simultaneously from common materials by the same diffusion processes, excellent tracking of component characteristics is inherent in integrated circuits.

If integrated circuits were designed for the maximum possible applications flexibility, external terminal connections would be required for each electrode of all active devices on the monolithic chip. With this approach, essentially custom-designed packages would have to be provided for each integrated circuit, except for very simple configurations. Standardization of packages, and the attendant cost advantages that result, could not then be achieved. Moreover, from the standpoint of reliability, external terminal connections are weak links in both integrated and discrete-component circuits. The more terminals that are used, the greater the potential causes of circuit failure become. The addition of external terminal connections also directly increases the cost of both the external package and the integrated-circuit chip. The formation and interconnection of the terminals and associated bonding pads represent a substantial portion of the over-all cost of assembly and packaging of the integrated-circuit chip. Each bonding pad that must be provided on the integrated-circuit chip (one for each terminal) requires a relatively large amount of chip area (approximately twice that required for a monolithic transistor). As explained previously, chip area is inversely proportional to integrated-circuit yield. The use of a large number of circuit terminals, therefore, significantly increases pellet costs.

It is apparent from the preceding discussion that the number of terminals provided on standard integrated-circuit packages represents a compromise between economic and reliability considerations and the desired applications flexibility. As pointed out in the section on **Fabrication, Packaging, and Mounting,** RCA linear integrated circuits are supplied in 8-, 10-, 12-, 14-, and 16-terminal packages. With these packages, universal flexibility is possible only for circuits that include a maximum of 3 or 4 active devices. The limitations on the number of available package terminals impose severe restrictions in the design of multistage monolithic circuits that are required to provide several highly complex functions. At least four, and often six, terminals are required for supply-voltage, ground, and the primary input and output connections. In complex circuits, the remaining terminals can be quickly used up for firmly prescribed functions, unless considerable care is taken in circuit design. The designer often must exercise great ingenuity to retain some degree of flexibility for his circuit and to ensure that terminals are provided for connections to external components, such as

inductors and large capacitors, that cannot be conveniently fabricated by monolithic techniques. In many instances, he must use techniques and include additional circuit elements and networks that would not be required in a discrete-component equivalent of his circuit merely to reduce the number of terminals required.

In summary, integrated-circuit technology offers the circuit designer a new approach to the synthesis of electronic functions. For most effective use of this approach, a designer should observe the following basic rules:

(a) Maximize the number of active components.
(b) Make the circuit design dependent upon resistor ratios rather than absolute values.
(c) Take advantage of matched component parameters.
(d) Use the minimum number of circuit terminals.

FUNCTIONAL CLASSIFICATIONS OF LINEAR INTEGRATED CIRCUITS

Circuits intended for linear applications have a broad range of diverse design requirements and often must be essentially custom-designed for the applications in which they are used. The variety of design requirements tends to prohibit standardization of circuit designs and, therefore, greatly complicates the selection of suitable configurations for linear integrated circuits. The configurations selected must be readily adaptable to monolithic fabrication techniques and, simultaneously, must offer widespread applicability to warrant production in the large volumes required to achieve low cost per unit. Linear integrated circuits designed for mass production, therefore, are either exceptionally versatile devices that can be adapted to provide many different types of circuit functions in a variety of electronic-equipment applications, or high-performance devices designed to provide highly specialized functions in high-volume applications. The following paragraphs briefly describe the basic functional classes of RCA linear integrated circuits that result from this design philosophy.

Differential-Amplifier Types

The balanced differential amplifier is an exceptionally versatile circuit and, simultaneously, is an ideal configuration for monolithic integrated-circuit processing. On the basis of these factors, this circuit is used as the basic building block for the broad line of RCA general-purpose linear integrated circuits. These circuits, in general, exhibit excellent gain-frequency characteristics, high common-mode-rejection ratios, a wide operating-temperature range, and good output-to-input isolation. They are designed for use in a wide variety of linear applications to provide many different circuit functions, such as amplification from dc to frequencies in the vhf region, signal limiting, frequency multiplication, mixing, signal generation, and many others.

Operational (Voltage and Transconductance) Amplifiers

An operational amplifier is basically a very-high-gain direct-coupled amplifier that uses external feedback for control of response characteristics. A common configuration for operational amplifiers is a direct-coupled cascade of two balanced differential-amplifier stages, with the second stage driven push-pull by the first stage, and an appropriate output stage. This circuit is readily adapted to integrated-circuit construction techniques.

By use of external feedback networks, the operational amplifier can be employed to synthesize a broad range of intricate transfer functions and, therefore, may be adapted for use in many widely different applications. Although this type of circuit was originally designed to perform various mathematical functions, such as differentiation, integration, analog comparisons, and summation, it may also be used for numerous linear applications that have widely different transfer and response requirements. For example, the same operational amplifier, by modification of the feedback network, may be used to provide the broad, flat frequency-gain response required of video amplifiers or the peaked responses required of various types of shaping amplifiers. This capability makes the operational amplifier the most versatile configuration used for linear integrated circuits.

Integrated-circuit operational devices supplied by RCA include the conventional **operational voltage amplifier (OVA)** and the more recently developed **operational transconductance amplifier (OTA).** Both types of devices are extremely versatile and are used to provide the same types of circuit functions. The operational voltage amplifier is characterized by a very high voltage gain and a very low output impedance. The operational transconductance amplifier provides a transconductance gain and a current output. The output circuit of an ideal operational transconductance amplifier is best characterized by an infinite-impedance current generator.

Multipurpose Amplifiers

RCA offers a group of high-gain integrated-circuit amplifiers that feature exceptional applications flexibility. These versatile amplifiers may be used to provide either a narrow- or a wide-band gain-frequency response and can be operated with or without gain-control capability. In addition, they can be adapted to operate over a wide dynamic range or to provide excellent limiting characteristics. This flexibility makes possible the use of this group of amplifiers in a broad range of industrial and commercial applications.

Arrays

Integrated-circuit arrays illustrate another approach to general-purpose configurations that offer widespread utility in many different types of circuit applications. Such arrays may consist of groups of unconnected active devices, of diode quads, of transistor Darlington pairs, or of individual circuit stages. The components of an array, which are fabricated simultaneously in the same way on a silicon chip, have nearly identical characteristics. The characteristics of the various components track each other with temperature variations because of the proximity of the components and the good thermal conductivity of silicon.

The integrated-circuit arrays are especially suited for applications in which closely matched device or circuit characteristics are required and in which a number of active devices must be interconnected with non-integrable components such as tuned circuits, large-value or variable resistors, and large bypass or filter capacitors. Diode arrays, for example, are particularly useful in the design of bridge rectifiers, balanced mixers or modulators, gating circuits, and other configurations that require identical diodes. Transistor arrays make available closely matched devices that may be used in a variety of circuit applications (for example,

push-pull amplifiers, differential amplifiers, multivibrators, and dual-channel circuits). The individual transistors in the array may also be employed in circuit stages that are located in different signal channels or in cascade or cascode circuits. Arrays of individual circuit stages are very useful in equipment that has two or more identical channels, such as stereo amplifiers, or they may be interconnected by use of external coupling elements to form cascade circuits.

Special-Purpose Circuits

Special-purpose linear integrated circuits are usually designed to replace discrete-component circuits in specialized high-volume applications. Such circuits may be intended to replace the if strips in AM or FM radio receivers, the sound circuits (if amplifier-limiters, discriminators, and audio voltage amplifiers) in intercarrier television receivers, the remote amplifier for remote-control television receivers, and similar types of specialized circuits. The configurations chosen for special-purpose integrated circuits, therefore, should provide the required circuit functions at performance levels equal to or greater than those of their discrete-component counterparts.

The high gain required of the amplifier sections of the special-purpose circuits can be provided by cascades of the balanced differential amplifier, the basic building block for most of the linear integrated circuits described in this manual. The differential amplifiers, however, must be augmented by other circuits such as voltage regulators or reference-voltage supplies, FM detectors, Darlington pairs, phase splitters, and buffer stages to provide the multiple circuit functions often required in the specific application.

Basic Circuit Elements

For purposes of analysis, relatively complex monolithic integrated circuits can usually be broken down into a number of simpler building-block elements. The following basic circuit elements are typical of the types of building blocks used in monolithic integrated circuits: signal-processing stages (gain elements), constant-current sources, biasing networks, dc level-shifting circuits, supply-regulation-and-decoupling circuits, and output circuits. The monolithic-circuit design rules and device-matching considerations discussed previously must be applied in the design of these separate building blocks, which together form an efficient, well-compensated operating circuit.

BASIC SIGNAL-PROCESSING CIRCUIT—THE BALANCED DIFFERENTIAL AMPLIFIER

The balanced differential amplifier is considered the optimum configuration for the gain stages of linear integrated circuits. This circuit configuration is preferred over other possible types (a feedback pair for example) for the following reasons:

1. Advantage can be taken of the exceptional balance between the differential inputs that results from the inherent match in base-to-emitter voltage and short-circuit current gain of the two (differential-pair) transistors which are processed in exactly the same way and are located very close to each other on the same very small silicon chip.

2. The differential-amplifier circuit uses a minimum number of capacitors.

3. The use of large resistors can usually be avoided, and the gain of the differential-amplifier circuit is a function of resistance ratios rather than of actual resistance values.

4. The differential amplifier is much more versatile than other possible circuit configurations and can be readily adapted for use in a variety of equipment applications.

The differential amplifier is an ideal configuration for monolithic integrated-circuit processing, as indicated by the fact that the use of capacitors and large-value resistors can be held to a minimum. The prime reason for the selection of this circuit as the basic configuration for RCA linear integrated circuits, however, is its exceptional versatility. The differential amplifier can provide linear amplification from dc through the audio and video frequencies into the vhf region and may also be used for such functions as

signal limiting, frequency multiplication, amplitude modulation, mixing, product detection, signal generation, gain control, squelch, and temperature compensation.

The differential-amplifier configuration inherently makes possible excellent output-to-input isolation, eliminates the need for neutralization, and simplifies feedback arrangements. The close match in temperature coefficients of components fabricated from the same material on a minute silicon chip assures stable electrical characteristics over a very broad temperature range.

Circuit Operation

The balanced differential amplifier shown in Fig. 40 is the basic confiuration used to provide signal gain in linear integrated circuits. This configuration is the fundamental building block for a broad line of RCA all-monolithic-silicon integrated circuits designed for a wide variety of linear applications at frequencies from dc into the vhf region. The differential pair of monolithic transistors Q1 and Q2 function in the same way as a pair of discrete transistors operated in a similar circuit configuration. The superior match of the integrated-circuit transistors, however, permits substantially better balanced operation than a discrete-transistor circuit.

The currents to the emitter-coupled differential transistors (Q1 and Q2) are supplied from a controlled constant-current source (either a transistor or a resistor). Temperature-compensating networks can be readily incorporated as an integral part of the controlled-source circuit to assure that circuit gain, dc operating point, and other important characteristics vary as required over the operating temperature range. The differential amplifier shown in Fig. 40 is connected to operate from symmetrical dual positive and negative supply voltages (V^+ and V^-). Single-supply operation is also feasible, but requires an external voltage-divider network for proper biasing of the bases of the transistors.

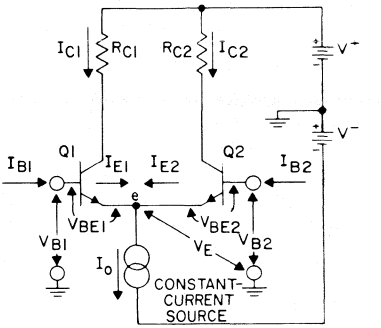


Fig. 40 — Balanced differential-amplifier configuration used as the basic gain stage for the linear integrated circuits.

The balanced differential amplifier may be considered as two symmetrically arranged "half-circuits," each with a transistor (Q1 or Q2) and a load resistor (R_{C1} or R_{C2}). If the characteristics of the transistor-resistor pairs are identical, the two "half-circuits" are perfectly matched and can be mated without introduction of a circuit unbalance when the emitters of Q1 and Q2 are joined and the transistors are operated from common dc supplies. If the two input voltages V_{B1} and V_{B2} are either zero or equal in magnitude and of the same polarity, the amplifier does not become unbalanced because the collector currents I_{C1} and I_{C2} remain equal; a zero voltage difference, therefore, is maintained between the collectors of transistors Q1 and Q2.

It is apparent from Fig. 40 that the sum of the emitter currents I_{E1} and I_{E2} is always equal to the constant source current I_O. Conse-

quently, an increase in one of the emitter currents is accompanied by an equal decrease in the other emitter current. This current relationship, of course, depends upon the quality of the constant-current source.

When the base of transistor Q1 is driven positive with respect to the base of transistor Q2 (i.e., a differential input is applied), the current through Q1 increases, and the current through Q2 decreases equally so that the source current I_O remains constant. For these conditions, I_{C1} is larger than I_{C2} and a voltage difference is developed between the transistor collectors such that the collector voltage of Q2 is more positive than the collector voltage of Q1. The differential input voltage, therefore, produces a differential output voltage. This sequence of events describes the operation of the differential amplifier in the **differential-input, differential-output mode.**

The differential amplifier is a versatile configuration that offers a number of circuit-connection modes. For example, if the voltage V_{B1} alone increases in a positive direction with respect to ground, the voltage at the collector of Q1 decreases with respect to ground. With the output taken from the collector of Q1, the differential amplifier, then, operates as though it were merely a classical single-stage, phase-inverting transistor amplifier. This type of operation is referred to as the **single-ended-input, single-ended-output inverting mode** of the differential amplifier.

In view of the fact that an increase in the current through Q1 results in an attendant decrease in the current through Q2 (to maintain a constant I_O), a positive-going increase in V_{B1} alone also results in an increase in the voltage at the collector of Q_2 with respect to ground. With the output taken from the collector of Q2, the differential amplifier then operates in the **single-ended-input, single-ended-output noninverting mode,** i.e., merely as a classical single-stage noninverting transistor amplifier.

The differential amplifier may also be operated in the **differential-input, single-ended output mode.** In this mode of operation, the output voltage is coupled from the collector of either Q1 or Q2 in response to a differential input voltage ($V_{B1} - V_{B2}$) applied between the bases of the two transistors.

The ratio of the change in collector voltage to the "difference" in the base voltages is the **differential voltage gain** (A_d). If the collector-to-collector voltage is used in the gain ratio, the result is referred to as the **double-ended differential-voltage gain** (A_{dDE}). If the collector-to-ground change is used, the ratio is called the **single-ended differential-voltage gain** (A_{dSE}).

Transfer Characteristics

The variation in the collector currents I_{C1} and I_{C2} as a function of the differential input voltage $V_{B1} - V_{B2}$ is an important characteristic of the differential amplifier. The collector current can be expressed in terms of the emitter currents on the basis of the usual transistor relationships, as follows:

$$I_{C1} = \alpha_1 I_{E1}$$

$$I_{C2} = \alpha_2 I_{E2}$$

where the alpha (α) terms represent the fractional part of the emitter current that reaches the collector.

If transistors Q1 and Q2 are identical, $\alpha_1 = \alpha_2 = \alpha$. The relationships between the emitter currents and the collector currents may then be expressed by the following equations:

$$I_{C1} = \alpha I_{E1} \quad \text{or} \quad I_{E1} = I_{C1}/\alpha$$

and

$$I_{C2} = \alpha I_{E2} \quad \text{or} \quad I_{E2} = I_{C2}/\alpha$$

The following equation expresses the emitter current I_E of a transistor in terms of the base-to-emitter voltage V_{BE}:

$$I_E = I_S\left(e^{\frac{V_{BE}}{h}-1}\right)$$

In this equation, I_S represents the saturation current of the base-emitter junction (i.e., the reverse-bias leakage current of the emitter-base diode) and $h = KT/q$ where K is Boltzman's constant ($= 1.38 \times 10^{-23}$ watt-second per °C), T is the temperature in degrees Kelvin, and q is the charge on an electron ($= 1.60 \times 10^{-19}$ coulomb). At 300°K ($\approx$ 27°C), the leakage current I_S is equal to 0.2×10^{-5} ampere for some typical monolithic transistors, and the factor h is equal to 26×10^{-13} volt. For an emitter current I_E greater than 1 nanoampere, the -1 term in the equation for I_E may be neglected. The emitter currents of transistors Q1 and Q2 may then be expressed in terms of the base-to-emitter voltages as follows:

$$I_{E1} = I_{S1}(e^{V_{BE1}/h})$$

$$I_{E2} = I_{S2}(e^{V_{BE2}/h})$$

For identical transistors, $I_{S1} = I_{S2} = I_S$. Therefore, the equations for I_{E1} and I_{E2} may be rewritten as follows:

$$I_{E1} = I_S(e^{V_{BE1}/h})$$

$$I_{E2} = I_S(e^{V_{BE2}/h})$$

As stated previously, the source current I_O is equal to the sum of the emitter currents of the emitter-coupled pair of transistors Q_1 and Q_2 (i.e., $I_O = I_{E1} + I_{E2}$). Thereore, I_O is given by

$$I_O = I_S(e^{V_{BE1}/h}) + I_S(e^{V_{BE2}/h})$$

$$= I_S(e^{V_{BE1}/h} + e^{V_{BE2}/h})$$

If the term $e^{V_{BE1}/h}$ is factored out of the expression enclosed by parentheses, the equation for I_O becomes

$$I_O = I_S e^{V_{BE1}/h}[1 + e^{(V_{BE2}-V_{BE1})/h}]$$

Similarly, if the term $e^{V_{BE2}/h}$, instead of $e^{V_{BE1}/h}$ is factored out, the equation for I_O can be written in the following form:

$$I_O = I_S e^{V_{BE2}/h}[1 + e^{(V_{BE1}-V_{BE2}/h}]$$

It was previously shown, however, that $I_S e^{V_{BE1}/h}$ is equal to I_{E1} and that $I_S e^{V_{BE2}/h}$ is equal to I_{E2}. Therefore,

$$I_O = I_{E1}[1 + e^{(V_{BE2}-V_{BE1})/h}]$$

and

$$I_O = I_{E2}[1 + e^{(V_{BE1}-V_{BE2})/h}]$$

if the values $I_{C1}/\alpha = I_{E1}$ and $I_{C2}/\alpha = I_{E2}$ are substituted in the above equations, the following results are obtained:

$$I_O = \frac{I_{C1}}{\alpha}[1 + e^{(V_{BE2}-V_{BE1})/h}]$$

and

$$I_O = \frac{I_{C2}}{\alpha}[1 + e^{(V_{BE1}-V_{BE2})/h}]$$

It is apparent from Fig. 40 that the base-to-emitter voltages V_{BE1} and V_{BE2} can be expressed in terms of the input voltages V_{B1} and V_{B2}, respectively, as follows:

$$V_{BE1} = V_{B1} - V_E$$

$$V_{BE2} = V_{B2} - V_E$$

Therefore,

$$V_{BE1} - V_{BE2} = V_{B1} - V_{B2}$$

and

$$V_{BE2} - V_{BE1} = V_{B2} - V_{B1}$$

If these relationships are used, the equations for the source current I_O can be expressed in terms of the differential input voltage, as follows:

$$I_O = \frac{I_{C1}}{\alpha}[1 + e^{(V_{B2}-V_{B1})/h}]$$

and

$$I_O = \frac{I_{C2}}{\alpha}[1 + e^{(V_{B1}-V_{B2})/h}]$$

The above equations are solved for I_{C1} and I_{C2} to obtain the following expressions of collector current in terms of differential input voltage:

$$I_{C1} = \frac{\alpha I_O}{1+e^{(V_{B2}-V_{B1})/h}}$$

and

$$I_{C2} = \frac{\alpha I_O}{1 + e^{(V_{B1}-V_{B2})/h}}$$

Fig. 41, which shows the currents I_{C1} and I_{C2} as a function of the factor h = KT/q, provides a graphic representation of these equations.

The transfer curves shown in Fig. 41 provide several important points of information about the differential amplifier:

1. The transfer characteristics are linear in a region about the operating point. For the curves shown (KT/q ≈ 26 millivolts), this linear region corresponds to an input-voltage swing of approximately 50 millivolts peak-to-peak.

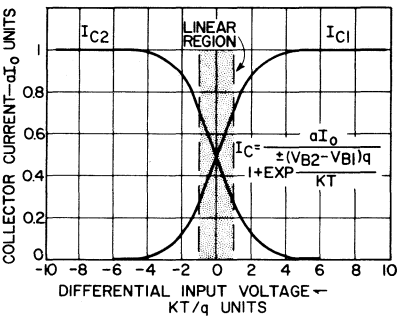


Fig. 41 — Transfer curves of the basic differential-amplifier circuit.

2. The maximum slope of the curves, which occurs at the operating point, defines the **effective transconductance** of the differential amplifier.

3. The slope of the transfer curves (i.e., the transconductance) is dependent upon the value of the total current I_O supplied to the constant-current source. The slope of the transfer curves can be changed, without changing the linear input region, by varying the value of I_O. This relationship implies that automatic gain control is inherent in the differential amplifier when the current I_O is controlled.

4. The transfer characteristics and the slopes of these characteristics are a function of the alpha of the transistors and of the temperature, both of which are predictable, and of two physical constants.

5. The differential amplifier is a natural limiter; when input excursions exceed ±4KT/q (approximately ±100 millivolts for the curves shown), no further increase in the output is obtained.

6. The output current of an amplifier is the product of the input voltage and the transconductance. In the differential amplifier, the transconductance is proportional to

the controlled current I_O; this circuit, therefore, may be used for mixing, frequency multiplication, modulation, or product detection when the current I_O is made a multiplicand and the input waveform is the multiplier.

The transconductance at the operating point (at $V_{B1} - V_{B2} = 0$) is the **maximum transconductance** of the differential amplifier and may be expressed by the following equation:

$$g_m = \frac{\alpha I_O}{4\frac{KT}{q}}$$

At an operating temperature of 25°C, the transconductance can be approximated as follows:

$$g_m = \frac{\alpha I_O}{4 \times 26\ mV}$$

The above equations reveal that, for the same value of source current I_O, the effective transconductance of the differential amplifier is one-fourth that of a single transistor. This condition results from the fact that, at the operating point, exactly one-half of the total current I_O flows through each transistor of the differential pair and the input voltage must be divided equally between the two transistors.

When the differential amplifier is operated to provide double-ended outputs so that the output voltage is measured between the collectors of the differential pair of transistors, the output currents through the load impedance contribute equally to the output voltage from each transistor. As a result, the output voltage is twice that obtained for single-ended operation. This increase in output voltage results because the load impedance is doubled, not because of any doubling of the transconductance. However, if an impedance is connected between the two collectors and the shunt collector-feed resistors are large compared to this load impedance, the load current is twice as large as can be expected from a single-ended circuit. This condition indicates an **apparent effective transconductance,** $g_{m(app)}$, for the double-ended circuit which is expressed by the following equation:

$$g_{m(app)} = \frac{q\alpha I_O}{2KT}$$

Effect of Emitter Degeneration

Fig. 42 shows a curve of transconductance as a function of the differential input voltage $V_{B1} - V_{B2}$. A study of this curve indicates that it may be desirable to increase the range of linearity of the transconductance and, thus, suggests the use of emitter degeneration. Fig. 43 shows the basic differential amplifier with two identical emitter resistors (R_E) added. The degeneration introduced by the emitter resistors reduces the gain (transconductance) of the differential pair of transistors, but it also increases the linearity of both

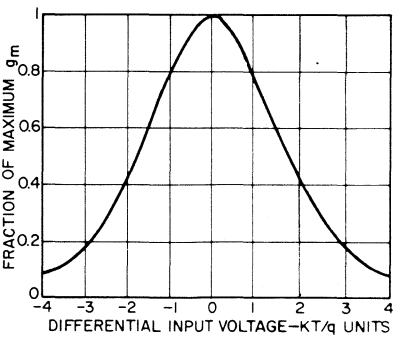


Fig. 42 — Transconductance (g_m) of the basic differential amplifier as a function of differential input voltage.

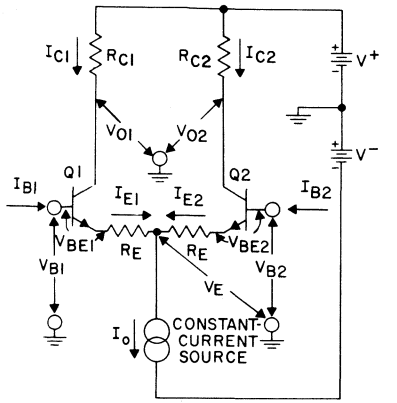


Fig. 43 — Balanced differential amplifier in which emitter degeneration is employed.

the transfer characteristics and the transconductance.

The combination of the nonlinear circuit characteristics and the linear emitter resistors does not lend itself immediately to a facile mathematical solution. A new transfer curve, which is a function of the actual level of the current I_O and the value of the emitter resistance R_E, can be constructed more easily by graphical techniques. The new transfer curve, shown in Fig. 44, is obtained from the addition, at a constant current, of the original differential-amplifier voltage drop and the voltage drop across the emitter resistor.

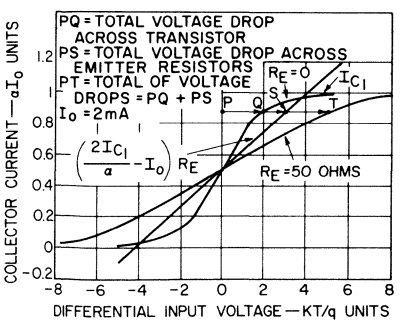


Fig. 44 — Effect of emitter degeneration on the transfer characteristics of the differential amplifier.

When emitter resistors are used, therefore, the new transfer characteristics for a differential amplifier can be determined for any given value of the current I_O by addition of the voltage drops of the differential amplifier to those of the emitter resistors. Thus, at the current value P in Fig. 44, the voltage drop across the differential pair of transistors is PQ and that across the emitter resistors is PS. The point on the combined transfer curve that corresponds to these conditions is PQ + PS = PT.

Fig. 45 shows transconductance curves for the differential amplifier shown in Fig. 43. These curves show the variation in transconductance as a function of the differential input

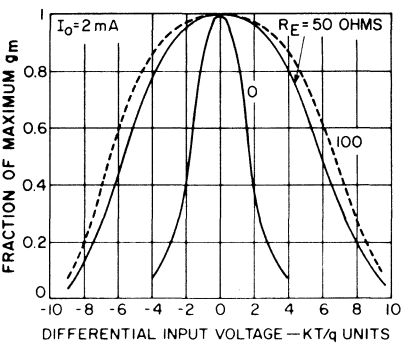


Fig. 45 — Effect of emitter degeneration on the transconductance of the differential amplifier.

voltage for emitter resistors (R_E) of 50 ohms and of 100 ohms. For comparison, the normalized transconductance of the circuit when no emitter resistors are used is also shown on the same scale.

The increased linearity of the transconductance characteristic that results from the degeneration introduced by the emitter resistors is evident from the curves shown in Fig. 45. This increased linearity, however, is accompanied by a reduction in the absolute value of the

transconductance. As mentioned previously, the use of 50-ohm emitter resistors reduces the absolute value of transconductance to one-third the original value (for an I_O of 2 milliamperes). The use of 100-ohm emitter resistors further reduces the transconductance by approximately 40 per cent.

The preceding discussion has shown that the introduction of emitter degeneration decreases the slope of the transfer characteristic (results in a more linear transconductance) and reduces the sharpness of the cutoff "knee." As a result of these factors, a higher input voltage is required to produce distortion or limiting in the differential amplifiers when emitter resistors are used.

Common-Mode Response

If the base voltages of both differential-pair transistors Q1 and Q2 are increased or decreased together (i.e., a **common-mode input voltage** is applied), then the emitter currents remain equal and, because their sum must be equal to the constant current I_O, no change in either emitter current occurs. Consequently, no change in collector output voltage results. This absence of output-voltage change in response to a common-mode input-voltage signal constitutes an ability of the differential amplifier to reject common-mode signals. The degree to which rejection is achieved depends on the impedance of the constant-current source (CCS). Because some finite impedance is always associated with the constant-current source, some small output signal is always produced in response to a common-mode signal. The ratio of this small output-voltage change to the change in common-mode input voltage is called the **common-mode voltage gain** (A_c). This gain is normally much less then unity. The ratio of the common-mode voltage gain (A_c) to the differential voltage gain is called the **common-mode rejection ratio** (CMRR),

$$\text{CMRR} = A_c/A_d$$

This common-mode rejection ratio is normally expressed in decibels as follows:

$$\text{CMRR (dB)} = 20 \log A_c/A_d$$

The common-mode rejection ratio is a measure of the ability of the differential amplifier to discriminate between differential and common-mode input signals and is usually of the order of 80 to 120 dB.

A change in common-mode voltage at the input results in a corresponding change in voltage across the constant-current source; however, there are limits to the levels of common-mode voltage that the circuit can handle before its performance is severely degraded. For example, it is apparent from Fig. 40 that if the base voltage of either Q1 or Q2 rises above the collector voltage, the transistor will be in saturation, and normal differential-amplifier operation will cease. If the base voltage decreases below some minimum level required by the constant-current source, the impedance of the constant-current source will decrease, and the common-mode rejection ratio will be degraded. This range of common-mode voltages over which the differential amplifier operates is normally called the input **common-mode voltage range,** V_{CMR}, and is usually defined for a specified distortion at the output, or for a specified degradation in the common-mode rejection ratio.

Balanced DC Amplification

The monolithic-integrated-circuit differential amplifier can provide excellent balanced dc amplification because of the close electrical and

thermal match of transistors Q1 and Q2. If the transistors were perfectly matched in terms of base-to-emitter voltage (V_{BE}), dc beta, and bulk and contact resistances, and if the resistances R_{C1} and R_{C2} were equal, the difference between the collector voltages would be zero when equal voltages were applied to the bases of the two transistors. Unfortunately, small unbalances do exist even with monolithic devices, and a small dc offset between the collectors exists when the bases are at equal potentials. When the bases of transistors Q1 and Q2 are driven from low-resistance sources, this offset results primarily from the unbalance in the base-to-emitter voltages of the two transistors. Unequal betas contribute to this offset when the bases are driven from high-resistance sources. For this condition, unequal voltage drops are developed across the resistors because unequal base currents result in a differential voltage drive at the bases.

Any of the following methods may be used to measure and specify the unbalance:

The **output offset voltage** V_{OO} is the difference in dc voltage between the collectors (for equal collector resistors) when the bases are connected to the same dc voltage within the input common-mode voltage range. The measurement can be made with or without resistors in series with the bases, but if resistors are used, they must be of equal value. This measurement is simple to make, but it suffers from a lack of generality because the measured value depends on the dc gain chosen for the test circuit.

The **input offset voltage** V_{IO} is the difference in base voltages ($V_{B1} - V_{B2}$) which must be applied to obtain equal collector dc voltages when the collector resistors R_{C1} and R_{C2} are equal. This offset is relatively independent of beta mismatch and is primarily a function of the mismatch in base-to-emitter voltages. A typical value for the input offset voltage in monolithic transistors is 1 millivolt; consequently, this voltage is more difficult to measure accurately than the output offset voltage. The input offset voltage, however, is more general because it is an offset referred to the input and is independent of circuit gain.

The **input bias-current offset** I_{IO} is the difference in input base-bias currents ($I_{B1} - I_{B2}$) when the collector voltages are equal. This offset is a measure of the beta mismatch at a particular operating current. The input bias-current offset is relatively small for low operating currents and is correspondingly larger for higher operating currents. This current offset is typically 5 to 10 per cent of the input base-bias current.

Offsets are usually specified at +25°C; additional parameters are needed, therefore, to describe the thermal match between the differential-pair transistors Q1 and Q2. The thermal match is indicated by the **offset drift** specifications, which give the change in the particular offset per degree C over a specified temperature range, as follows:

$$\text{Input Offset-Voltage Drift} = \frac{\Delta I_{IO}}{\Delta T}$$

$$\text{Input Offset-Current Drift} = \frac{\Delta I_{IO}}{\Delta T}$$

These parameters are sometimes given as curves of the input offset voltage V_{IO} and the input bias-current offset I_{IO} as a function of temperature.

CONSTANT-CURRENT SOURCE

The preceding discussion of basic differential-amplifier operation indi-

cated the need for a constant-current source (CCS) to assure that the sum of the emitter currents in the differential-amplifier transistor pair would always be constant. This condition was assumed in the development of the equations for the differential amplifier and was shown to be a requirement for good common-mode rejection. A constant-current source is an infinite-impedance source. The simplest way to approximate a constant-current source, therefore, is by use of a high-value resistor R_{CCS}, as shown in Fig. 46.

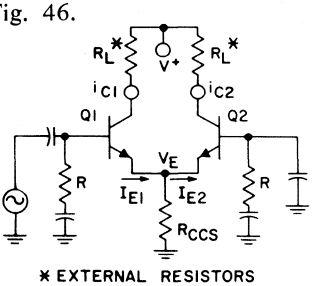


Fig. 46 — Balanced differential amplifier that uses a resistor as the constant-current source.

For balanced operation, the resistor R_{CCS} must be very large compared to the emitter impedances of transistors Q1 and Q2 to assure that the signal current i_C will not be shunted into R_{CCS} and cause the current i_{C2} to be less than the current i_{C1}. For a given operating current, the value of R_{CCS} is limited by the dc voltage required at the emitter to produce the required value for the constant current I_O. Consequently, the resistance R_{CCS} is determined on the basis of the largest value possible consistent with the minimum permissible value for the current I_O. This compromise normally results in a constant-current source which, although simple, does not provide the best balanced operation or common-mode rejection.

A transistor connected as shown in Fig. 47 provides a much better constant-current source. The impedance, as it appears at the collector of Q3, is very large, but the voltage

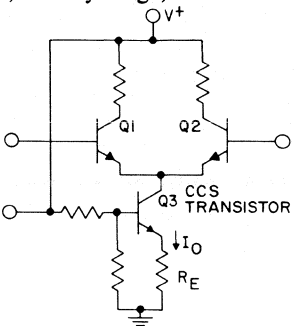


Fig. 47 — Balanced differential amplifier that uses a transistor constant-current-source circuit.

required to drive the current I_O through the resistor R_E can be relatively small because a high value of resistance is not required for R_E. The minimum voltage required at the common emitters must be just large enough to sustain the $I_O R_E$ drop plus the collector-to-emitter voltage (approximately 0.5 volt) for Q3 to prevent saturation of this transistor. The dc voltage would, of course, normally be larger than this minimum limit in order to allow for a large common-mode voltage swing at the input bases. The bias of this constant-current source can be adjusted so that the negative temperature coefficient of the forward base-to-emitter voltage of transistor Q3 approximately compensates for the positive temperature coefficient of the diffused resistor R_E. This compensation assures that the operating current is maintained nearly constant with changes in temperature. This feature is particularly important for circuits that employ external load resistors because such load resistors do not track with the internal current-setting resistor.

The temperature coefficient for the base-to-emitter voltage is approximately −2 millivolts per degree C, and the temperature coefficient of R_E is approximately +0.2 per cent per degree C. If the current I_O is to remain constant when the change in base-to-emitter voltage with temperature causes a rise in voltage across resistor R_E of 2 millivolts per degree C, the increase of 0.2 per cent per degree C in the voltage drop $I_O R_E$ caused by the change in the value of R_E with temperature must equal 2 millivolts per degree C. The quiescent $I_O R_E$ drop, therefore, must be 1 volt because 0.2 per cent of 1 volt is 2 millivolts.

When diffused load resistors are included on the chip, the emitter voltage of transistor Q3 must be mantained constant with temperature because changes in the value of R_E will be compensated for by changes in the diffused load resistors R_L. As a result, the operating point and voltage gain remain relatively fixed with changes in temperature. The circuit shown in Fig. 48 illustrates the use of diodes in the base-bias circuit to compensate for the variations in the base-to-emitter voltage of transistor Q3. The base-to-emitter voltage, therefore, is maintained at a constant value. Two diodes are required to compensate for the temperature-induced changes in the base-to-emitter voltage because the effect of the diodes on the base bias is reduced by the voltage division of the resistances. In RCA differential-amplifier circuits, the base-bias voltage is reduced by a factor of 2. This relationship is clearly illustrated by the Thevenin equivalent circuit of the base-bias network for transistor Q3 shown in Fig. 49.

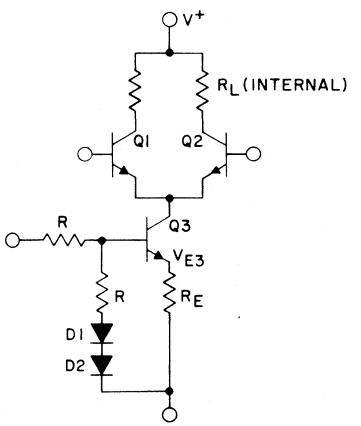


Fig. 48 — Differential amplifier in which temperature-compensating diodes are used in the base-bias network of the constant-current transistor.

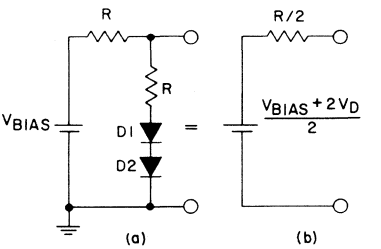


Fig. 49 — Base-bias circuit for the constant-current transistor: (a) actual circuit; (b) Thevenin's equivalent circuit.

Fig. 50 shows a third biasing method for the constant-current-source transistor. This method makes use of the fact that two matched monolithic transistors will conduct equal emitter currents if their bases and emitters are connected in parallel. D1 is a diode-connected transistor operated in parallel with the base-emitter junction of transistor Q3. The emitter current of transistor Q3, therefore, is very nearly equal to the current through D1. If the dc beta of transistor Q3 is high enough so that the base current can be neglected, the current through D1 can be expressed by the following equation:

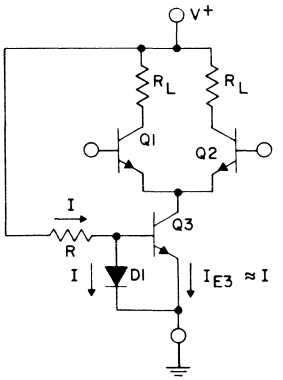


Fig. 50 — Differential amplifier in which circuit biasing is based on the match in the characteristics of two monolithic base-emitter junctions connected in parallel.

$$I = \frac{V^+ - V_{D1}}{R} = I_{E3}$$

This equation shows that the current in the constant-current source can be set by selection of the supply voltage V^+ and the resistance R because the voltage V_{D1} will always be close to 0.7 volt.

The circuit shown in Fig. 50 is similar to the one shown in Fig. 48 in respect to its behavior with variations in temperature. That is, if R and R_L are both diffused resistors, their change with temperature will have compensating effects to keep the operating voltage and voltage gain relatively constant. If they are both external resistors with low or matching temperature coefficients, the constancy will also be maintained.

BIASING CIRCUITRY

The biasing circuitry for a linear integrated circuit is an integral part of the differential-amplifier constant-current source. The following analysis of biasing methods, therefore, is essentially an extension of the treatment on the constant-current source given in the preceding paragraphs.

Biasing of One- and Two-Stage Circuits

Fig. 51(a) shows the circuit diagram for a basic constant-current

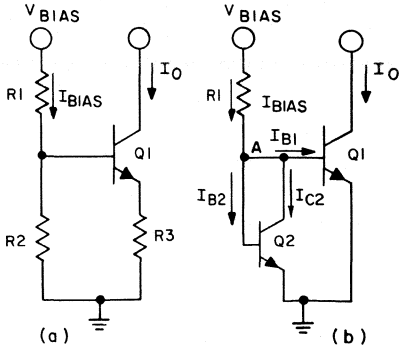


Fig. 51 — Transistor constant-current source: (a) basic circuit; (b) circuit using a compensating diode in the base-bias network.

source. The constant source current I_O can be appxoximated by

$$I_O \approx \frac{V_{BIAS}\,[R3/(R1 + R3)] - V_{BE}}{R3}$$

Because the base-to-emitter voltage V_{BE} is a function of temperature, I_O varies rapidly with temperature in this circuit unless the emitter resistor R3 is large. However, the use of a large value for R3 partially defeats the use of a transistor for the constant-current source because of the large voltage drop developed across the resistor.

The circuit shown in Fig. 51(b) avoids the problem of a large emitter resistance. If it is assumed that the forward-voltage characteristic of the diode-connected transistor matches the base-to-emitter characteristic of the transistor, the emitter current can be expressed as follows:

$$I_O \approx I_{BIAS}\frac{V_{BIAS} - V_{BE}}{R1}$$

Although I_O is also a function of the base-to-emitter voltage in this circuit, the resistor R1 is much larger than resistor R3 so that the rate of change in I_O for a change in base-to-emitter voltage is smaller, and the bias is more stable.

Achievement of accurate bias values requires that the emitter current densities (milliamperes per square mil) of transistors Q1 and Q2 be as nearly equal as possible and that both transistors have high h_{FE} ratios (greater than 40). The bases of both Q1 and Q2 are biased from the same point [point "A" in Fig. 51(b)]; the base-to-emitter voltages of these transistors, therefore, are equal (i.e., $V_{BE1} = V_{BE2}$). Moreover, if the transistors are identical, the collector currents I_{C1} and I_{C2} are equal, and the base currents I_{B1} and I_{B2} are also similar. For these conditions, the source current I_O is approximately equal (within 5 per cent) to the bias current, as shown in Table II.

The circuit shown in Fig. 51(b) can be used as an amplifier if point A is used as the input. This circuit, however, is not very practical because the input resistance is very low. The diode-connected transistor shunts the input with an impedance of a forward-biased diode, determined as follows:

$$r = 0.026/I_{BIAS}$$

The bias method shown in Fig. 52 makes greater use of the matching capabilities of the integrated circuit to achieve higher input impedances. In this method, the bias transistor is used as a transistor, not as a diode. The transistors are assumed to be matched for both V_{BE} and h_{FE}, and R2 and R3 are assumed to be equal. Because both units are biased from point "A," symmetry requires that

Table II — *Bias Relationships for Circuit Shown in Fig. 51(b)*

Conditions	Equations
Q1 and Q2 are assumed to be identical. Their base currents, therefore, are equal.	$I_{B1} = I_{B2} = I_B$
The h_{FE} of both transistors is large (>40). The collector currents of Q1 and Q2, therefore, closely approximate their emitter currents.	$I_{E1} = I_O = h_{FE}I_{B1} = h_{FE}I_B$ $I_{E2} = I_{C2} = h_{FE}I_{B2} = h_{FE}I_B$
The bias current is the sum of the currents I_{C2}, I_{B2}, and I_{B1}.	$I_{BIAS} = I_{C2} + I_{B2} + I_{B1}$ $= h_{FE}I_B + 2I_B$ $= I_B(h_{FE} + 2)$
The bias-current equation is solved for I_B	$I_B = \frac{I_{BIAS}}{h_{FE} + 2}$
Relationship for I_B is substituted in equation for I_O	$I_O = h_{FE}\frac{I_{BIAS}}{h_{FE} + 2}$ $= \frac{I_{BIAS}}{1 + (2/h_{FE})}$
For large values of h_{FE}, I_O very closely approximates I_{BIAS}.*	$I_O \approx \frac{I_{BIAS}}{1 + 0}$ $\approx I_{BIAS}$

* For h_{FE} ratios of 40 or greater, the source current I_O matches the bias current I_{BIAS} within 5 per cent.

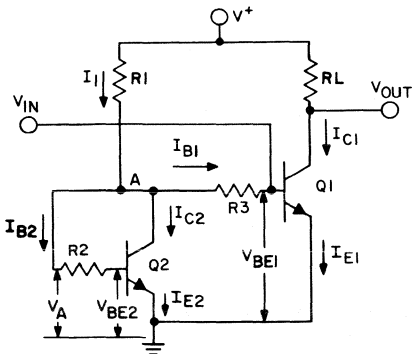


Fig. 52 — Transistor biasing circuit that uses a bias transistor rather than a bias diode.

they both must operate at the same current. Any lack of symmetry causes a mismatch of the currents. The integrated-circuit designer must take the potential unbalances into account to assure proper circuit operation. Table III shows the bias relationships for the circuit.

The circuit shown in Fig. 53(a) is a widely used two-stage amplifier. The bias conditions are easily calculated if V_{RE} and V_{BE} are assumed to be matched. If this circuit is part of an integrated circuit, point "B" must be brought to a terminal because any reasonable value of bypass capacitor cannot be integrated. This point must be bypassed to maintain a high input impedance and to retain high voltage gain.

Fig. 53(b) shows how a matching dummy amplifier may be used to eliminate the bypass capacitor [C in Fig. 53(a)] and the associated terminal [at point B in Fig. 53(a)] that would be required. Table IV shows the characteristics required for the dummy amplifier.

In this circuit, Q2 and Q3 are connected in the same manner as in the circuit of Fig. 53(a) except that no ac signals are applied to these transistors. If all the resistors are matched

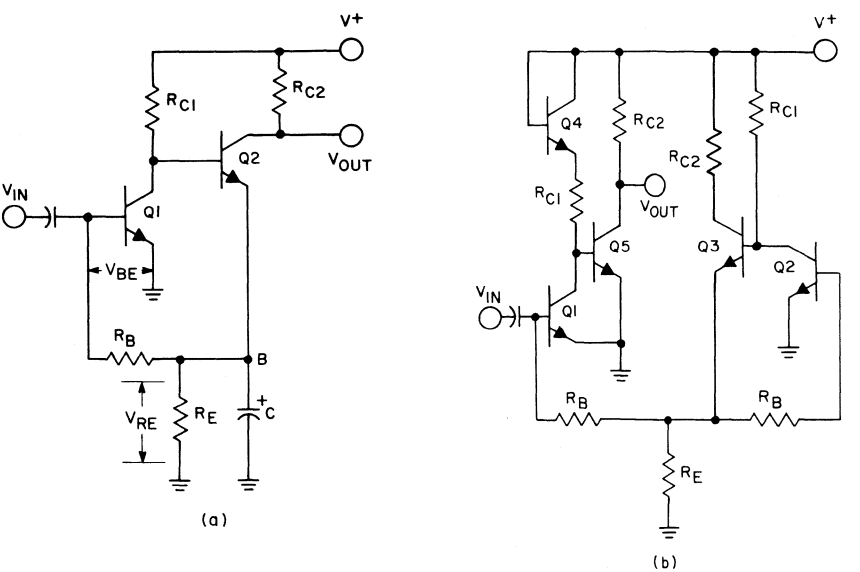


Fig. 53 — Two-stage amplifier that may be used as a biasing circuit: (a) basic amplifier; (b) addition of a dummy amplifier to basic circuit to eliminate need for an external large capacitor and associated circuit terminal.

Table III — *Bias Relationships for the Circuit Shown in Fig. 52*

Conditions	Equations
Q1 and Q are assumed to be identical transistors that have high h_{FE} ratios. The collector current of each transistor, then, is very nearly equal to the emitter current.	$I_{C1} = I_{E1} = h_{FE}I_{B1}$
The base currents of transistors Q1 and Q2 are readily determined by application of Ohm's law to Fig. 52.	$I_{B1} = \frac{V_A - V_{BE1}}{R3}$ and $I_{B2} = \frac{V_A - V_{BE2}}{R2}$
The values of resistors R2 and R3 are the same.	$R2 = R3 = R$
If transistors Q1 and Q2 are identical and the resistances of R1 and R2 are equal, then the transistors have equal base-to-emitter voltage drops and equal base currents.	$V_{BE1} = V_{BE2} = V_{BE}$ $I_{B1} = I_{B2} = I_B$ Therefore, $I_B = \frac{V_A - V_{BE}}{R}$ or $V_A = V_{BE} + I_BR$
It is apparent from Fig. 52 that the current I_{BIAS} is equal to the sum of the base currents of transistors Q1 and Q2 and the collector current of transistor Q2.	$I_{BIAS} = I_{B1} + I_{B2} + I_{C2}$ $= \frac{V^+ - V_A}{R1}$ $= \frac{V^+ - (V_{BE} + I_BR)}{R1}$
For identical transistors, $I_{C1} = I_{C2} = I_C$, and, as pointed out previously, $I_{B1} = I_{B2} = I_B$.	Therefore, $\frac{V^+ - V_{BE}}{R1} - I_BR = I_C + 2I_B$ and $\frac{V^+ - V_{BE}}{R1} = I_C + 2I_B + I_B\frac{R}{R1}$ $= I_C + I_B\left(2 + \frac{R}{R1}\right)$
V^+ is normally much greater than V_{BE} (i.e., $V^+ + V_{BE} \approx V^+$), and (for high h_{FE} ratios) I_C is much greater than I_B. The quantity $I_B(2 + R/R1)$, therefore, is negligible in comparison to I_C.	Then, $I_C \approx \frac{V^+}{R1}$

Table IV — *Approximate Characteristics for Circuit Shown in Fig. 53(b)*

$$\text{Voltage gain} = \frac{(V^+ - 2V_{BE})(V^+ - V_{BE})}{2(0.026)^2}\left[\frac{1}{1 + \frac{(V^+ - 2V_{BE})}{0.026(\beta_2)}\left(\frac{I_{C2}}{I_{C1}}\right)}\right]$$

$$R_{in}(\text{minimum}) = \frac{0.022\beta_1(\text{min})}{I_{C1}} \qquad R_B = \frac{0.140\beta(\text{min})}{I_{C1}} \qquad R_{C1} = \frac{V^+ - 2V_{BE}}{I_{C1}}$$

$$R_{out} = R_{C2} \qquad R_E = \frac{V_{BE}}{I_{C2}} \qquad R_{C2} = \frac{V^+ - V_{BE}}{2I_{C2}}$$

Example

$V^+ = 12$ V
$V_{BE} \approx 700$ mV
$I_{C2} = 1$ mA
$I_{C1} = 0.1$ mA
$\beta_2 = 100$
$\beta_1(\text{min}) = 30$

$R_{C1} = 0.1$ megohm
$R_{C2} = 5600$ ohms
$R_B = 42{,}000$ ohms
$R_E = 700$ ohms

Voltage gain $= 2.12 \times 10^3 = 67$ dB
$R_{in}(\text{min}) = 6600$ ohms
$R_{out} = 5600$ ohms

within 1 or 2 per cent, the current in Q1 is the same as that in Q2. The voltage drop across the diode-connected transistor Q4 then exactly compensates for the voltage drop across R_E in the circuit of Fig. 53(a). The operating points of Q1 and Q5 are at the levels desired, and the dynamic performance is the same as that of the discrete-component circuit.

Biasing of Multistage Circuits

Fig. 54 shows the typical relationship between the base-to-emitter voltage (V_{BE}) and collector current (I_C) of an integrated-circuit transistor. Realization of how rapidly the collector current changes with variations in the base-to-emitter voltage is essential to any valid analysis of the biasing requirements for complex linear integrated circuits. The curve shows that the collector current is

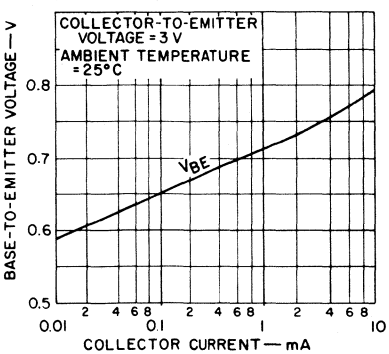
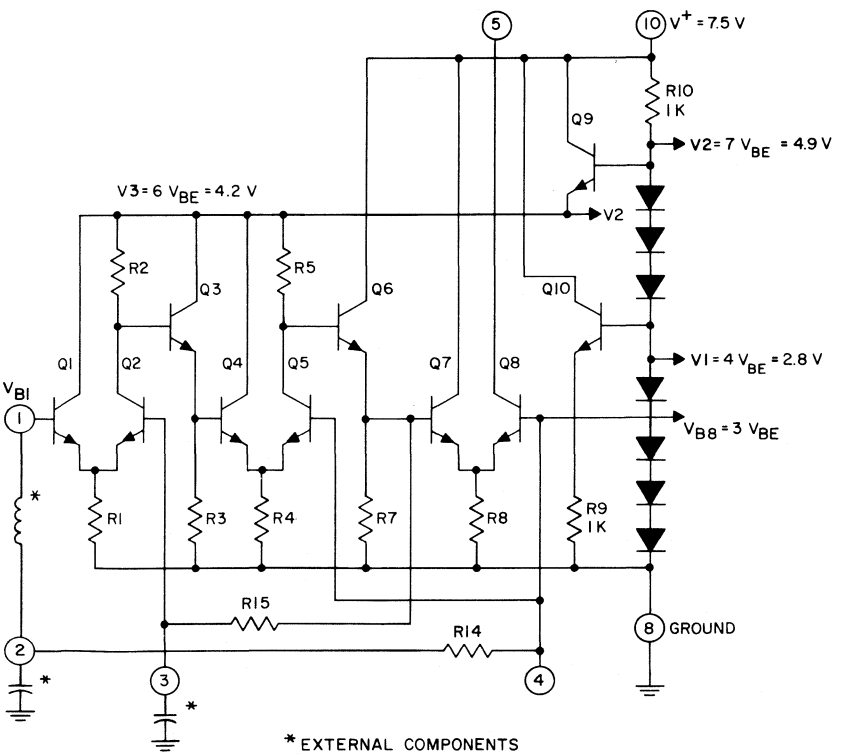


Fig. 54 — Base-to-emitter voltage as a function of collector current for a typical integrated-circuit transistor.

doubled for an increase in base-to-emitter voltage of only 18 millivolts and increases tenfold for a rise in base-to-emitter voltage of 60 millivolts. At a collector current of 1 milliampere, the base-to-emitter voltage is approximately 700 millivolts. A change in this voltage of ±10 per cent causes a maximum-to-minimum-value change of 100 to 1 in collector current. In the following circuit analyses, therefore, the voltage drops across all diode and base-emitter junctions can be assumed as 700 millivolts with reasonable expectations that the calculated operating points will closely approximate the actual values.

Fig. 55 shows the circuit diagram for a three-stage direct-coupled integrated-circuit amplifier. The required circuit gain is provided by three differential-amplifier stages (Q1 and Q2, Q4 and Q5, and Q7 and Q8). These stages are coupled toegther by emitter-follower stages (Q3 and Q6) that provide the required impedance matching and prevent a rise in the dc voltage level through successive differential-amplifier stages. (A detailed explanation of dc level shifting is provided in a subsequent discussion.) The following analysis can be used to approximate the biasing requirements for the three-stage amplifier.



All resistance values in ohms unless otherwise specified.

Fig. 55 — Multistage amplifier in which the required circuit biasing is provided by a series string of diodes.

1. All transistors and diodes and all similar-value resistors are assumed to be matched, and the voltage drop across diodes and base-emitter junctions is approximated as 0.7 volt.

2. As stated previously, the gain of a differential-amplifier stage is maximum when the stage is balanced. With no signal applied, the base voltages and collector currents of the differential-pair transistors should be equal.

3. The voltage drops across resistors R14 and R15 are assumed to be small and equal.

4. The bias for the circuit is developed by the series diode string. The bias voltage V_1 is equal to four diode voltage drops, or 2.8 volts. The bias voltage V_2 is equal to seven diode voltage drops, or 4.9 volts.

5. The bias for transistors Q1, Q5, and Q8 is derived from the voltage V_1 through the emitter-follower transistor Q10. The bias voltage V_1, therefore, is reduced by one base-emitter voltage drop so that the bias voltage applied to transistors Q1, Q5, and Q8 is equal to 2.1 volts (i.e., $V_{B1} = V_{B5} = V_{B8} = V_1 - 1V_{BE} = 3V_{BE}$).

6. If the base voltages of transistors Q1 and Q2 are equal (i.e., if $V_{B1} = V_{B2}$), the voltage drop across R1 is one base-emitter drop less than the base voltages, or $2V_{BE} = 1.4$ volts. The operating current for the first differential-amplifier stage, therefore, is 2.8 milliamperes, as determined from Fig. 55 ($I_{E1} = 2V_{BE}/R1$). One-half this current flows through resistor R2 to produce a voltage drop (1000 ohms x 1.4 milliamperes) of 1.4 volts, or $2V_{BE}$, between the supply line V_3 and the base of transistor Q3.

7. The supply-line voltage V_3 is one base-to-emitter voltage drop less than the bias voltage V_2 because of the emitter follower Q9, i.e., $V_3 = V_2 - 1V_{BE} = 6V_{BE}$, or 4.2 volts.

8. The base voltage of transistor Q3, therefore, is two base-emitter drops less than V_3, i.e., $V_{B3} = 6V_{BE} - 2V_{BE} = 4V_{BE}$.

9. The voltage V_{B4} at the base of transistor Q4 is one diode voltage drop less than the voltage V_{B3} at the base of transistor Q3 and, therefore, is equal to three base-emitter drops ($V_{B4} = V_{B3} - V_{BE} = 3V_{BE}$). This value, however, is equal to the voltage V_{B5} at the base of transistor Q5 established by the diode string (step 5). The second differential-amplifier, therefore, is balanced.

10. The first and second differential amplifiers are identical; the total current in the second stage, therefore, is also 2.8 milliamperes. Similarly, the voltage V_{B6} at the base of transistor Q6 is equal to $4V_{BE}$ and the voltage V_{B7} at the base of transistor Q7 is equal to $3V_{BE}$. (This analysis shows that $V_{B7} = V_{B2} = 3V_{BE}$, and the assumptions made in step 5 are verified.) A similar analysis can be used to check the balance of the third differential-amplifier stage. It is readily determined that the voltage V_{B8} at the base of transistor Q8 is also equal to $3V_{BE}$, which indicates that the third stage is balanced and is identical to the first two stages. The total current of the third stage, therefore, is also 2.8 milliamperes.

11. If desired, the analysis can be continued further. The emitters of transistors Q3 and Q6 are operated at $3V_{BE}$ above ground so that the emitter current for these transistors can be approximated as follows:

$$I_{E3} = I_{E6} \approx 2.1 \text{ volts}/2000 \text{ ohms} \approx 1 \text{ milliampere}$$

12. The approximate operating currents of all transistors in the

three-stage amplifier have been determined and the low-frequency gain of the circuit can be calculated.

An analysis of the type used for the three-stage integrated-circuit amplifier can also be used to determine quiescent conditions and low-frequency gain capabilities of any multistage direct-coupled differential amplifier integrated circuit.

DC LEVEL-SHIFTING CIRCUITS

The dc level of cascaded direct-coupled amplifiers rises through the successive stages toward the supply voltage, unless the circuit includes provisions to compensate for this condition. In linear monolithic integrated circuits, the dc voltage tends to build up through the n-p-n stages in the positive direction and must be shifted negatively if large output-signal swings are to be obtained. In multistage high-gain integrated circuits, such as operational amplifiers and special-purpose multifunction circuits, which use external feedback to provide a wide range of gain-bandwidth and gain-stability trade-offs, it is especially important to include provisions that compensate for the shift in dc level. Such amplifiers must have equal (preferably zero) input and output dc levels so that the dc coupling of the feedback connection does not shift any bias point.

Emitter-Follower Level-Shifting Circuit

The simplest method used to provide the required downward shift in dc level employs an emitter-follower stage between successive differential-amplifier stages, as shown in Fig. 56. The values of the resistance R_C and the current I_O are selected so that the dc voltage at the collector of transistor Q1 is two forward-biased diode voltage drops ($2V_{BE}$) above

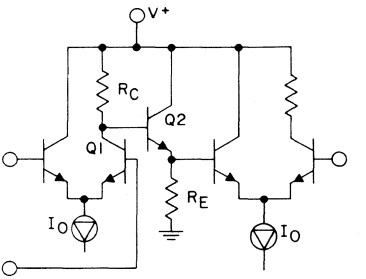


Fig. 56 — Emitter-follower dc level-shifting circuit.

the dc voltage at the emitter of transistor Q1. The voltage drop across the base-emitter junction of transistor Q2 then makes the base voltage of transistor Q3 equal to the base voltage of transistor Q1. In this way, similar stages can be cascaded with the dc collector and base voltages maintained at the same level. DC feedback is normally required to stabilize the dc operating points. A disadvantage of this technique, however, is that the collector voltage swings are limited to a peak-to-peak value of about 2 volts.

p-n-p Transistor Level-Shifting Circuits

Fig. 57 shows a level-shifting technique that allows larger voltage swings. This technique uses a p-n-p transistor between adjacent stages to shift the dc voltage downward. The required downward shift

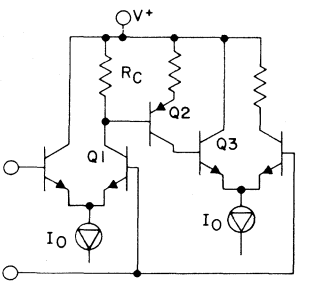


Fig. 57 — Use of a p-n-p transistor to provide dc level shifting.

between the collector voltage of transistor Q1 and the base voltage of transistor Q3 is provided by the collector-to-emitter voltage of the p-n-p transistor Q2. This latter voltage is automatically adjusted in response to a dc feedback voltage. Use of this technique tends to degrade the frequency response of the circuit because of the relatively poor common-emitter high-frequency characteristic of a monolithic p-n-p transistor. A better arrangement of p-n-p transistors for level shifting when high-frequency performance is desired is shown in Fig. 58. In this arrangement, the p-n-p level-shifting transistor Q4 is operated in the common-base mode, and signal currents in

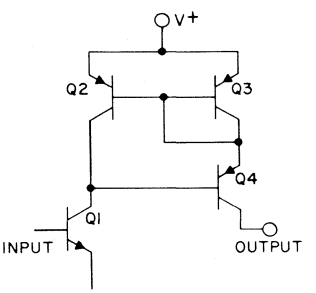


Fig. 58 — DC level-shifting circuit that uses a p-n-p transistor operated in the common-base mode.

the collector of transistor Q1 are duplicated in the emitter of transistor Q4 because of the matched characteristics of the differential-pair transistors Q2 and Q3.

Level-Shifting Output Stage

The use of an output stage such as that shown in Fig. 59 is a common technique employed to prevent a shift in dc level between the output and input of an integrated circuit. Transistor Q1 operates as an input buffer, and transistor Q2 is essentially a constant-current source for Q1. The shift in dc level is accomplished by the voltage drop across resistor R1 produced by the collector current of transistor Q2. The emitter of the output transistor Q3 is connected in a bootstrap arrangement to the emitter of transistor Q2. Feedback from this transistor through R3 results in a decrease in the voltage drop across R1 for negative-going output swings and an increase in this voltage drop for positive-going output swings.

If properly designed, the dc level-shifting circuit shown in Fig. 59 can provide substantial voltage gain, high input impedance, low output impedance, and an output swing nearly equal to the supply voltages, in addition to the desired shift in dc level. Moreover, feedback may be coupled from this circuit to the differentiial-amplifier stages to compensate for dc common-mode effects that result from variation in the dc supply voltages.

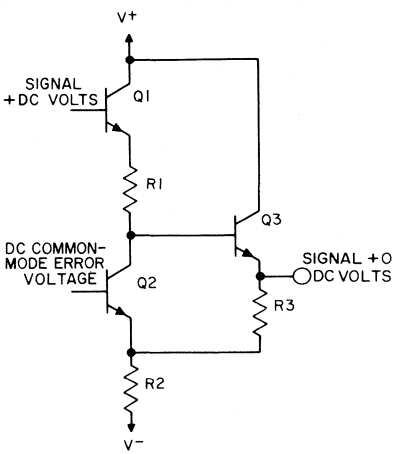


Fig. 59 — Output circuit used in linear integrated circuits to prevent a shift in dc voltage level between output and input.

Use of Forward-Biased Diodes For Level Shifting

Fig. 60 shows another simple method of level shifting. With this method, several forward-biased diodes, or a zener diode, are used in series between the collector and base of cascaded stages. Use of this simple method, however, places an unwanted series impedance in the signal path.

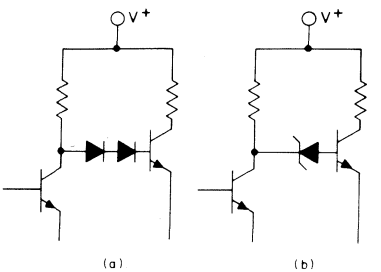


Fig. 60 — Use of (a) forward-biased diodes and (b) zener diode to provide dc level shifting.

OUTPUT STAGES

Although output stages are usually considered as "power" stages, even low-power signal amplifiers require some type of output stage to permit easy coupling, buffering, or dc level shifting.

Class A Output Circuits

Most linear integrated circuits use class A output stages. Power levels are low so that excessive power drain or dissipation is rarely a problem.

Uncommitted-Collector Types— The simplest output stage employs an uncommitted transistor collector. Several general-purpose differential-amplifier integrated circuits, such as the CA3004, CA3005, CA3006 and CA3028, use this type of output circuit. More complex multiple-stage special-purpose circuits, such as the CA3041, may also include an audio amplifier with no load impedance in the output collector. This type of output provides a high output impedance and maximum flexibility. Voltage gain of the amplifier is, of course, highly dependent upon the load. Fig. 61 shows the flexibility made possible by an uncommitted-collector type of output stage.

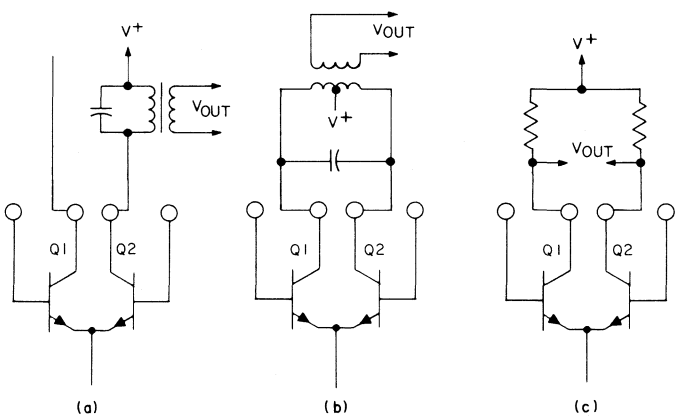


Fig. 61 — Integrated-circuit output stages with uncommitted collectors operated with (a) an external single-ended tuned load, (b) an external balanced load, and (c) an external balanced resistive load.

Use of Collector Load Resistors— Fig. 62 shows an integrated circuit that employs internal load resistors in the output stage. This approach results in less flexibility than the uncommitted-collector approach. The output resistance, however, remains high so that gain is still a function of the load on the stage.

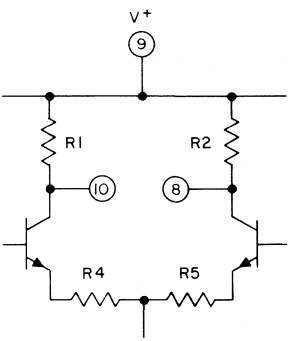
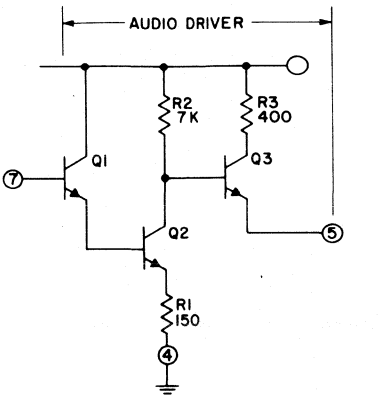


Fig. 62 — Integrated-circuit output stage that uses internal load resistors.

Emitter-Follower Output — An emitter follower is often added to the basic integrated-circuit amplifier to reduce the output impedance and, in this way, decrease the effects of loading upon gain and frequency response. The integrated-circuit audio amplifier shown in Fig. 63 illustrates this arrangement. Q1 and Q2 are used in a voltage amplifier that provides a gain of 30 dB. If transistor Q3 were not used and the output were taken from the collector of transistor Q2, the output impedance R_{out} would be 7000 ohms, and a load impedance of 70,000 ohms or more would be required to maintain a high value of gain. With transistor Q3 in the circuit, the output impedance becomes

$$R_{out} = \frac{R2}{h_{fe3}} + h_1b_3$$



All resistance values in ohms unless otherwise specified.

Fig. 63 — Emitter-follower output stage.

where h_{fe3} is the value of h_{fe} for transistor Q3 and

$$h_1b_3 = \frac{0.026}{I_{E3}} + \frac{r_{bb}'}{h_{fe3}}$$

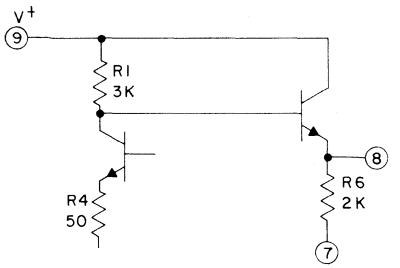
In nearly all practical cases, the base-spreading resistance r′ is much smaller than R2; the output impedance, therefore can be approximated by

$$R_{out} = \frac{R2}{h_{fe3}} + \frac{0.026}{I_{E3}}$$

The above equation illustrates that R_{out} is strongly dependent upon the operating point of the emitter follower. If a minimum h_{fe} of 30 is assumed, then R_{out} is approximately 260 ohms when I_{E3} equals 1 milliampere, but increases to 493 ohms when I_{E3} decreases to 0.1 milliampere. This type of stage must, therefore, have a dc load, and care must be used to assure that I_{E3} does not decrease below an acceptable minimum value. This requirement is particularly important when distortion

is a factor because the changing value of output resistance can contribute strongly to the distortion in the output.

In many circuits, an attempt is made to assure that I_{E3} does not decrease below a specified minimum value. For example, in the output circuit shown in Fig. 64, R6 draws a minimum current of at least 1 milliampere under most operating conditions when terminal 7 is grounded.

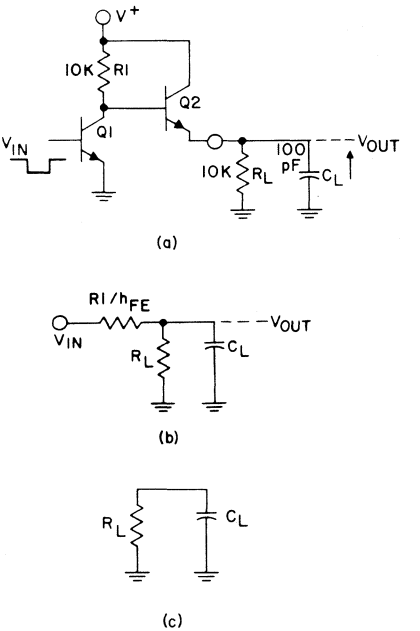


All resistance values in ohms unless otherwise specified.

Fig. 64 — Emitter-follower output stage designed to assure that current is maintained above a specified minimum value.

Augmented Emitter-Followers— The circuit shown in Fig. 64 is satisfactory for most linear low-frequency applications. However, it has limitations in high-frequency and pulse circuits. The pulse response of a circuit which includes capacitive loading is a function of the capacitance and the driving impedance. In the circuit of Fig. 65(a), the load capacitance C_L is charged by the emitter current of transistor Q2 during the negative alternation of the input signal V_{in}. The approximate circuit during the charging of C_L is shown in Fig. 65(b). The charging time constant τ_c is determined as follows:

$$\tau_c = \frac{R1R_LC_L}{R1 + h_{FE}R_L}$$



All resistance values in ohms unless otherwise specified.

Fig. 65 — Emitter-follower output circuit operated with a capacitive load: (a) over-all circuit; (b) approximate circuit during the charging of the load capacitance; (c) equivalent circuit during discharge of load capacitance.

which, for the values shown and an h_{FE} of 100, is approximately 10 nanoseconds.

During the positive alternation of V_{in}, a negative-going voltage is produced at the collector of transistor Q1 and at the base of transistor Q2. The voltage at the emitter of transistor Q2 does not change as rapidly because of the capacitor C_L. With the base of transistor Q2 negative with respect to its emitter, Q2 is cut off and the capacitor must discharge through R_L. The equivalent circuit is shown in Fig. 65(c). For the values used, the discharge time constant ($\tau_{discharge} = R_LC_L$) is

1 microsecond, or 10 times greater than the charging time constant.

Fig. 66 shows an augmented-emitter-follower type of circuit used as the output stage for most RCA integrated-circuit operational amplifiers. A modification of this circuit was discussed briefly in the section on **DC Level Shifting Circuits.** An interesting feature of the circuit is that it functions as an emitter-follower and also provides voltage gain. The basic equations for the circuit and the results obtained for the component values shown on the schematic diagram are also shown in Fig. 66. The input-impedance term r_{in} shown in Fig. 66 includes a positive component from the reflected load impedance R_L as well as a negative component. The worst-case condition for stability occurs when R_L equals −40,000 ohms. For this condition r_{in} is equal to 40,000 ohms. The source resistance R_S, therefore, must be much smaller than 40,000 ohms. In the RCA operational amplifiers that use this type of output stage, the source resistance is approximately 7500 ohms.

Class B Output Stages

A weakness of single-ended class A output stages is the difference in the time required to charge and discharge a capacitive load. A modification of the circuit shown in Fig. 65 can result in the class B circuit shown in Fig. 67, which is a much better output stage for many applications. In the modified circuit, transistors Q1 and Q3 are driven from the same source. This circuit is intended primarily for feedback amplifiers. In

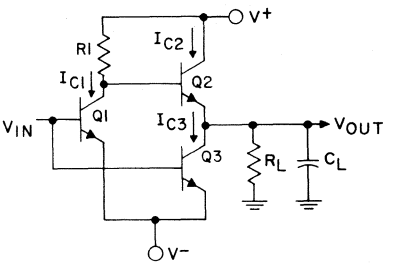
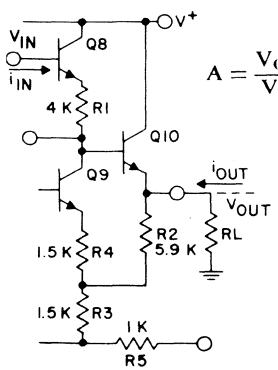


Fig. 67 — Basic class B output stage.



$$A = \frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - \frac{R1}{R2}\left(\frac{R3}{R3+R4} + \frac{1}{h_{fe}}\right) + \frac{R2R4}{R2(R3+R4)}} = 1.24$$

$$r_{OUT} = \frac{R1A_O}{h_{fe}}\left[1 + \frac{R3R4}{R2(R3+R4)}\right] = 140 \text{ ohms}$$

$$r_{IN} = \frac{\beta_1}{A}\left[\frac{1}{\frac{1}{R_L}\left(1 + \frac{R3R4}{R2(R3+R4)}\right) + \frac{1}{R2}\left(\frac{R3}{R3+R4} + \frac{1}{h_{fe}}\right)}\right]$$

Note: Refer to text for value of r_{IN}.

All resistance values in ohms unless otherwise specified.

Fig. 66 — Augmented-emitter-follower output circuit.

such an amplifier, the feedback maintains the output voltage V_{out} approximately at zero during operation with positive and negative supplies. As a result, the current flow in the load is small, and the collector currents of transistors Q1 and Q3 are approximately equal.

For the condition $V_{out} = 0$, the voltage at the base of transistor Q2 with respect to ground is very nearly equal to the base-to-emitter voltage V_{BE}. The collector current of transistor Q1, then, can be very closely approximated by the following equation:

$$I_{C1} = (V^+ - V_{BE})/R1$$

If Q1 and Q3 are matched transistors and $I_{C1} = I_{C3}$, then the quiescent current of the stage is determined by use of the equation for I_{C1} given above. When V_{in} is made more positive than its quiescent value, I_{C1} and I_{C3} increase and the voltages at both collectors decrease in accordance with the following relationships:

$$\Delta I_{C1} \approx \Delta I_{C2} \approx \Delta I$$

$$\Delta V_{C1} \approx -\Delta I(R1//h_{fe}R_L) \approx \Delta IR1$$

$$\Delta V_{C2} \approx \Delta V_{out} \approx -\Delta IR_L$$

The change in V_{BE} for Q2 is then given by

$$\Delta V_{BE2} \approx -\Delta I(R1 - R_L)$$

In most practical cases, R_1 is much greater than R_2 so that V_{BE2} decreases rapidly, and Q2 is cut off.

When V_{in} changes in a negative direction, I_{C1} and I_{C3} decrease, and V_{C1} increases more rapidly than the output voltage would increase because of the action of transistor Q3. The voltage V_{BE2} therefore increases, and the output follows the collector voltage of transistor Q1. The output follows Q3 for positive-going inputs and follows Q1 for negative-going inputs. This relationship suggests the two equivalent circuits shown in Fig. 68.

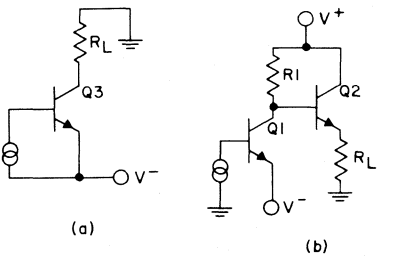
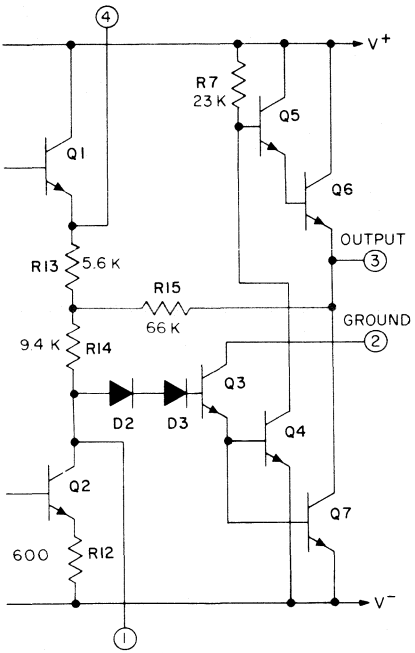


Fig. 68 — Equivalent circuits of output stage shown in Fig. 67: (a) for positive alternations of an input signal; (b) for negative alternations of an input signal.

The voltage gain for the circuit shown in Fig. 68(b) is greater than that of the circuit shown in Fig. 68(a) by nearly the ratio R1/RL so that feedback must be used to reduce the resulting distortion. This principle is employed in the output stage shown in Fig. 69. In this circuit, transistors Q4, Q6, and Q7 serve the same functions as transistors Q1, Q2, and Q3, respectively, in Fig. 67. Transistor Q5 is added to increase the effective h_{fe} of Q6. Resistors R13 and R15 form a local feedback network to reduce amplifier distortion.

A major advantage of the class B output stage shown in Fig. 69 for monolithic construction is that it uses only n-p-n transistors. In this circuit, however, the gain and output impedance are asymmetric, and the crossover distortion is substantial. These disadvantages can be overcome by use of complementary-symmetry output stages. Use of complementary output stages in inte-



All resistance values in ohms unless otherwise specified.

Fig. 69 — Class B output stage that used feedback to assure equal positive and negative swings in the output voltage.

grated circuits is becoming more practical and increasingly desirable as the ability to produce good monolithic p-n-p transistors improves.

Fig. 70 shows a basic complementary-symmetry output stage. Diodes

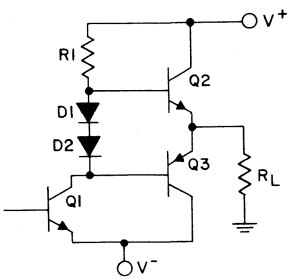


Fig. 70 — Basic complementary-symmetry output stage.

D1 and D2 are selected so that the desired value of quiescent current flows through transistors Q2 and Q3. When I_C is increased, the voltage at the bases of transistors Q2 and Q3 becomes more negative and the p-n-p transistor Q3 conducts. Similarly, the n-p-n transistor Q2 conducts when I_{C1} decreases. This circuit, therefore, is a class B push-pull amplifier. The collector of the p-n-p transistor is connected to the negative supply. Because the substrate of the integrated circuit is also connected at this point, Q3 may be constructed as a "vertical" or "substrate" p-n-p transistor, as previously described in the section on **Effects of Monolithic Fabrication on Circuit Design.** Present technology provides substrate p-n-p transistors that have h_{fe} ratios greater than 30 so that the complementary-symmetry type of output circuit is now practical. Some refinements of the basic complementary-symmetry circuit configuration, however, are required. The resultant circuit obtained is shown in Fig. 71.

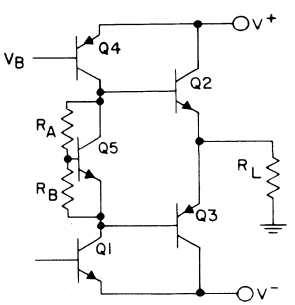


Fig. 71 — Improved version of the basic complementary-symmetry output stage shown in Fig. 70.

The resistor R1 in the basic circuit is replaced by a p-n-p transistor Q4 in the modified circuit. This modification results in the following advantages:

1. Higher gain can be obtained because the output resistance of the transistor can be many times the value of the resistor.

2. A greater output-voltage swing can be achieved. In the basic complementary-symmetry circuit shown in Fig. 70, the output-voltage swing is limited by the value of resistor R1, as shown by the following equation:

$$V_{out}(max) = (V^+ - V_{BE})\frac{R_L}{R_L + R1/h_{fe}}$$

An increase in the value of R1 to obtain higher gain results in a decrease in the output-voltage swing. With the transistor load, the maximum output-voltage swing becomes

$$V_{out}(max) = V^+ - V_{BE} - V_{sat}$$

3. Diodes D1 and D2 of the basic circuit are replaced by transistor Q5 and resistors R_A and R_B. The transistor-resistor network provides better control of idling current.

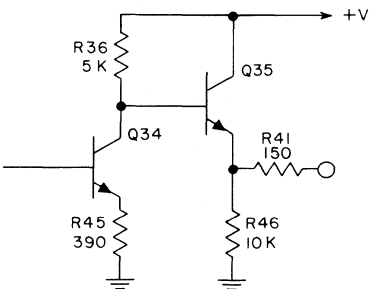
Output-Stage Protection Circuitry

The basic output stages shown in Figs. 61 and 62 require no protection; when an emitter-follower is added, however, the potential for damage to the integrated circuit from shorted outputs becomes high. When terminal 8 of the output stage shown in Fig. 64 is shorted to ground, the maximum current that can flow in this circuit is given by

$$I_{max} = \left(\frac{V^+ - V_{BE}}{R1}\right)h_{fe}$$

If $V^+ = -V^- = 6$ volts and h_{fe} is high, the magnitude of this current may be in the range of 50 to 100 milliamperes.

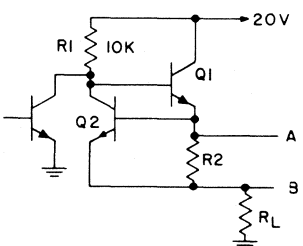
A simple way to limit the current is to add a resistance in the collector, as shown in Fig. 63, or in the emitter of the output transistor. The current in this circuit is limited to 30 milliamperes. The addition of the resistor in the collector does not affect the output resistance, but merely limits the dynamic range. When a resistor is placed in series with the output terminal, as shown in Fig. 72, the output impedance is increased.



All resistance values in ohms unless otherwise specified.

Fig. 72 — Emitter-follower output stage with a resistor connected in series with the output terminal.

Fig. 73 shows a circuit in which the effects of the protection circuit are minimized until the protection is needed. In the basic circuit, point "A" is the output, and resistor R2 and transistor Q2 are not included. The resistor and transistor comprise the protection circuit. Resistor R2 is selected so that, for normal loads,



All resistance values in ohms unless otherwise specified.

Fig. 73 — Output stage with overload protection circuitry.

the voltage across the base-emitter junction of transistor Q2 is less than 500 millivolts. For this condition, I_{C2} is less than 0.5 microampere so that little current is removed from the available drive for transistor Q1. The current I_{C2} must be increased to more than 2 milliamperes to increase the base-to-emitter voltage of transistor Q2 to 750 millivolts. In the circuit shown, the maximum current available in R1 is only 2 milliamperes so that this condition can only be met if the h_{fe} is very high. If the value of R2 is only 25 ohms, the current is limited to 30 milliamperes, as in the case of the circuit shown in Fig. 63, and the effect of this circuit on dynamic range and output impedance is much less than before. Another advantage of the circuit shown in Fig. 73 is that limiting occurs at lower currents as the temperature of the integrated-circuit chip rises. For a junction temperature of 1250°C, the threshold of the circuit is nearly 200 millivolts less than that at 250°C. The maximum current, therefore, is only two-thirds of the value allowed at the lower temperature. In addition, if R2 is on the chip, it has a positive temperature coefficient so that its value is 20 per cent higher, and the current is then reduced to nearly half of the room-temperature value. Many variatons of the circuit are used. It should also be realized that the nonlinearity of the emitter-base diode junction can easily be used to protect other devices.

POWER-SUPPLY AND VOLTAGE-REFERENCE CIRCUITS

Multistage linear integrated circuits usually include internal power-supply and voltage-reference elements that substantially increase the complexity of the over-all circuit. The additional complexity added by such elements, which seemingly have no bearing on the signal-processing capability, would be unwarranted in equivalent discrete-component circuits. These elements, however, are essential in monolithic circuits that include a cascade of several direct-coupled amplifiers to provide supply- and bias-voltage decoupling and to assure stable bias voltages.

Basic amplifier design principles demand that the individual stages of a multistage amplifier be decoupled from the dc supply-voltage line. Separate decoupling of the bias networks may also be required. In conventional discrete-component amplifiers, this decoupling may be provided by use of simple resistance-capacitance networks. Fig. 74 illustrates the use of resistance-capacitance networks to provide supply-voltage decoupling for a three-stage discrete-component amplifier.

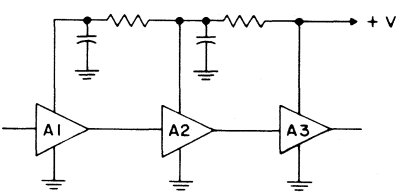


Fig. 74 — Block diagrams showing supply decoupling requirements for a direct-coupled three-stage discrete-component amplifier.

The values of the bypass capacitors required for supply- or bias-voltage decoupling are much larger than can possibly be provided on an integrated-circuit chip. The bypass capacitors, therefore, would have to be external to the integrated-circuit chip, and additional circuit terminals would be required to interconnect such components to

the integrated circuit. For example, an integrated-circuit design of the three-stage amplifier shown in Fig. 74 would require two additional circuit terminals for use in bypassing the supply-voltage line. Restrictions on the maximum number of circuit terminals, however, is generally a major limiting factor in integrated-circuit design, and use of two additional terminals merely for supply-voltage decoupling would be highly extravagant. Much of the complexity added to an integrated circuit by internal power-supply elements results from the need to provide decoupling between individual stages or between input and output and is justified by a reduction in the number of circuit terminals that would otherwise be required.

Direct coupling is nearly always required to provide signal interconnections between cascaded stages in a monolithic integrated circuit. In contrast, the stages of a discrete-component amplifier, such as that shown in Fig. 74, may be interconnected by direct coupling, or other conventional methods. Direct coupling is used only when this method results in a decided economic or performance advantage.

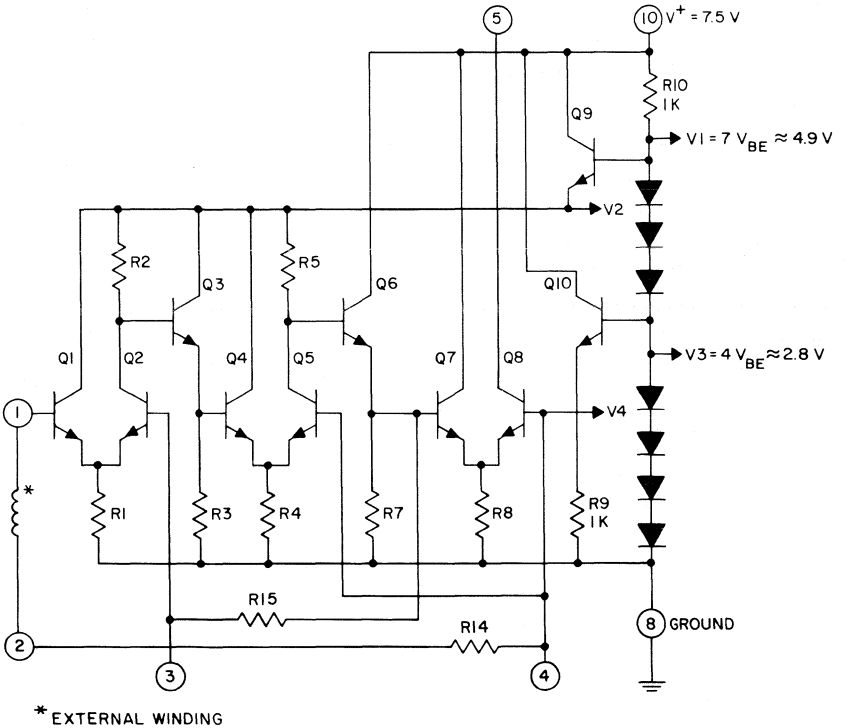
The requirement for direct coupling is another factor that makes it necessary to include power-supply and voltage-reference elements in multistage integrated circuits. With this coupling method, stable and reproducible bias voltages are essential for each stage. The following paragraphs explain the use of different types of circuit elements to assure that this requirement is met and to assure adequate supply- and bias-voltage decoupling.

Diode-String Regulators

Fig. 75 shows the use of a series string of emitter-base diode junctions as basic voltage-reference elements and of emitter-followers to decouple the collectors and bias points of the amplifiers. The repeatability of the value of the voltage across a base-emitter junction at a given current is nearly 15 per cent, and such voltages can be matched to within 1 per cent. Moreover, for a bias current of 1 milliampere, the voltage across a typical integrated-circuit diode changes less than 1 per cent for a change in current of ±30 per cent.

In the circuit shown in Fig. 75, a string of seven diodes establishes the circuit operating voltages for a dc supply voltage of +7.5 volts. The current in the string is 2.5 milliamperes, and the voltages at various points are as indicated on the circuit diagram. If the supply voltage V+ is increased to 9 volts, the current increases to approximately 4 milliamperes, and the voltages V_1 and V_2 increase to only 5.1 volts and 2.92 volts, respectively. This small changes does not measurably affect circuit performance. The diode string, therefore, provides a good stable reference voltage.

The emitter-follower Q9 couples the collectors of the transistors in the first and second amplifiers to the reference string and also provides isolation of the voltage-reference circuit from the loading of the amplifier and from changes in ac signals. This isolation is important because the ac impedance of the diode string is nearly 15 ohms per diode at 2.5 milliamperes, or approximately 100 ohms at point V_1. If the h_{fe} of transistor Q9 is 30 or greater, the ripple currents at the emitter of Q9 are reduced 30 times so that the ripple voltage at V_1 is proportional to 100/30.



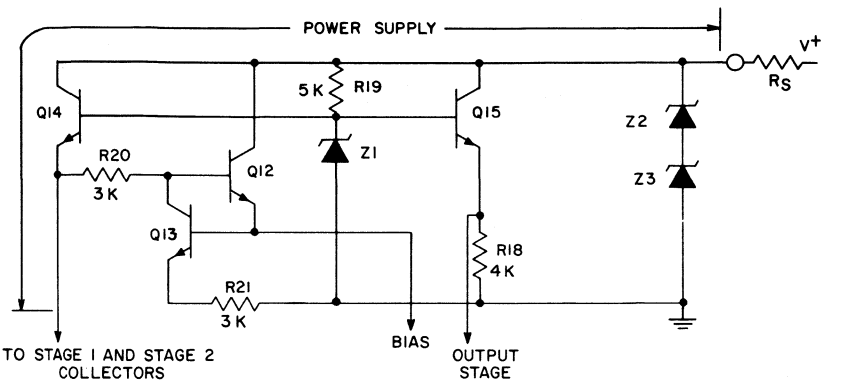
All resistance values in ohms unless otherwise specified.

Fig. 75 — Multistage circuit that uses diode-string bias regulation.

Zener-Diode Regulators

Zener-diode regulators can be used to obtain improved performance over the simple diode-string type described in the preceding paragraph. As discussed previously, the emitter-base junction of a normal monolithic transistor operated in the breakdown region can be used as a zener diode. This device, however, has a series impedance of 60 to 100 ohms over much of the current range. Improved zener diodes are achieved by addition of a p^+-type diffusion to the standard emitter-base junction. This technique results in isolated zener diodes that have series impedances of only 5 to 10 ohms and lower temperature coefficients than conventional emitter-base junctions. The conventional emitter-base zener diodes have a zener voltage of approximately 7 volts and a temperature coefficient of approximately 3 millivolts per °C. The improved zener diodes have a zener voltage of approximately 5.6 volts and a temperature coefficient of approximately 1.2 to 2 millivolts per °C.

Fig. 76 shows the use of the improved zener diodes in an internal power supply of an integrated circuit. In this circuit, zener diodes Z2 and Z3 form a primary regulator. DC power is supplied from the ex-



All resistance values in ohms unless otherwise specified.

Fig. 76 — Integrated power supply that uses zener-diode voltage regulation.

ternal equipment in which the circuit is used, and Z2 and Z3 serve to stabilize the voltages on the integrated-circuit chip and to filter ripple from the power-supply line. Although a zener diode is not normally considered as a filter, the impedance provided by Z2 and Z3 is nearly equivalent to that provided by a 50-microfarad capacitor at 120 Hz. Zener diode Z1 is the reference for an if amplifier in the integrated circuit. This device has a nominal voltage drop of 5.6 volts so that voltages of approximately 4.9 volts are applied to the collectors of the signal-processing transistors.

The remaining components (R20, R21, Q12, and Q13) form an interesting circuit which applies one half of the emitter voltage of Q14 to the bias network of the chip and simultaneously presents a very low output impedance. For convenience, this portion of the power-supply circuit is shown separately in Fig. 77. If h_{fe} is high (50 or greater), then $I_{C12} \approx I_{C13}$, and $I_{E13} \approx I_{C13} \approx I$. The voltages across R20 and R21, therefore, are very nearly equal. In addition, as shown previously, even if I_{C12} does not equal I_{C13}, V_{BE12} nearly equals V_{BE13}. Therefore, the voltage between points "A" and "C" is equal to the voltage between points "C"

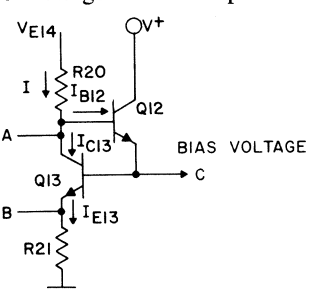


Fig. 77 — Bias-voltage circuit included in the power supply shown in Fig. 76.

and "B", and point "C" is halfway between V_{E14} and ground. The output impedance may be approximated as follows:

$$r_{out} \approx \frac{1}{g_{m2}\left(\frac{R20}{\frac{26}{I_{C13}} + R21} + 1\right)}$$

$$\approx \frac{1}{g_{m2}\left(\frac{R20}{R21} + 1\right)} \approx \frac{1}{2g_{m2}}$$

The output impedance of the circuit, therefore, is approximately one-half the output impedance of a simple emitter follower.

Precision Voltage Reference

The voltage-reference sources discussed in the preceding sections are adequate for most application. Some circuit applications, however, require a precision voltage source that does not change with temperature. Fig. 78 shows the voltage-reference circuit used in the RCA-CA3055 integrated-circuit voltage regulator. This

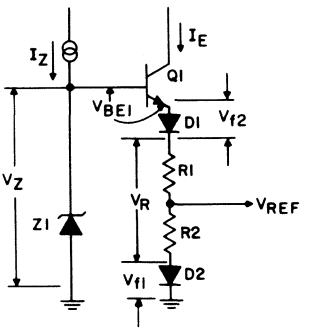


Fig. 78 — Precision voltage-reference circuit.

voltage-reference circuit, which provides a voltage source that has a zero temperature coefficient, illustrates how variations in the characteristics of transistors, diodes, and resistors may be balanced against one another to achieve stable, reproducible voltages.

If the terminology used in Fig. 78 is employed, the output reference voltage V_{REF} may be expressed as follows:

$$V_{REF} = V_f + R2I_E$$

where

$$I_E = V_R/(R1 + R2)$$

and

$$V_R = V_Z - V_{BE1} - V_{f1} - V_{f2}$$
$$= V_Z - 3V_f$$

The voltage-reference circuit is designed so that the emitter current I_E remains constant with changes in temperature. For this condition, component values for the circuit must be chosen so that the following relationship is satisfied:

$$\frac{dI_E}{dT} =$$

$$\frac{(R1 + R2)\frac{dV_R}{dT} - V_R\frac{d(R1 + R2)}{dT}}{(R1 + R2)^2} = 0$$

Therefore,

$$(R1 + R2)\frac{dV_R}{dT} = V_R\frac{d(R1 + R2)}{dT}$$

or

$$\frac{dV_R/dT}{V_R} = \frac{d(R1 + R2)/dT}{R1 + R2}$$

As pointed out previously, integrated-circuit resistors have a temperature coefficient of +0.2 per cent per °C. The circuit must be designed, therefore, so that the following condition is established:

$$\frac{dV_R/dT}{V_R} = +0.2\%/°C$$

The values of the voltages V_Z and V_f and the temperature coefficients of the zener diode and the emitter-base diode junctions are functions of current. Analysis of the voltage-current characteristics of these elements shows that, for $I_Z = I_E =$ 0.565 milliampere, the voltage V_Z is 5.2 volts and the voltage V_f is 0.7 volt. The zener diode has a tempera-

ture coefficient of +1.1 millivolts per °C. The following calculation shows that, for these values, the circuit is balanced (a change in temperature of 1°C is assumed):

$$\frac{\Delta V_R}{V_R} = \frac{\Delta V_Z - 3\Delta V_f}{V_Z - 3V_f}$$

$$= \frac{1.1 - 3(-1.7)\text{mV}}{5.2 - 3(0.7)}$$

$$= \frac{6.3 \times 10^{-3}}{3.1} = 0.203\%/°\text{C}$$

For the required current I_E of 0.565 milliampere, the total value of the resistors R1 and R2 is calculated to be

$$R1 + R2 = \frac{3.1 \text{ volt}}{0.565 \text{ mA}} = 5500 \text{ ohms}$$

The values of resistors R1 and R2 can then be determined individually.

Because I_E is constant with temperature, the first derivative of the equation for the output reference voltage V_{REF} can be written as follows:

$$\frac{dV_{REF}}{dT} = \frac{dV_f}{dT} + I_E\left(\frac{dR2}{dt}\right)$$

For a zero temperature coefficient,

$$\frac{dV}{dT}V_{REF} = 0$$

and

$$I_E\frac{dR2}{dT} = -\frac{dV_f}{dT}$$

For a change in temperature of 1 per cent,

$$0.585 \times 10^{-3} \times 0.002R2 = 1.6 \times 10^{-3}$$

$$R2 = 1.495 \times 10^3 \approx 1500 \text{ ohms}$$

and R1 is equal to 4000 ohms.

Differential-Amplifier Circuits

The RCA family of differential-amplifier integrated circuits includes a broad variety of general-purpose devices in which the basic signal-processing function is accomplished primarily by a single differential-amplifier stage. This family of devices represents the simplest level of complete circuit fabricated by monolithic techniques. (Although an integrated-circuit array may be simpler, this type of device consists basically of a collection of independent matched components and does not constitute a complete circuit.)

Table V lists the circuits included in the RCA differential-amplifier product line and points out some of the distinguishing features and the major applications of each type. Each circuit in the differential-amplifier product category consists basically of an emitter-coupled pair of transistors and a transistor constant-current-source network. A variety of additional components are then added to the separate circuits to provide a wide selection of "black-box" characteristics in relation to performance factors such as gain, bandwidth, input and output impedance, dynamic range, and flexibility of application. Because of the exceptional versatility of the differential-amplifier circuits, a single descriptive name cannot completely categorize any one of them. The descriptive names assigned to these circuits, therefore, are merely generic designations provided for convenience of identification and are not indicative of the large variety of circuit functions for which they may be used.

GENERAL CIRCUIT CHARACTERISTICS

All the differential-amplifier circuits have inverting and non-inverting inputs and, therefore, exhibit excellent common-mode-rejection ratios CMRR. Some of the differential-amplifier circuits have double-ended outputs for balanced operation, and others have single-ended outputs. Several circuits have uncommitted collectors so that they may be terminated by external inductive or resistive loads appropriate for the application. All the differential-amplifier circuits include bias resistors to set the constant-source current, and most of them have temperature-compensating diodes in the constant-current-source bias network.

The simplest of the differential-amplifier circuits then consists of the differential-amplifier pair of transistors, a constant-current-source tran-

Table V — *RCA Differential-Amplifier Integrated Circuits*

Type No. and Name	Package	Significant Features	Applications
CA3000 DC Amplifier	10-terminal TO-5-style	Emitter-follower input for high input impedance; emitter degeneration for wider dynamic range; frequency range: dc to 30 MHz (with external resistors and capacitors)	DC amplifier, crystal oscillator, Schmitt trigger, sense amplifier, mixer, comparator, modulator, RC-coupled feedback amplifier
CA3001 Video and Wide-Band Amplifier	12-terminal TO-5-style	Emitter-follower (high-impedance) input and emitter-follower (low-impedance) output; small-value collector load resistors for wide bandwidth (29 MHz at 3-dB-down points)	DC, if, and video amplifiers; Schmitt trigger; mixer; and modulator
CA3002 IF Amplifier	10-terminal TO-5-style	Emitter-follower input and output; frequency range: dc to 15 MHz	IF and video amplifiers, AM detector, product detector, and Schmitt trigger
CA3004 RF Amplifier	12-terminal TO-5-style	Emitter degeneration for increased linearity; uncommitted collectors for increased applications flexibility; frequency range: dc to 100 MHz	RF, if, and video amplifiers; modulator; detector; agc; and limiter
CA3005 Diff./Cascode RF Amplifier	12-terminal TO-5-style	Uncommitted collectors and additional bias components and terminal connections for increased applications flexibility; operation in either differential-amplifier or cascode configuration; frequency range: dc to 100 MHz	Wide- and narrow-band amplifiers, converter and multiplier service, detector, limiter, and modulator
CA3006 Diff./Cascode RF Amplifier	12-terminal TO-5-style	Very small offset voltage (1 millivolt maximum); otherwise, same as CA3005	Same as CA3005
CA3028A Diff./Cascode Amplifier	8-terminal TO-5-style	Single- or dual-ended operation to 120 MHz; operation in either differential-amplifier or cascode configuration	RF-amplifier, mixer, oscillator, and agc service; limiter; converter; dc, audio, and sense amplifiers
CA3028B Diff./Cascode RF Amplifier	8-terminal TO-5-style	Operation at supply voltages up to ±15 volts; specially controlled input characteristics; otherwise same as CA3028A	Same as CA3028A; particularly advantageous for critical dc and differential-amplifier applications
CA3049* Dual Independent Differential RF/IF Amplifier	12-terminal TO-5-style	Independently accessible inputs and outputs for increased application flexibility; operation to 500 MHz	Dual independent differential rf/if amplifier, balanced quadrature detector, doubly-balanced modulator and demodulator, dual Schmitt trigger, and product and synchro detector

Table V — *RCA Differential-Amplifier Integrated Circuits (Cont.)*

Type No. and Name	Package	Significant Features	Applications
CA3050* Dual Differential Darlington-Connected Amplifiers	14-terminal dual-in-line ceramic	Dual independent differential Darlington-connected amplifiers for high input impedance; diode bias string for temperature compensation	Matched dual differential amplifier, balanced quadrature detector, doubly-balanced detector and modulator, dual multivibrator, and dual Schmitt trigger
CA3051* Dual Differential Darlington-Connected Amplifier	14-terminal dual-in-line plastic	Same as CA3050	Same as CA3050
CA3053 Diff./Cascode Amplifier	8-terminal TO-5-style	Single- or dual-ended operation to 10.7 MHz; operation in either differential-amplifier or cascode configuration	Same as CA3028A up to a frequency of 10.7 MHz.

* The CA3049, CA3050, and CA3051 are described in the section on **Arrays.**

sistor and bias resistors for the constant-current-source, as shown in Fig. 79(a). In more sophisticated types, diodes are added to the constant-current-source bias circuit, and emitter resistors may be included to increase the range of linearity of the transconductance, as shown in Fig. 79(b).

The differential-amplifier integrated circuits can be further refined by (1) addition of diffused collector load resistors which track the current-setting resistor on the chip and thus maintain a relatively constant voltage gain, (2) use of emitter-follower transistors at the input to provide high input impedance, and

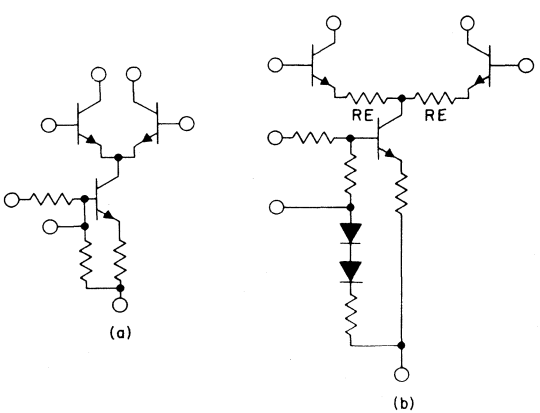


Fig.79 — Integrated-circuit differential-amplifier configurations: (a) basic circuit; (b) circuit in which emitter degeneration is used and temperature-compensating diodes are included in the constant-current bias network.

(3) use of emitter-follower transistors at the outputs to provide low output impedance. Three different values of internal collector resistors are available from circuits in the differential-amplifier product line that include these elements, so that a different combination of gain and bandwidth can be provided by different circuits. Larger collector resistance results in higher voltage gain and smaller bandwidth.

Each differential-amplifier circuit may be operated from dual dc supplies or from a single dc supply. When a single supply is used, however, an additional resistor divider and bypass capacitor are required. Fig. 80 shows bias arrangements for both dual- and single-supply operation of a differential-amplifier integrated circuit.

DC AMPLIFIER

Fig. 81 shows the schematic diagram of the CA3000 integrated-circuit dc amplifier. This stabilized and compensated differential amplifier provides push-pull outputs, high-impedance (0.1-megohm) inputs, and gain of approximately 30 dB at frequencies up to 1 MHz. Its useful frequency response can be increased to several tens of megahertz by the use of external resistors or coils.

The circuit, which is supplied in a 10-terminal TO-5-style package, is basically a single-stage differential amplifier (Q2 and Q4) with input emitter-followers (Q1 and Q5) and a constant-current source (Q3) in the emitter-coupled leg. Push-pull input and output capabilities are inherent in the differential configuration.

The use of degenerative resistors R4 and R5 in the emitter-coupled pair of transistors increases the linearity of the circuit. The low-frequency output impedance between each output (terminals 8 and 10) and ground is essentially the value of the collector resistors R1 and R2 in the differential stage.

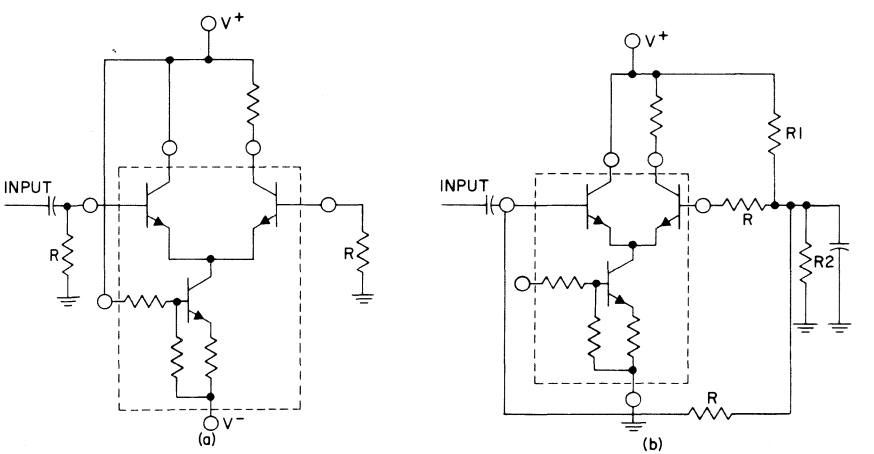
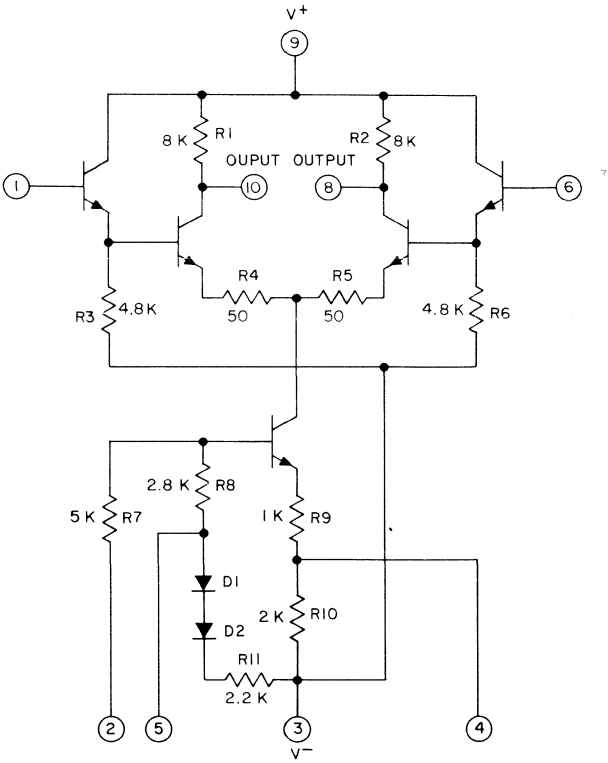


Fig. 80 — Supply-voltage connections for integrated-circuit differential amplifiers: (a) dual-supply operation; (b) single-supply operation.



All resistance values in ohms unless otherwise specified.

Fig. 81 — CA3000 integrated-circuit dc amplifier.

Operating Requirements and Characteristics

The CA3000 is designed for operation from a wide range of supply voltages. Operation from either one or two power supplies is feasible; however, operation from two supplies is recommended because fewer external bias components are required and, therefore, less power is consumed.

The maximum voltage that can be applied across the circuit (positive supply voltage V^+ plus negative supply voltage V^-) is 16 volts. The maximum voltage capability (V_{CE}) of the differential-pair transistors is 8 volts. Extra care must be used to ensure that these values are not exceeded when the circuit is used to drive inductive loads.

The operating-current conditions of the differential pair of transistors are determined by the base-bias circuit and emitter-resistance of the emitter-coupled constant-current-source transistor (Q3), as well as by the voltage between terminals 2 and 3. Each possible current condition is manifested by (1) a distinct set of dc operating characteristics with differing temperature characteristics, (2) a particular value of gain having its own temperature

Table VI — *Operating Modes for CA3000 DC Amplifier*

Mode	Shorted Terminals	Condition of Diodes	Q3 Emitter Resistor
A	none	in	R9 + R10
B	5-3	out	R9 + R10
C	4-3	in	R9
D	5-4-3	out	R9

dependence, and (3) a particular dynamic output-voltage capability. For each value of voltage between terminals 2 and 3 (V^- when terminal 2 is grounded), there are four possible operating modes, as described in Table VI.

The operating characteristics for these modes of operation are summarized in Table VII for various two-supply configurations with terminal 2 grounded and with V^- values of −3 and −6 volts dc.

Table VII shows that the positive supply voltage can be adjusted for each mode of operation and for each value of negative supply so that the nominal dc output voltage is zero. (Although the V^+ value required for mode C for a V^- of −6 volts dc is in excess of the maximum rating, operation within ratings can be achieved with slightly negative values of output voltage.) The use of these adjusted values of positive supply provides two advantages: (1) direct interstage coupling can be effected in a single-ended configuration, and (2) negative feedback can be introduced from a single output back to the appropriate input. For low-level applications in mode D with a negative supply voltage V^- of −3 volts dc and a posi-

Table VII — *Design Characteristics of CA3000 Operating Modes*

DC Supply Volts Positive V+	DC Supply Volts Negative V⁻	Operating Mode	Single-ended Mid-Band Voltage Gain — dB G_{V_S}	DC Output Volts (Term. 8 or 10 to ground) $V_{o_{dc}}$	Positive Voltage Swing $V_{o_{max}}$*	Negative Voltage Swing $V_{o_{min}}$*	Total Power Dissipation — mW
6	−6	A	31.2	+2.3	+3.7	−3.8	40
6	−6	B	27.3	+4.3	+1.7	−5.7	36
6	−6	C	34.6	−1.5■	+7.5	0	61
6	−6	D	32.4	+1.0	+5.0	−2.4	47
3.7	−6	A	31.2	0	+3.7	−1.4	33
1.7	−6	B	27.3	0	+1.7	−1.4	25
10.6▲	−6	C	34.6	0	+10.6	−1.5	83
5.0	−6	D	32.4	0	+5.0	−1.5	43
3	−3	A	27.5	+1.2	+1.8	−2.6	8.8
3	−3	B	16.6	+2.6	+0.4	−4.1	7.4
3	−3	C	32.6	−1.5■	+4.5	0	14
3	−3	D	24.4	+1.9	+1.1	−3.3	8.5
1.8	−3	A	27.5	0	+1.8	−1.5	7.2
0.4	−3	B	16.6	0	+0.4	−1.5	8.4
5.3	−3	C	32.6	0	+5.3	−1.5	19
1.1	−3	D	24.4	0	+1.1	−2.6	6.2

* $V_{o_{max}}$ and $V_{o_{min}}$ are the ac swing extremities above and below $V_{o_{dc}}$.
▲ Over rating. ■ Saturated.

tive supply voltage V^+ of 1.1 volts dc, the CA3000 has a gain of 24.4 dB, a dissipation of 6.2 milliwatts, an output capability of 2.2 volts peak-to-peak, and a dc output-voltage reference level of zero.

The information in Table VII can be modified for single-supply designs by simple addition and/or subtraction of dc values. For example, the correct information for a single supply of 12 volts dc for operating mode A can be obtained from the conditions shown in the table for mode A for $V^+ = 6$ volts, and $V^- = -6$ volts by the addition of 6 volts to the values shown for V^+, V^-, Vo_{dc}, Vo_{max}, and Vo_{min}. (It should be noted that the required voltage levels at the input terminals 1 and 6 and at terminal 2 are also 6 volts higher.)

As mentioned previously, the four operating modes exhibit different temperature characteristics. Fig. 82 shows theoretical curves of dc output voltage as a function of temperature for each operating mode for a negative supply voltage V^- of −6 volts dc.

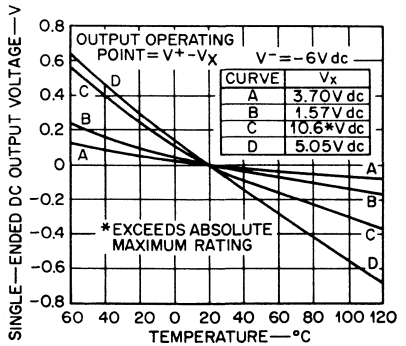


Fig. 82 — Theoretical curves of dc output voltage as a function of temperature (calculated for $\beta = 35$ at 20°C).

Fig. 83 shows theoretical curves of gain as a function of temperature for the four operating modes with V^- values of −3 and −6 volts dc.

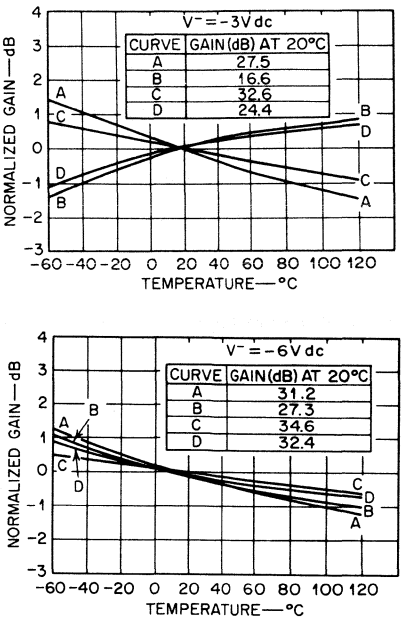


Fig. 83 — Theoretical curves of gain as a function of temperature for negative-supply voltages of −3 and −6 volts (calculated for $\beta = 35$ at 20°C).

With the diodes in (modes A and C), the gain decreases for both values of V^-. With the diodes out (modes B and D), on the other hand, the gain increases with temperature for a negative supply of −3 volts dc, but decreases with temperature for a negative supply of −6 volts dc. With the diodes out, there is a value of negative supply (approximately −4.5 volts dc) for which the gain is independent of temperature. Fig. 84 shows measured values of single-ended and push-pull gain for mode A with symmetrical power supplies of ±6 volts dc. (This configuration is used in the remaining discussion because it provides the maximum sinusoidal output capability, as shown in Table VII, and because of the convenience of ±6-volt dc supplies.)

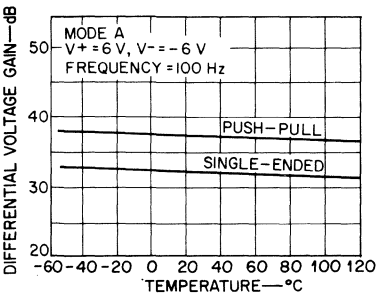


Fig. 84 — Measured values of single-ended and push-pull gain for mode A operation.

The typical single-ended voltage-gain/frequency-response curve of the CA3000 for dc supplies of ±6 volts in operating mode A is shown in Fig. 85. The responses of the CA3000 are virtually independent

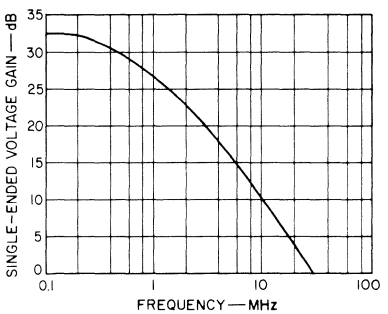


Fig. 85 — Single-ended voltage gain of the CA3000 as a function of frequency.

of source impedance up to 10,000 ohms because of the emitter-follower inputs. The curves in Fig. 86 show that gain and bandwidth are virtually independent of temperature for operation in mode A with ±6-volt dc supplies.

Fig. 87 shows agc characteristics for the CA3000 for an input frequency of 1 kHz. When the agc voltage at terminal 2 is varied from 0 to −6 volts, the amplifier gain can be varied over a range of 90 dB.

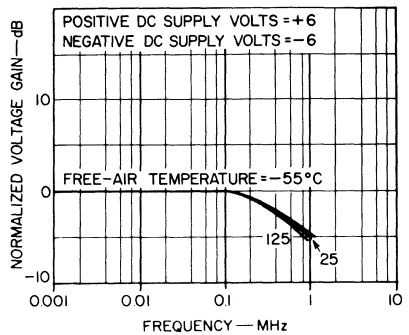


Fig. 86 — Normalized gain-frequency curves for the CA3000 at three different temperatures.

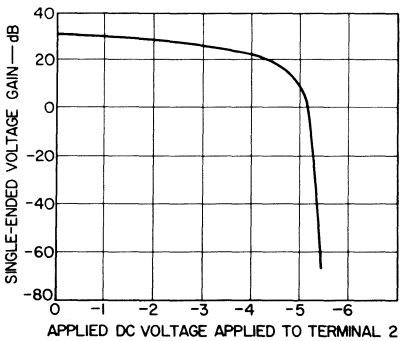


Fig. 87 — AGC characteristics of the CA3000 at a frequency of 1 kHz.

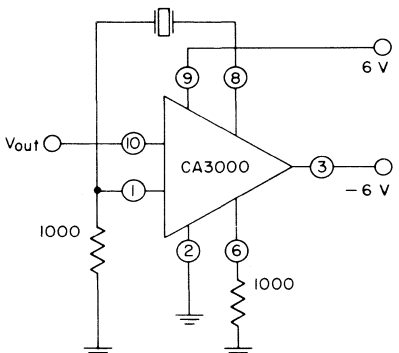
Applications of the DC Amplifier

The full gain-control capability inherent in the CA3000 makes possible the use of this circuit as a signal switch (with pedestal), a squelchable audio amplifier (with suppressed switching transient), a modulator, a mixer, or a product detector. When suitable external components are added, it can also be used as an oscillator, a one-shot multivibrator, or a trigger with controllable hysteresis. Within its specified frequency range, it is an excellent limiter and can handle input signals up to about 80 millivolts rms before significant

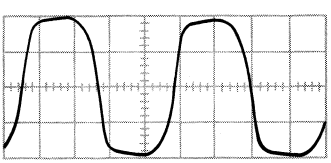
cross-modulation or intermodulation products are generated. Some of the applications of the CA3000 are discussed below.

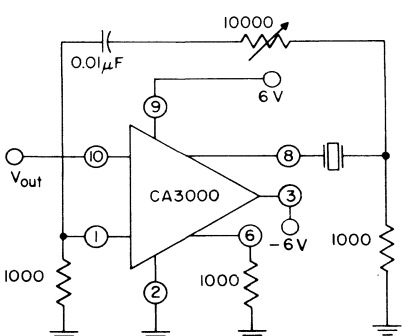
Crystal Oscillator—The CA3000 can be used as a crystal oscillator at frequencies up to 1 MHz by connection of a crystal between terminals 8 and 1 and use of two external resistors, as shown in Fig. 88(a). The output is taken from the collector that is not connected to the crystal (in this case, terminal 10). If a variable-feedback-ratio network is used, as shown in Fig. 88(b), the feedback may be adjusted to provide a sinusoidal oscillation. Output waveforms for both circuits are also shown. The frequency in each circuit is 455 kHz, as determined by the crystal. The range of these crystal oscillators can be extended to frequencies of 10 MHz or more by use of collector tuning.

Modulated Oscillator—If a low-frequency signal is connected to terminal 2, as shown in Fig. 89, the CA3000 can function as an oscillator and produce an amplitude-modulated signal. The waveform in Fig. 89 shows the modulated signal output produced by the modulated os-

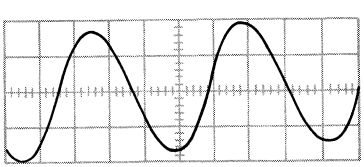


(a)



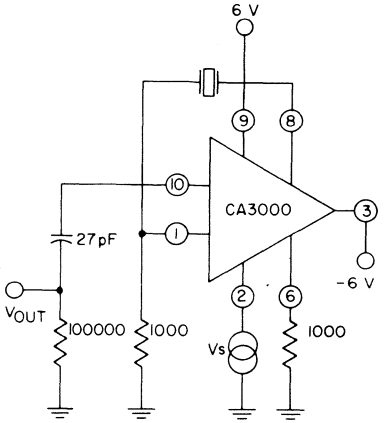


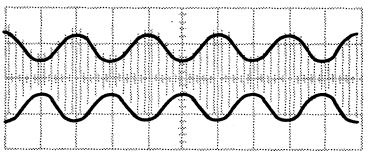
(b)



All resistance values in ohms unless otherwise specified.

Fig. 88 — Circuit diagrams and output waveforms of (a) a basic crystal oscillator and (b) a crystal oscillator with variable feedback.





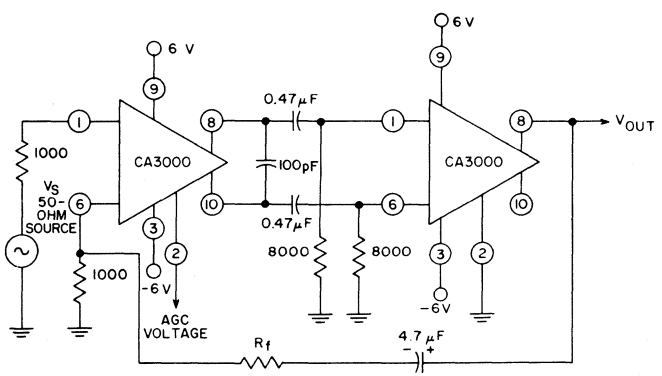
All resistance values in ohms unless otherwise specified.

Fig. 89 — Circuit diagram and output waveform of a CA3000 modulated oscillator.

cillator circuit when a 1-kHz signal is introduced at terminal 2 and a high-pass filter is used at the output.

Low-Frequency Mixer—In a configuration similar to that used in modulated-oscillator applications, the CA3000 amplifier may be used as a mixer by connection of a carrier signal at the base input of either differential-pair transistor (terminal 1 or 6) and connection of a modulating signal to terminal 2 or 5.

Cascaded RC-Coupled Feedback Amplifier—The two-stage feedback cascade amplifier shown in Fig. 90 produces a typical open-loop midband gain of 63 dB. This circuit uses a 100-picofarad capacitor C1 to shunt the differential outputs of the first stage. This capacitor staggers



FOR $V_{AGC} = 0$

R_f	G_V
∞	63 db (OPEN LOOP)
100000 OHMS	40 db
9000 OHMS	20 db

All resistance values in ohms unless otherwise specified.

Fig. 90 — Cascaded RC-coupled feedback amplifier using two CA3000 circuits.

the high-frequency roll-offs of the amplifier and thus improves stability.

The gain-frequency characteristic of the feedback amplifier is shown in Fig. 91(a) for a feedback resistance R_f approaching infinity. The low-end roll-off of the amplifier is determined by the interstage coupling. Because agc may be applied to the first stage, the amplifier shown in Fig. 90 may be used in high-gain video-agc applications under open-loop conditions. If feedback is used to control the gain, agc may still be applied successfully.

Fig. 91(b) shows the agc characteristics for the two-stage amplifier under open-loop and two closed-loop conditions at a frequency of 1 kHz.

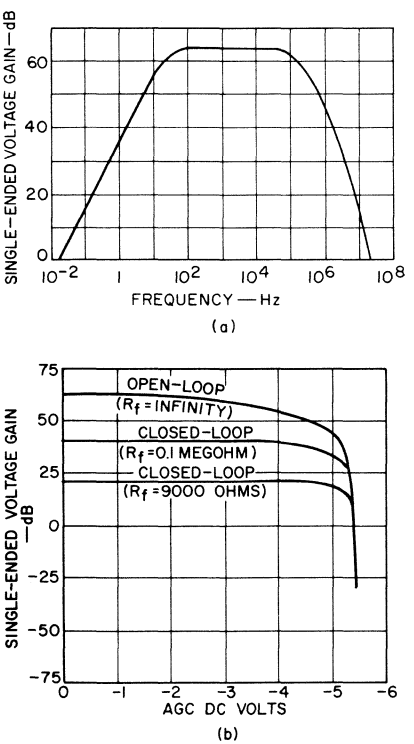


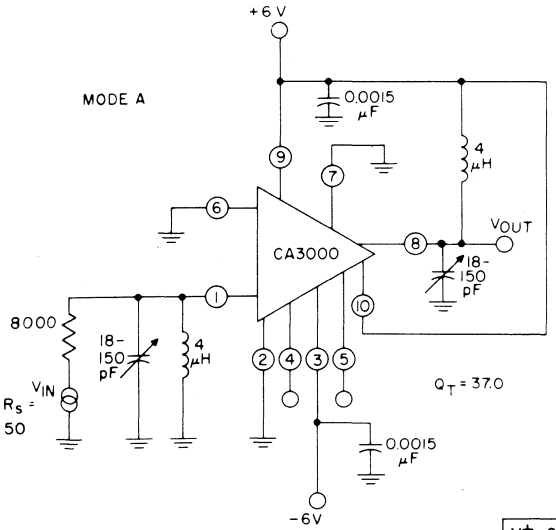
Fig. 91 — Gain-frequency (a) and agc (b) characteristics of the feedback amplifier shown in Fig. 90.

As shown in Fig. 91(a), the open-loop band pass is 18 Hz to 135 kHz; under closed-loop conditions, the band pass is 1.3 Hz to 2 MHz for 40-dB gain and 0.13 Hz to 6.6 MHz or 20-dB gain. The negative feedback thus improves low-frequency performance sufficiently so that the use of the small coupling capacitors C2 and C3 involves little sacrifice in low-frequency response. If three or more CA3000 amplifiers are cascaded, the low-frequency roll-offs must be staggered as well as those at the high end to prevent oscillation. A three-stage cascade has a midband gain of approximately 94 dB.

Narrow-Band Tuned Amplifier— Because of its high input and output impedances, the CA3000 is suitable for use in parallel tuned-input and tuned-output applications. There is comparative freedom in selection of circuit Q because the differential amplifier exhibits inherently low feedback qualities provided the following conditions are met: (1) the collector of the driven transistor is returned to ac ground and the output is taken from the nondriven side, and (2) the input is adequately shielded from the output by a ground plane.

The CA3000 has an output capacitance of approximately 9 picofarads at a frequency of 10 MHz. This capacitance will resonate a 28-microhenry coil at this frequency and provide a minimum Q of 4.55 when the collector load resistor is the only significant load. With this low Q, stagger tuning may be unnecessary for many broad-band applications.

Fig. 92 shows the CA3000 in a narrow-band, tuned-input, tuned-output configuration for operation at 10 MHz with an input Q of 26 and an output Q of 25; the response curve of the amplifier is also shown.



All resistance values in ohms unless otherwise specified.

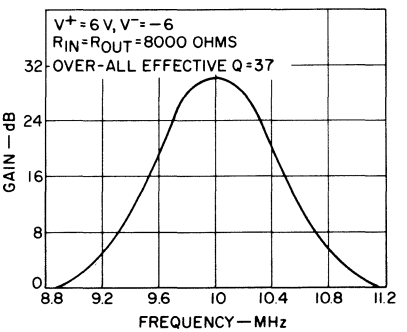
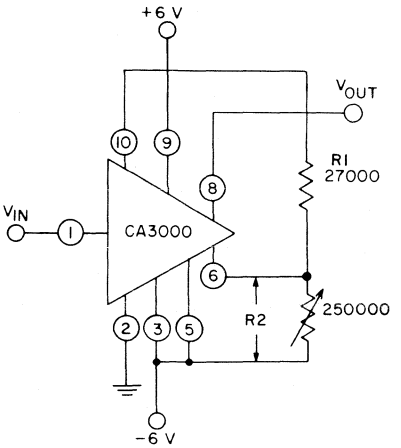


Fig. 92 — Circuit diagram and response curves for a 10-MHz tuned-input, tuned-output narrow-band amplifier using the CA3000.

The 10-MHz voltage gain is 29.6 dB, and the total effective circuit Q is 37. There is very little feedback skew in the response curve. The CA3000 can be used in tuned-amplifier applications at frequencies up to the 30-MHz range.

Schmitt Trigger—The CA3000 can be operated as an accurate, predictable Schmitt trigger provided saturation of either side of the differential amplifier is prevented (hysteresis is less predictable if saturation occurs). Nonsaturating operation is accomplished by operation in mode B (terminals 3 and 5 shorted together) in the configuration shown in Fig. 93. Large values are required for external resistors R1 and R2 because they receive the total collector current from terminal 10. Because of the high impedances, resistor R2 is actually a parallel combination of the input impedance (approximately 0.1 megohm) of the CA3000 and the 0.25-megohm external resistor. The Schmitt-trigger design equations (for $\alpha = 1$) are summarized below. In these equations, Q2 and Q4 are the



All resistance values in ohms unless otherwise specified.

Fig. 93 — Schmitt trigger using a CA3000.

differential-pair transistors, Q1 and Q5 are the emitter-follower transistors, and Q3 is the constant-current-source transistor. The terms V_6 and V_8 represent the voltages at terminal 6 and 8 of the CA3000, and the subscripts I and II indicate the operating state of the Schmitt trigger.

State I: Q2 off, Q4 conducting (not saturated)

$$V_{6I} = \frac{V^+ (R2) - V^- (R1 + 8000)}{R1 + R2 + 8000}$$

where 8000 ohms is the output impedance of Q4 (obtained from the published data). For R1 = 27000 ohms and $V^+ = -V^- = 6$ volts,

$$V_{6I} = \frac{6V (R2) - 6V (35000)}{R2 + 35000}$$

$$R2 = (R1 + 8000)\frac{V^- + V_{6I}}{V^+ - V_{6I}}$$

$$R2 = (35000)\frac{6V + V_{6I}}{6V - V_{6I}}$$

$$V_{8I} = V^+ - I_E (8000)$$

where I_E is the collector current of transistor Q3 ($I_E \approx 0.48$ milliampere in operating mode B with $V^- = -6$ volts.)

$V_{8I} = 2.14$ V
$V_{FI} \equiv$ Firing voltage for transition from state I to state II
$V_{FI} = V_{6I} - 0.053 - 100\ I_E$ at 25°C
$V_{FI} = V_{6I} - 0.101$ V at 25°C

State II: Q2 conducting (not saturated), Q4 off

$$V_{8II} = V^+$$
$$V_{8II} = 6 \text{ V}$$

$$V_{6II} = \frac{(V^+ - I_E\ 8000)\ R2}{R1 + R2 + 8000} - \frac{V^- (R1 + 8000)}{R1 + R2 + 8000}$$

$$V_{6II} = \frac{2.14 \text{ V } (R2)}{R2 + 35000} - \frac{6 \text{ V } (35000)}{R2 + 35000}$$

$V_{FII} \equiv$ Firing voltage for transition from state II back to state I

$$V_{FII} = V_{6II} + 0.053 + 100\ I_E \text{ at } 25°C$$

$$V_{FII} = V_{6II} + 0.101 \text{ V at } 25°C$$

Hysteresis Voltage

$$V_{HYS} = V_{Y_I} - V_{F_{II}}$$

$$= \frac{3.86\ V\ (R2)}{R2 + 35000}$$

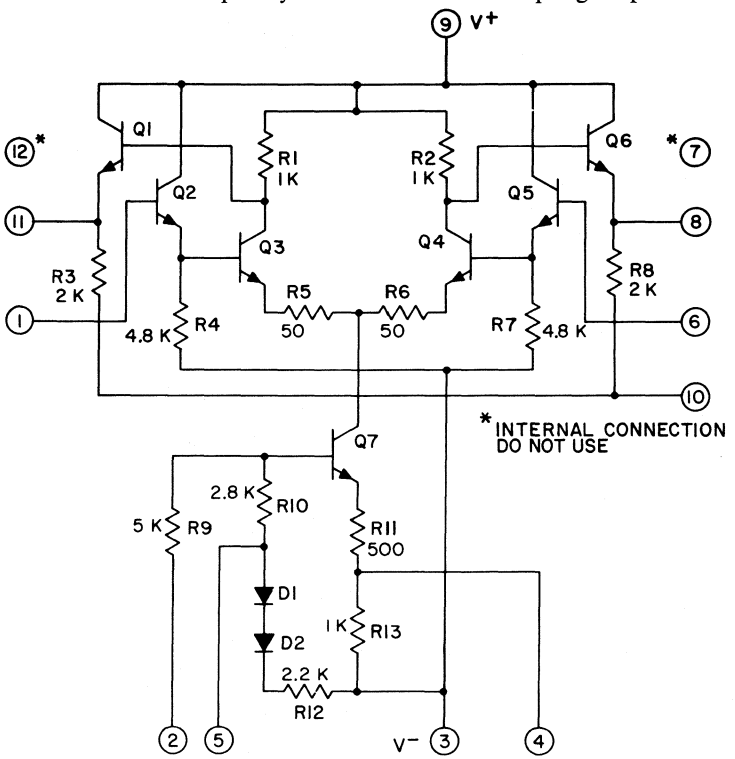
$$= 0.202\ V \text{ at } 25°C$$

From the calculations for state I, it is evident that either V_{6I} or R2 must be a known design value. Because R2 is a composite value, V_{6I} is the more reasonable choice.

VIDEO AMPLIFIER

The CA3001 integrated circuit, shown in Fig. 94, is designed for use in intermediate-frequency or video amplifiers at frequencies up to 20 MHz and in Schmitt-trigger applications. This integrated circuit can be gated, and gain control can be applied. The CA3001 is available in a 12-terminal TO-5-style low silhouette package.

The circuit consists of a differential pair of transistors, Q3 and Q4, the current of which is controlled by a constant-current transistor Q7. Transistors Q1, Q2, Q5, and Q6 are operated in the common-collector configuration to provide a high-impedance input and low-impedance output. Thus, the CA3001 provides double-ended input and output, and can be iteratively connected with low-value coupling capacitors. The



All resistance values in ohms unless otherwise specified.

Fig. 94 — CA3001 integrated-circuit video amplifier.

high-frequency response of the circuit is determined primarily by the resistance and capacitance in the collectors of the differential pair Q3 and Q4.

Biasing Requirements and Operating Modes

When voltage supplies are connected to the CA3001, the most positive voltage must be connected to terminal 9 and the most negative voltage to terminal 3 (internally connected to the substrate and the case). For typical operation, terminals 2 and 10 are returned to ground. If desired, however, automatic gain control can be applied to terminal 2, and terminal 10 can be connected to the negative supply to permit larger negative-going output swings in the output transistors.

The CA3001 may be operated with various supplies and at various levels. Operation from either a single supply or dual supplies is feasible. When dual supplies are used, they may be either symmetrical or nonsymmetrical. The use of separate positive and negative supplies minimizes the need for external components. For single-supply applications, a resistor divider and a bypass capacitor must be added.

When dual supplies are used, the inputs (terminals 1 and 6) are returned to ground through equal external resistors (the maximum recommended value of R is 3300 ohms for linear operation). For single-supply operation, the current through the resistor divider should be greater than 1.5 milliamperes. For either single or dual supplies, the operating current in transistor Q4 is determined by the operating mode. For any given bias voltage, four operating modes are possible, as described in Table VIII. Each mode is characterized by a distinct operating current and a corresponding voltage gain, both of which have a particular temperature dependence.

Table IX shows typical design performance characteristics for the four operating modes of the CA3001 at room temperature. The output operating point and voltage gain of the circuit are reasonably independent of resistor value, but the current and power dissipation may vary with resistor values. Figs. 95 and 96 show theoretical curves of output operating point and voltage gain, respectively, as functions of temperature for nominal resistor values with a supply voltage V^- of -6 volts dc. The voltage between terminals 8 and 9 or terminals 11 and 9 is denoted by V_X. Because the variation of voltage gain and operating point with temperature is small for all operating modes, the choice of mode depends on application requirements. With a supply voltage V^- of -4.5 volts, voltage-gain variation is normally less than 0.5 dB for all operating modes over the temperature range of -55 to 125°C.

Table VIII — *Four Possible Operating Modes for CA3001 Amplifier*

Operating Mode	Shorted Terminals	Condition of Diodes	Q4 Emitter Resistor
A	none	in	R11 + R13
B	5-3	out	R11 + R13
C	4-3	in	R11
D	5-4-3	out	R11

Table IX — *Typical Design Performance Characteristics for the CA3001 Amplifier (terminals 2, 10, 6, and 1 referenced to ground) at 25°C*

Operating Mode	Supplies (±V)	Output Operating Volts (Term. 8 and 11 to ground)	Positive Supply Current (mA)	Negative Supply Current (mA)	Power Dissipation (mW)	Single-Ended Voltage Gain at 1 MHz (dB)
A	6	4.3	8.4	—4.7	79	15.5
B	6	4.8	7.8	—3.9	70	12.7
C	6	2.8	9.9	—7.9	106	17.8
D	6	4.1	8.7	—5.5	85	16.4
A	4.5	3.0	6.0	—3.4	43.6	14.6
B	4.5	3.4	5.6	—2.7	37.6	10.0
C	4.5	2.0	7.2	—5.8	58.4	17.7
D	4.5	2.9	6.0	—3.7	43.6	15.5
A	3	1.8	3.7	—3.9	22.6	13.0
B	3	2.1	3.3	—1.4	14.3	3.8
C	3	1.0	4.4	—3.7	25.5	16.4
D	3	2.0	2.4	—1.9	13.0	10.8

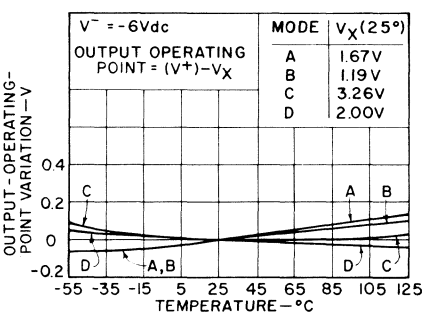


Fig. 95 — Output operating point of the CA3001 (normalized to the 25°C operating point) as a function of temperature.

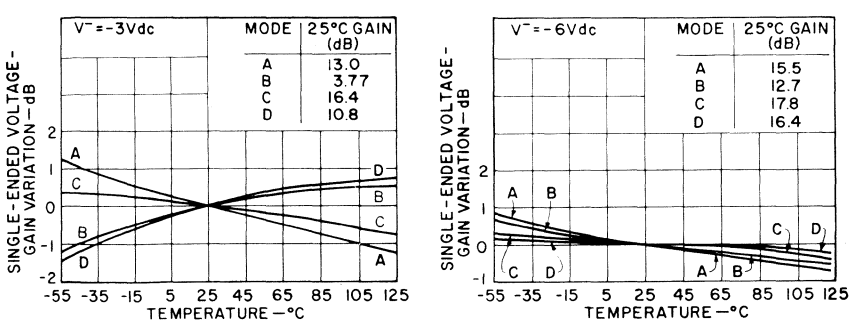


Fig. 96 — Voltage gain of the CA3001 (normalized to the 25°C gain) as a function of temperature.

Frequency Response

When the CA3001 video amplifier is used in cascade, its high-frequency response is determined primarily by the RC roll-off at the collectors of the differential-pair transistors Q3 and Q4. The generator source resistance may affect high-frequency bandwidth; for full bandwidth capability, the parallel combination of source resistance and base-bias resistance should not exceed 800 ohms. The low-frequency response is determined by the coupling capacitor and the base-bias resistance value.

Fig. 97 shows the frequency-response characteristics of the CA3001 operated in mode C with supplies of ±6 volts. The high-frequency roll-off of the CA3001 is a function of the values of resistors R1 and R2 in Fig. 94 and their variation with temperature.

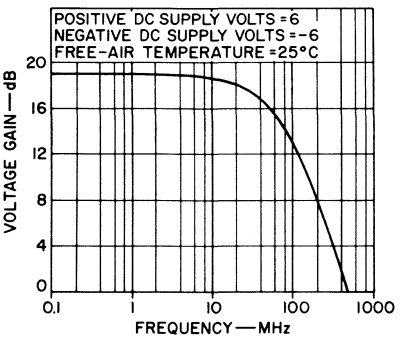


Fig. 97 — Frequency response of the CA3001 in mode C.

Input and Output Impedance

Fig. 98 shows the parallel input resistance and capacitance of the CA3001 as a function of frequency. The input capacitance is constant until it begins to decrease at high frequencies. The input resistance decreases through the frequency range from 0.1 to 10 MHz. Because the input resistance is high in comparison with the external base-bias resistors used (3300 ohms maximum), the high-frequency response characteristic of the input is determined by the driving-source resistance, the base-bias resistors, and the parallel input capacitance.

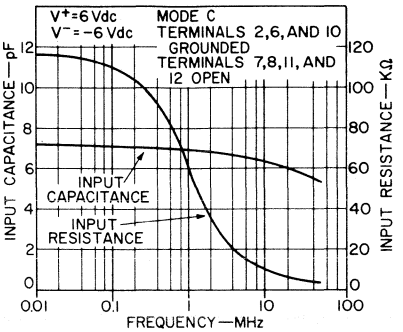


Fig. 98 — Parallel input resistance and capacitance of the CA3001 as functions of frequency.

The parallel output resistance of the CA3001 is low (approximately 70 ohms), and the output reactance is sufficiently high to provide little or no degradation of frequency response through the usable frequency range.

Noise Figure

Fig. 99 shows noise figure as a function of source resistance for fre-

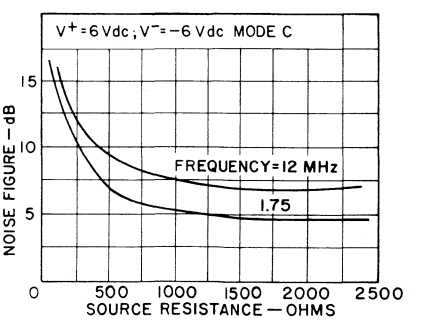


Fig. 99 — Noise figure of the CA3001 as a function of source resistance.

quencies of 1.75 and 12 MHz. For stages in which noise performance is important, the source resistance should not be less than 500 ohms because of the rapid rise in noise figure at lower values. The noise figure of the CA3001 increases when non-driven base-bias resistors are unbypassed. For stages in which noise performance is important, the external resistor on an input base that is not receiving the signal must be bypassed if minimum noise figure is to be achieved.

Gain Control

AGC can be applied to the CA3001 at terminal 2 for any of the four operating modes. Fig. 100 shows representative agc characteristics for modes C and D at a frequency of 1 MHz. The threshold

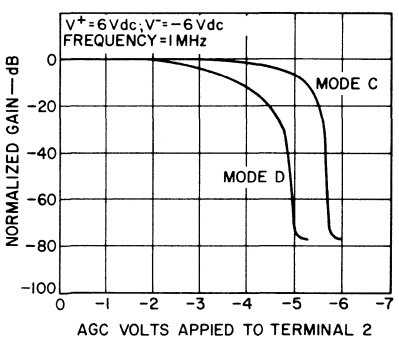


Fig. 100 — AGC characteristics of the CA3001 in modes C and D at 1 MHz.

voltage is higher in mode C than in mode D because of the difference in the base-bias circuit for the constant-current-source transistor (Q4).

The agc range is dependent on frequency at high frequencies because the feedthrough parameters are primarily capacitive; therefore, it should eventually decrease at a rate of approximately 20 dB per decade. The average measured agc range at 10 MHz is 62 dB, and is 15 dB less than that at 1 MHz.

Harmonic Distortion and Swing Capability

When equal positive and negative supplies are used, operating mode C provides the largest swing capability because the output operating point is approximately centered. With voltage supplies of ±6 volts dc at a frequency of 1 MHz, the single-ended output is 1.3 volts rms for 3-per-cent distortion in mode C and 0.665 volt rms in mode D.

The signal-swing capability was also evaluated as a function of temperature in mode C with voltage supplies of ±6 volts dc. For 3-per-cent distortion, an output swing of 1.2 volts rms can be obtained over the temperature range from 25 to 125°C.

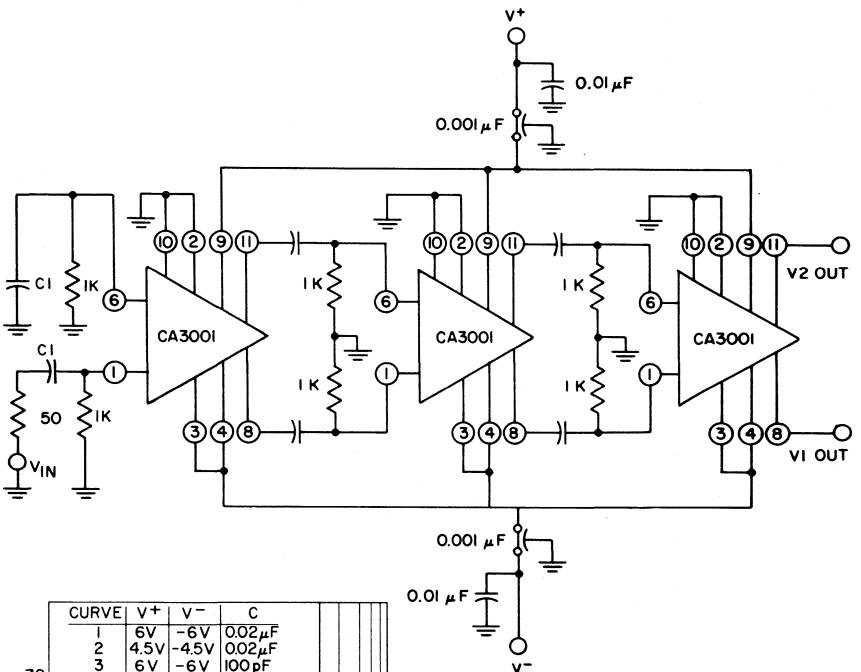
For pulse-type signals, the total possible swing capability is important. The voltage at the collectors of the differential pair may rise to the positive supply voltage, V^+, and fall to the saturation level. If the bases of the input emitter-followers are maintained at zero potential, the emitters of the differential pair are negative by twice the base-to-emitter voltage drop, V_{BE}, or approximately −1.4 volts. If the saturation voltage is assumed to be 0.2 volt, the collectors drop to about −1.2 volts before saturation. Therefore, the total swing available at the collectors is approximately $V^+ + 1.2$ volts; for a V^+ of 6 volts, the swing is 7.2 volts. The output voltage swing is lower than this value by V_{BE}, or from 5.3 to −2.0 volts. This total swing capability can be realized only when the resistors R3 and R8 are returned to the negative supply voltage (terminal 10 shorted to terminal 3). Selection of the operating point to obtain most of the available total swing in

one direction involves proper choice of the operating mode and the negative supply voltage.

Cascade Operation

Over-all performance characteristics for three CA3001 stages operated in cascade are shown in Fig. 101. The need for supply decoupling is minimized by the symmetry of the circuit, which ensures equal and out-of-phase currents in the supply leads. Three circuits in close proximity can provide stable over-all gains of approximately 65 dB. A further advantage of the CA3001 in cascade is that a gain increase of 6 dB accrues each time a double-ended output is used.

Table X and Fig. 101 show the performance of the CA3001 in the three-stage cascade circuit for various values of supplies and coupling capacitors. The only advantage of ±6-volt supplies as compared to ±4.5-volt supplies is a larger output-swing capability.



All resistance values in ohms unless otherwise specified.

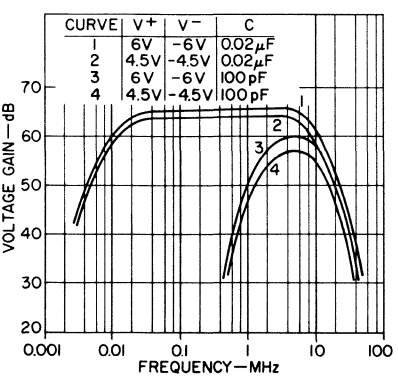


Fig. 101 — Three-stage CA3001 cascade amplifier and frequency-response characteristics.

Table X — *Performance of CA3001 Cascade Amplifier shown in Fig. 101*

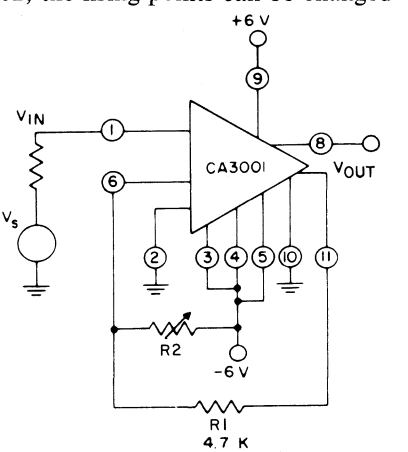
Coupling Capacitor	0.02 μF		100 pF		
Voltage Supplies	±6	±4.5	±6	±4.5	Vdc
Power Dissipation	276	146	276	146	mW
Single-Ended-Output					
Mid-Band Gain	64.5	63	60.5	57.5	dB
3-dB Response: Upper	9	9	10.5	10.5	MHz
Lower	0.0125	0.0125	1.9	1.9	MHz
AGC Range	65	63	61	59	dB
Output Signal for 3-per-cent Distortion	1.3	1.15	1.15	0.7	Vrms
Input Signal for 3-dB Signal-to-Noise Ratio	26	14	20	18.5	μVrms

The use of ±4.5-volt supplies entails no sacrifice in bandwidth and little gain loss, and provides a saving in power dissipation of almost 2 to 1. Better signal-to-noise performance can be achieved with no change in bandwidth if a higher value of source resistance is used (e.g., 800 ohms, rather than the value of 50 ohms shown in Fig. 101). The agc range of the cascaded circuit is 10 dB less than that for an individual circuit because no interstage shielding is provided and double-ended output is not used.

Schmitt-Trigger Operation

The CA3001 has an advantage in Schmitt-trigger applications because the emitter-follower outputs isolate the impedances of the feedback loop from the differential stage. These outputs are also capable of driving low-impedance loads. When symmetrical power supplies of up to ±6 volts are used, the CA3001 operates without saturation of the basic differential pair (Q3 and Q5). For each of the four operating modes, a complete offset at the input that causes all the source current to pass through either Q3 or Q4 does not bring these transistors into saturation. As a result, uncertainties resulting in hysteresis prediction caused by storage time are eliminated.

When the CA3001 is connected as a Schmitt trigger, as shown in Fig. 102, the firing points can be changed by adjustment of the resistor R2. This resistor value effectively sets the voltage at the input terminal 6 and requires that the input firing voltage at terminal 1 approach this value to obtain trigger action. The hysteresis voltages obtained for various trigger levels in the circuit of Fig. 102 are shown in Table XI.



All resistance values in ohms unless otherwise specified.

Fig. 102 — CA3001 Schmitt trigger.

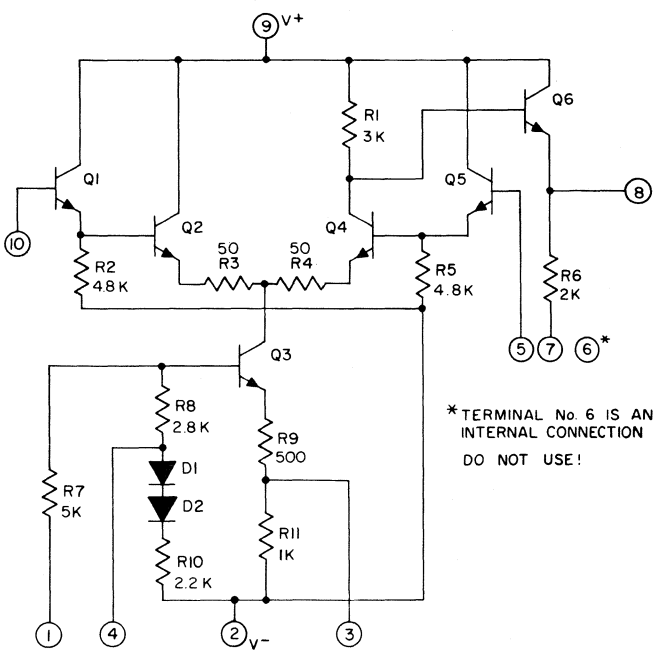
Table XI — *Performance Data for CA3001 Used as a Schmitt Trigger*

Input Firing Volts			
Transition from State I to State II	Transition from State II to State I	Hysteresis Volts	R2 Approximate Setting
3.0	1.5	1.5	max. resistance
1.1	0.1	1.0	decreasing R2
−1.4	−1.9	0.5	
−3.2	−3.2	0	

IF AMPLIFIER

The CA3002 integrated-circuit if amplifier can be used with either a single-ended or a push-pull input. Its applications include RC-coupled if amplifiers, video amplifiers, envelope detectors, product detectors, and various trigger circuits. The if amplifier is supplied in a 10-terminal TO-5-style low-silhouette package.

Fig. 103 shows the circuit diagram for the CA3002 integrated circuit. The circuit is basically a single-stage balanced differential amplifier (Q2 and Q4) with input emitter followers (Q1 and Q5), a constant-current-source transistor (Q3) in the emitter-coupled leg, and an output emitter follower (Q6). A single-ended input is connected to terminal 10 or a push-pull input to terminals 10 and 5. A single-ended output is direct-coupled at terminal 8. Terminals 5 and 10 must be provided with dc returns to ground through equal external base resistors. The emitters of the differential-pair transistors (Q2



All resistance values in ohms unless otherwise specified.

Fig. 103 — CA3002 integrated-circuit if amplifier.

and Q4) are connected through degenerative resistors (R3 and R4) to the current-source transistor (Q3). The use of these resistors improves the linearity of the transfer characteristic and increases the signal-handling capability.

Transistor Q1 provides a high input impedance for the if amplifier. Transistor Q5 preserves the circuit symmetry, and also partially bypasses the base of Q4. Additional bypassing can be obtained by connection of an external capacitor between terminal 5 and ground. The emitter-follower transistor Q6 provides a direct-coupled output impedance of less than 100 ohms.

Circuit Characteristics

When voltage supplies are connected to the CA3002, the most positive voltage must be connected to terminal 9 and the most negative voltage to terminal 2 (internally connected to the substrate and case). The CA3002 may be operated from various supplies and at various levels. Operation from either single or dual power supplies is feasible. When two supplies are used, they may be either symmetrical or nonsymmetrical. When both positive and negative voltage supplies are used, external components can be minimized. For single-supply applications, a resistor divider and a bypass capacitor must be added externally. The current through R2 and R3 should be greater than one milliampere. Except in applications that use inductive drive, equal external base resistors must be added at terminals 5 and 10 to provide base-current returns. Terminal 7 can be connected to ground, or to the negative supply if a larger negative-going voltage swing is desired at any operating point.

For either single or dual supplies, the operating current in transistor Q3 is determined by the bias voltage between terminals 1 and 2. The more negative point of this bias voltage must be connected to terminal 2. For dual-supply systems, terminal 1 is usually referenced to ground.

Operating Modes—For any given bias voltage (V^- when terminal 1 is grounded), four operating modes are possible, as described in Table XII. In general, each mode is characterized by (1) a distinct dc operating point with a characteristic temperature dependence, and (2) a particular value of gain that has a distinct temperature dependence.

When the diodes are utilized in the bias circuit (modes A and C), the current is essentially dependent on the temperature coefficient of the diffused emitter resistors R9 and R11, and has a tendency to decrease with increasing temperature at a rate independent of the negative supply voltage. The temperature coefficient of the diffused collector resistor R1 is the same as that of the emitter resistor, and a constant collector-voltage operating point results at the collector of transistor Q4. However, the operating point at output terminal 8 is modified by the base-emitter

Table XII — *Identification of CA3002 Operating Modes*

Operating Mode	Shorted Terminals	Condition of Diodes	Q3 Emitter Resistor
A	none	in	R9 + R11
B	4-2	out	R9 + R11
C	3-2	in	R9
D	4-3-2	out	R9

voltage drop of transistor Q6 and its temperature dependence. Typical variation of the output operating point with temperature is shown in Fig. 104 for the four operating modes. The voltage between terminals 8 and 9 is denoted by V_X. In

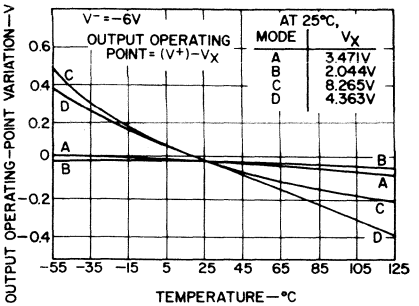


Fig. 104 — Output operating point of the CA3002 (normalized to the 25°C operating point) as a function of temperature.

mode B (with the diodes out of the bias circuit), it should be noted that the output operating point is constant with temperature because the change in the collector operating point is cancelled by the change in the base-emitter voltage drop (V_{BE}).

When the diodes are out of the bias circuit, the current-temperature curves become dependent on the negative supply voltage. Therefore, the value of V^- can be adjusted so that the transconductance decreases, increases, or remains constant with temperature. As shown in Fig. 105, the gain increases with temperature for a −3-volt V^- supply, but decreases with increasing temperature for a −6-volt V^- supply. At some intermediate value of V^- (approximately −4.5 volts), the gain should be constant as a function of temperature. In any case, however, a constant ac gain with temperature is accompanied by a change in the collector operating point of transistor Q4.

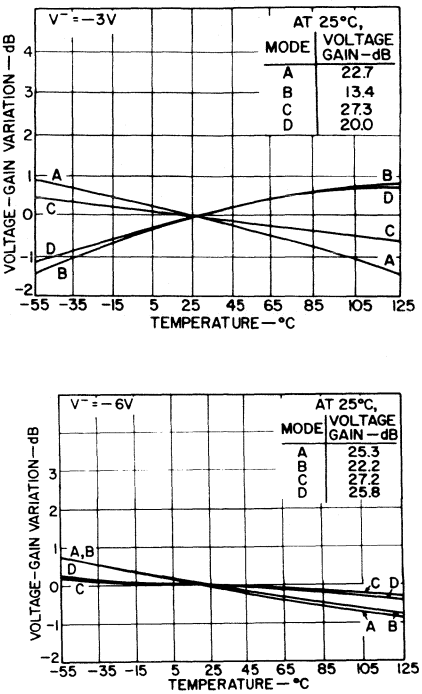


Fig. 105 — Voltage gain of the CA3002 (normalized to the 25°C voltage gain) as a function of temperature with V^- supply voltages of −3 and −6 volts.

Table XIII lists typical design performance characteristics for the four operating modes of the CA3002. By use of the data in this table and in Figs. 104 and 105, it is possible to select the proper operating mode to provide the most transconductance per milliwatt of dissipation, the specified output-swing capability, and the desired temperature performance for a particular design requirement.

In operating mode C, a valid nonsaturated operating point may be obtained by use of nonsymmetrical voltage supplies. For example, when V^- is −3 volts, the operating point will not be in saturation if a positive supply voltage of 4.5 volts or more is used. Resistor R6 may then

Table XIII — *Typical Design Performance Characteristics for the Four Operating Modes of the CA3002 (Terminals 7 and 1 are grounded; temperature = 25°C)*

Mode	± Supply Volts	Output Operating Volts (Term. 8 to ground)	Voltage Gain (dB) at 1 MHz	+ Supply Current (mA)	− Supply Current (mA)	Power Dissipation (mW)
A	6	2.6	26.4	5.0	4.2	55.2
B	6	3.8	22.5	4.7	3.7	50.4
C	6	0	*	*	*	*
D	6	1.8	25.4	5.1	4.9	60
A	4.5	2.0	24.0	3.6	3.0	29.7
B	4.5	3.0	19.8	3.4	2.6	27.0
C	4.5	0	*	*	*	*
D	4.5	1.8	24.5	3.7	3.3	31.5
A	3	1.1	22	2.3	2.0	12.9
B	3	2.0	14.5	2.1	1.5	10.8
C	3	0	*	*	*	*
D	3	1.5	20	2.2	1.9	12.3

* Transistor Q4 saturated, transistor Q6 cut off.

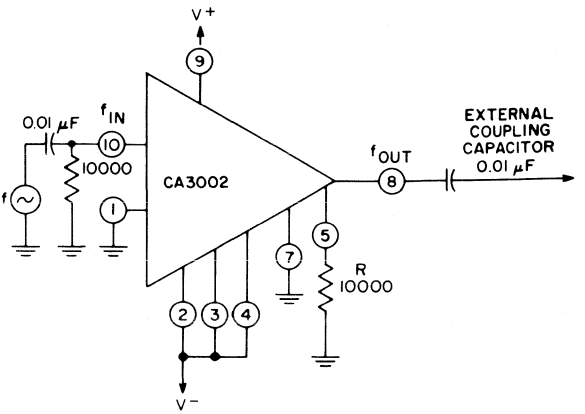
be returned to the negative supply instead of to ground to ensure the desired negative swings.

Input Impedance—The input impedance of the CA3002 is essentially a characteristic of the input emitter followers, Q1 and Q5. Because these transistors are lightly loaded, they have parallel input impedances that are approximately 0.1 megohm at low frequencies and rise to infinity and become negative at a few megahertz. In most cases, these impedances are negligible in comparison with the impedances of external base resistors or inductors. The input capacitance is 3 to 5 picofarads.

The input impedance decreases with decreasing operating temperature. A typical low-frequency value of parallel input resistance is 55,000 ohms at −55°C. If a resonant line or tuned circuit that has appreciable impedance in the vhf range is connected to either input terminal, a series parasitic resistor of 50 to 100 ohms should be placed in series with the input lead to prevent vhf oscillation.

Output Impedance—The output impedance of the CA3002 is essentially that of the output emitter follower Q6, and is a function of the current in Q6. The current, in turn, is determined by the operating mode, the supply voltages, and the connection of resistor R6 to ground or to terminal 2. In operating mode D with R6 returned to ground and ±6-volt supplies, the output resistance is approximately 80 ohms over most of the useful frequency range and rises to about 110 ohms (its highest value) at −55°C.

Frequency Response—The mid-frequency voltage gain of the CA3002 if amplifier is essentially independent of absolute resistor values, but depends on the resistor ratios. The response curves for an iterative-coupled amplifier that uses 0.01-microfarad input-coupling and output-coupling capacitors are shown in Fig. 106. If 1-microfarad coupling capacitors are used, the low-frequency response can be extended below 100 Hz. The addition of a 0.01-microfarad capacitor at termi-



All resistance values in ohms unless otherwise specified.

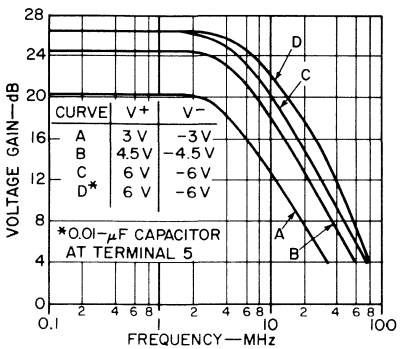


Fig. 106 — Effective single-stage response characteristics for CA3002 if amplifier using 0.01-microfarad coupling capacitors. Curve D represents operation with 0.01-microfarad bypass capacitor (not shown) connected at terminal 5.

nal 5 improves the high-frequency performance.

Gain Control—The voltage gain of the CA3002 can be controlled over a wide range by adjustment of a negative dc voltage applied at terminal 1. Fig. 107 shows the voltage gain at 1.75 MHz as a function of the dc voltage. When the gain is controlled in this manner, the CA3002 can be used as an if amplifier with a 75-dB agc range, or as a video gating, squelching, or blanking circuit with a similar range. The circuit function depends only on the manner in which the dc voltage applied to terminal 1 is controlled. The agc range is dependent on frequency, and decreases from 75 dB at 1 MHz to 60 dB at 25 MHz.

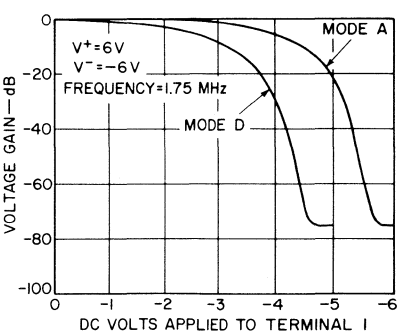


Fig. 107 — Voltage gain of the CA3002 as a function of negative dc supply voltage applied at terminal 1 (normalized to a gain of 26 dB).

Third-Order Intermodulation Distortion—Fig. 108 shows the peak-to-peak input signal required to pro-

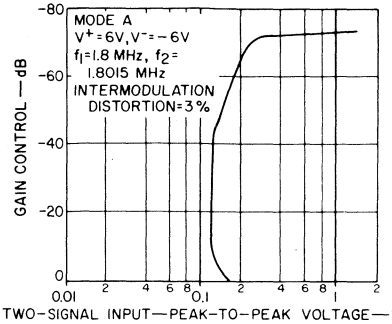


Fig. 108 — Third-order intermodulation characteristics of the CA3002 as a function of agc.

duce third-order intermodulation distortion of 3 per cent as a function of gain control for the CA3002 integrated circuit. The maximum tolerable signal input for 3-per-cent intermodulation distortion is relatively constant over the entire agc range, but increases dramatically as cutoff is attained. When the CA3002 is operated in mode A with supplies of ±6 volts and an agc of −30 dB, a peak-to-peak input signal in excess of 100 millivolts is typically required for 3-per-cent distortion.

Noise Figure—Noise figure is an important design parameter for both video and if-amplifier applications. When a 1000-ohm source is used, the noise figure of the CA3002 is 4 dB over a large portion of the frequency range of 1 kHz to 10 MHz. The 1/f noise corner occurs at approximately 15 kHz, and the high-frequency noise rise begins at approximately 4 MHz. Fig. 109 shows noise figure as a function of source resistance at 1.75 MHz. The typical noise figure is less than 4 dB. It is reasonably flat for source resistances from 500 to 2500 ohms, but rises rapidly at values below 500 ohms.

When external base-bias resistors are used, terminal 5 should be bypassed by an external capacitor for any stage in which low noise figure is required. If the base-bias resistors are not bypassed, the noise figure increases. In a practical receiver, bypassing may be avoided if the input at terminal 10 is transformer driven (from a filter) and terminal 5 is grounded. In the later if stages, noise figure can usually be ignored.

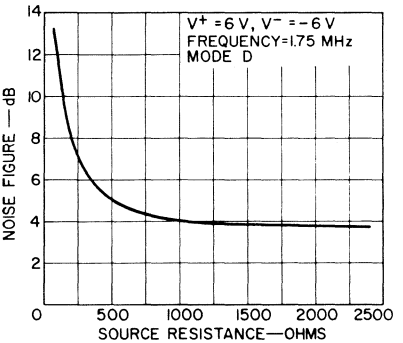
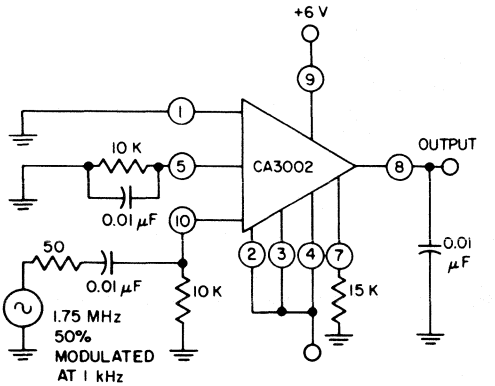


Fig. 109 — Noise figure of the CA3002 as a function of source resistance.

Applications of the IF Amplifier

The CA3002 integrated-circuit if amplifier is a versatile circuit that can be used for many diverse applications. The balanced differential amplifier fed from a constant-current source makes an excellent controlled-gain if amplifier. The gain-control function may be extended to include video gating, squelching, and blanking applications. Envelope detection can be achieved by suitable biasing of the emitter-base diode of the output emitter-follower transistor. Product detection can be obtained by reinsertion of the carrier at the base of the constant-current-source transistor. Various trigger and waveform-generating circuits can also be achieved by the addition of suitable external components.

Envelope Detector—Fig. 110 illustrates the use of the CA3002 integrated circuit as an envelope detector.



All resistance values in ohms unless otherwise specified.

Fig. 110 — Envelope detector using a CA3002.

In this circuit, the emitter of the output transistor Q6 is operated at zero voltage by connection of an external resistor in the bias loop of the constant-current transistor Q3.

The current in the differential-pair transistors (Q2 and Q4 in Fig. 103) is increased to the point at which the common-collector output transistor Q6 is biased almost to cutoff. For this current increase, the constant-current transistor Q3 is operated with terminal 4 open, and the emitter resistor R9 is shunt loaded by the external resistor at terminal 3. With this circuit, envelope detection can be accomplished only in mode A.

Although the output transistor is nearly cut off, all the other active devices are operating in their linear regions. For small ac signals, therefore, the circuit provides linear operation except for Q6, which is turned on only by a positive signal. The maximum acceptable input signal depends on the linear range of the differential amplifier. An external filter capacitor is connected between terminal 8 and ground to remove the rf signal from the detected audio output.

Fig. 111 shows the input-output characteristics of the CA3002 envelope-detector circuit shown in Fig. 110. The usable range of input signals for distortion below 3 per cent is 10 to 100 millivolts (20-dB range).

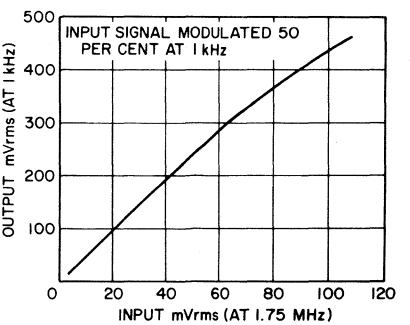


Fig. 111 — Input-output characteristics of the envelope detector shown in Fig. 110.

Automatic gain control of the if amplifier must maintain the input signals to the detector within this range.

Product Detector—A differential pair of transistors driven by a constant-current transistor can be used as a product detector if a suppressed-

carrier signal is applied to the differential pair and the regenerated carrier is applied to the constant-current transistor. There are two requirements for linearity: (1) the circuit must be operated in a linear region, and (2) the current from the constant-current transistor must be linear with respect to the reinserted carrier voltage.

The CA3002 satisfies these requirements and can be used as a product detector in the circuit shown in Fig. 112. A double-sideband suppressed-carrier signal is applied at terminal 10, and the 1.7-MHz carrier is applied to terminal 1. Because of the single-ended output, a high-frequency bypass capacitor (0.01 microfarad) is connected between terminal 8 and ground to provide filtering for the high-frequency components of the oscillator signal at the output.

When the amplitudes of the suppressed-carrier signal and the oscillator signal are varied, the gain and distortion characteristics shown in Table XIV are obtained. The conversion voltage gain is constant at input signals up to 16 millivolts and would be 6 dB less for a single-sideband signal than for the double-sideband signal. The distortion increases with increasing input signal; for distortion of less than 1 per cent, the input drive level does not exceed

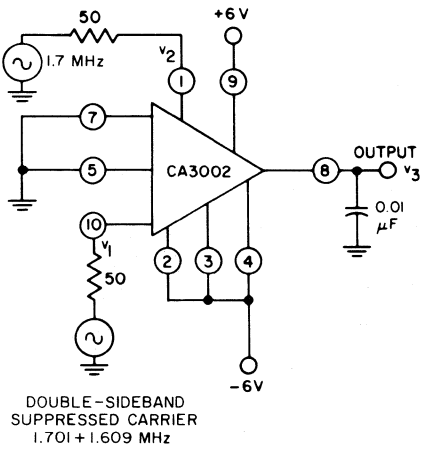


Fig. 112 — CA3002 product-detector circuit.

Table XIV — *Performance Data for CA3002 as Product Detector*

V_1 Double-Sideband Voltage (mV)	V_2 Oscillator Voltage at Term. 1 (V)	V_3 Output at Term. 8 at 1 kHz (mV)	Conversion Voltage Gain (dB)	dB down from Fundamental of Harmonics * Harmonic 2nd	3rd
1	1.7	12.5	21.9	60	>65
4	1.7	50	21.9	51	61
8	1.7	100	21.9	46	56
16	1.7	200	21.9	37	46
32	1.7	310	19.8	32	30▲
4	0.25	22	15.6	15	42■
4	0.5	42	20.3	32	52
4	1.0	60	23.5	45	60
4	1.3	60	23.5	49	61
4	1.7	50	21.9	51	61
4	2.0	48	21.6	52	62
4	2.5	31	17.8	49	60
4	3.0	15	11.4	42	60

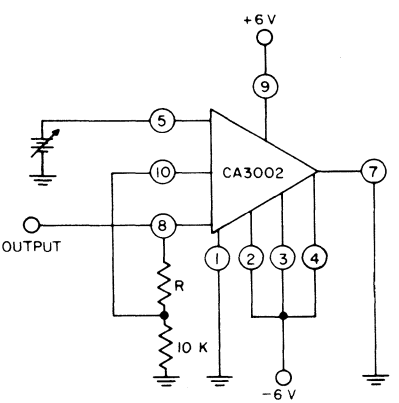
* 4th and 5th harmonics greater than 65 dB down except as noted.
▲ 4th harmonic 51 dB down, 5th harmonic 64 dB down.
■ 4th harmonic 44 dB down.

8 millivolts. The gain maximizes for oscillator voltages of 1 to 2 volts, and the distortion characteristic is also best in this region. Distortion increases both at low oscillator drive levels (0.25 volt) and at high levels (3 volts).

Schmitt Trigger—Fig. 113 shows the use of the CA3002 as a Schmitt trigger. In this application, the input is applied to terminal 5, and both the output and the feedback are taken from the output emitter follower at terminal 8. The emitter-follower output isolates the feedback loop from the differential pair and makes it possible for the circuit to drive low-impedance loads. An additional advantage is that neither transistor of the differential pair saturates as the resistance of the feedback loop is varied. Fig. 113 also shows the output swing and associated hysteresis of the Schmitt trigger as a function of resistor R and the dc input voltage level at terminal 5.

RF AMPLIFIERS

The CA3004, CA3005, CA3006, CA3028A, CA3028B, and CA3053 integrated-circuit rf amplifiers are supplied in TO-5-style packages. The CA3004, CA3005, and CA3006 are 12-terminal units designed to operate from low or medium dc supply voltages at frequencies from dc to 120 MHz. These circuits may be operated from single or dual dc power supplies. For dual-supply operation, either symmetrical or nonsymmetrical power supplies may be used. The CA3028A is an 8-terminal unit designed to operate from a single dc supply of 9 or 12 volts at frequencies from dc to 120 MHz. The CA3028B, which is essentially a premium version of the CA3028A, features tight control of operating current, input offset voltage, input bias, and offset current and increased device breakdown capability that permits operation at supply voltages



All resistance values in ohms unless otherwise specified.

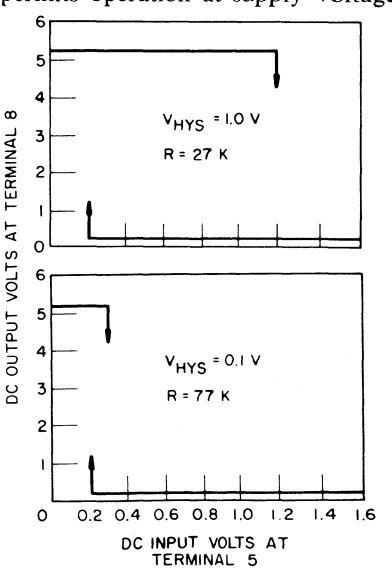
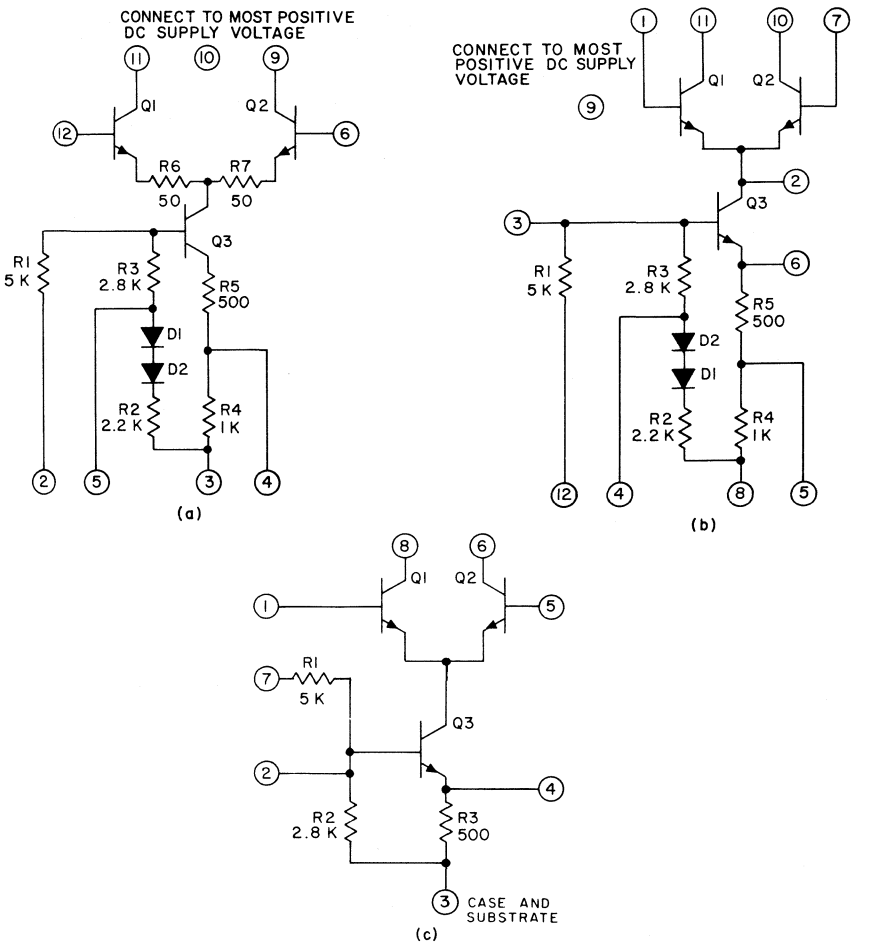


Fig. 113 — CA3002 Schmitt trigger circuit and the output swing and associated hysteresis for the circuit.

greater than 15 volts. This circuit is recommended for those applications in which exceptional dc balance and stability of operating conditions are prime requisites. The CA3053 is essentially a low-frequency version of the CA3028A. This type is intended primarily for FM if-amplifier applications. All the rf amplifiers have an inherent gain-control capability and provide stable operation over a range of ambient temperatures from −55°C to +125°C. These circuits are extremely versatile devices and may be used with external tuned-circuit, transformer, or resistive load



All resistance values in ohms unless otherwise specified.

Fig. 114 — Integrated-circuit rf amplifiers: (a) CA3004; (b) CA3005 or CA3006; and (c) CA3028A, CA3028B, or CA3053.

impedances to provide the following types of functions:

1. Wide- or narrow-band amplification
2. Mixing
3. Limiting
4. Product detection
5. Frequency generation
6. Generation of pulse or digital waveforms.

Operating Requirements and Characteristics

Fig. 114 shows the schematic diagrams for the integrated-circuit rf amplifiers. Each circuit consists of a balanced differential amplifier that is driven from a controlled constant-current source.

In the CA3004 circuit, resistors (R6 and R7) are included in the emitter leads of the differential pair of transistors, Q1 and Q2. The degeneration introduced by these unbypassed emitter resistors improves the linearity of the transfer characteristics and increases the signal-handling capabilities of the circuit. Fig. 115 shows the dynamic transfer and limiting characteristics of the CA3004. The characteristics show that linear operation is possible over a wide range of differential input voltage and, thus, indicate that relatively large input signals can be handled by the circuit without limiting. These features indicate that the CA3004 is particularly useful for applications in which the ability to handle large input signals is an important consideration.

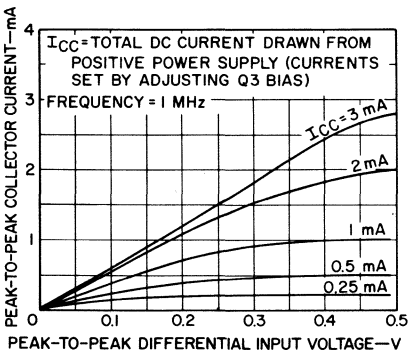


Fig. 115 — Dynamic transfer and limiting characteristics of the CA3004.

In the other rf amplifiers, no emitter resistors are provided for the differential pair of transistors. As a result, these circuits have a smaller dynamic range and provide higher gain than the CA3004 circuit. The dynamic transfer and limiting characteristics of the CA3005 and CA3006, given in Fig. 116, show that these circuits are very good limiting amplifiers. A comparison of the curves in Fig. 116 with those given for the CA3004 in Fig. 115 emphasizes the excellent limiting characteristics of the CA3005 and CA3006.

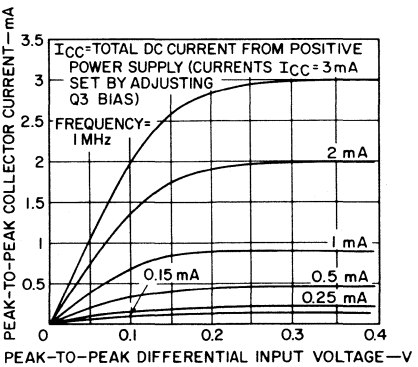


Fig. 116 — Dynamic transfer and limiting characteristics of the CA3005 or CA3006 operated in the differential-amplifier configuration.

Exceptional versatility in the operation of the CA3005, CA3006, CA3028A, CA3028B, and CA3053 is made possible by the availability of internal circuit points to which external circuit elements may be connected to alter the basic circuit con-

figuration. As a result of such external modifications, it is possible to operate these circuits as push-pull amplifiers, as cascode amplifiers, or as single amplifiers in cascade or parallel channels.

The CA3005 and CA3006 rf amplifiers are identical except for their input offset voltages. The offset voltage for the CA3006 is typically less than 1 millivolt, while the offset voltage for the CA3005 is normally in the order of 3 millivolts. The low level of input offset voltage makes the CA3006 well suited for balanced-modulator, mixer, or other push-pull applications that require a well-balanced circuit.

In the CA3028A, CA3028B, and CA3053 rf amplifiers, the temperature-compensating diodes (D1 and D2) used in the other rf amplifiers are omitted from the current-source bias network, and only one value of emitter resistance is available for the constant-current transistor. As a result, these circuits do not provide the bias-circuit options that permit a choice of any one of four possible operating modes in the other rf amplifiers. (These operating modes are discussed in a subsequent paragraph.) The CA3028A and CA3028B circuit exhibits especially good performance characteristics when used in if amplifiers and in FM front ends as an rf amplifier, if amplifier, or converter. The CA3053 provides excellent if-amplifier performance in this type of application.

Supply-Voltage Connections—Fig. 117 shows the supply-voltage connections for differential- and cascode-amplifier operation of the CA3005 or CA3006 from single and dual supplies. When two supplies, one for positive voltage and one for negative voltage, are used, as shown in Fig. 117(a) and 117(c), fewer external components are required. When only one supply is used, an external resistive voltage divider and bypass capacitor must be added to the circuit, as shown in Figs. 117(b) and 117(d). Tuned amplifiers that operate from dual supplies, such as that shown in Fig. 117(a), require the least number of external components.

For either single- or dual-supply operation, the operating current of transistor Q3 is determined by the bias voltage, V^-, applied between terminals 2 and 3 on the CA3004 or between terminals 8 and 12 on the CA3005 and CA3006 (refer to the circuit diagrams in Fig. 114). The more negative terminal of the bias-voltage source must be connected to terminal 3 on the CA3004 or to terminal 8 on the CA3005 and CA3006. In dual-supply systems, terminal 2 of the CA3004 and terminal 12 of the CA3005 and CA3006 are usually returned to dc ground.

Fig. 118 shows the supply-voltage connections for several operating arrangements of the CA3028A, CA3028B, and CA3053. Connections are shown for a differential amplifier that has agc capability, a cascode amplifier with a constant-impedance or conventional agc capability, a converter, a mixer, and an oscillator. Cascode operation of these circuits is preferred for applications that require high gain. The differential-amplifier configuration is preferred when good limiting is required.

Operating Modes—For any given bias voltage V^-, there are four possible operating modes for the CA3004, CA3005, and CA3006 integrated-circuit rf amplifiers. In general, each mode is characterized by (1) a distinct level of operating current and corresponding transconductance, (2) the degree of dependence of the operating current on temperature, and (3) the way in which the

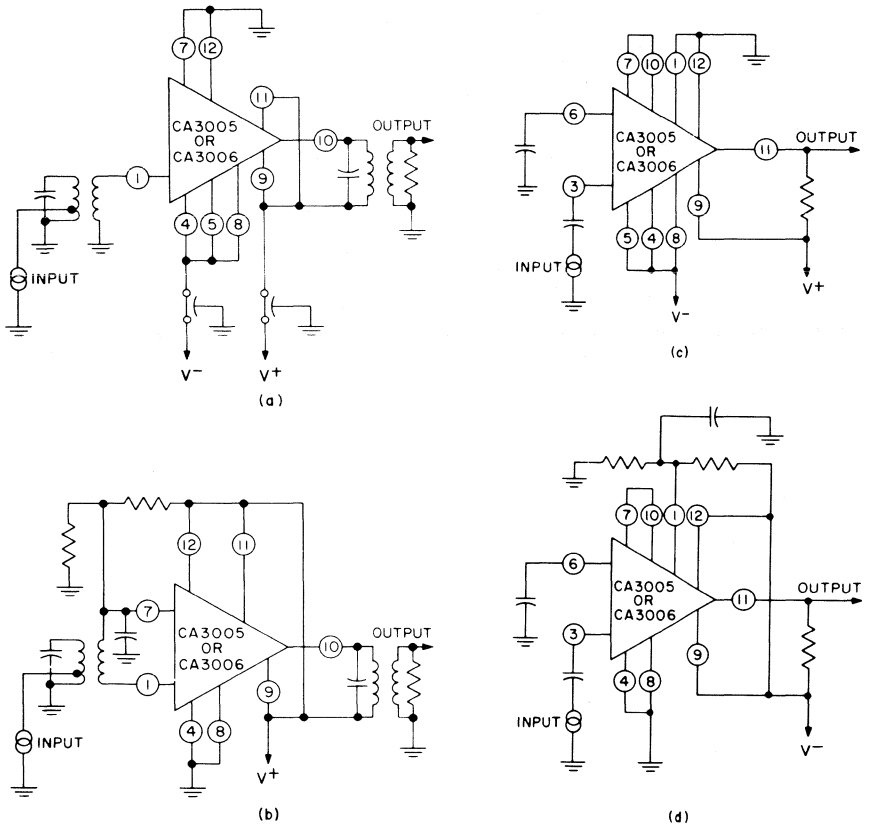


Fig. 117 — Supply-voltage connections for the CA3005 or CA3006 in (a) a differential-amplifier configuration operated from dual supplies, (b) a differential-amplifier configuration operated from a single supply, (c) a cascode configuration operated from dual supply, and (d) a cascode configuration operation from a single supply.

transconductance is affected by temperature. The operating points for the various modes are established by:

1. The emitter resistance selected for the constant-current source transistor, Q3;
2. Whether the base-bias network includes the diodes shown in Fig. 114;
3. The magnitude of the bias voltage, V^-, applied to the circuit.

As pointed out previously, the CA3028A, CA3028B, and CA3053 are designed for only one mode of operation. The performance of the CA3028A and CA3053 circuit, however, is very similar to that of the CA3005 operated in mode C, and the performance of the CA3028B is very similar to that of the CA3006 in mode C. For operation at the same dc supply-voltage levels, the operating current, transconductance characteristics, and temperature dependence of the CA3028A and CA3053 are essentially the same as those of the CA3005 in mode C. Similarly,

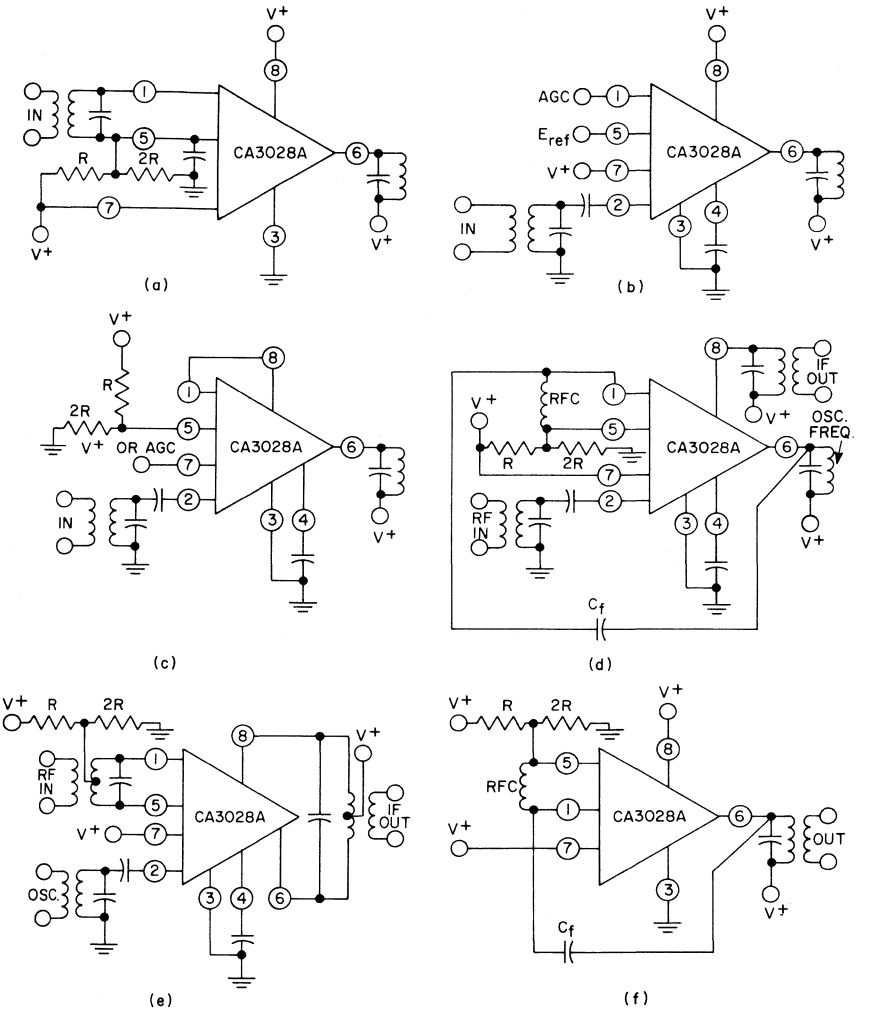


Fig. 118 — Connections for the CA3028A, CA3028B, or CA3053 for use as (a) a balanced differential amplifier with a controlled constant-current-source drive and agc capability, (b) a cascode amplifier with a constant-impedance agc capability, (c) a cascode amplifier with conventional agc capability, (d) a converter, (e) a mixer, and (f) an oscillator.

the behavior of the CA3028B in terms of these parameters closely matches that of the CA3006 in mode C.

Table XV lists the required conditions for the four operating modes of the CA3004, CA3005, and CA3006 integrated-circuit rf amplifiers. When the diodes are included in the base-bias circuit (modes A and C), the operating current, which is primarily dependent on the tem-

Table XV — *Required Conditions for Each Operating Mode of the CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers*

Operating Mode*	CA3004 Terminals Shorted to Term. 3	CA3005 or CA3006 Terminals Shorted to Term. 8	Diodes In or Out of Bias Circuit	Q3 Emitter Resistor(s)
A	—	—	In	R4 + R5
B	5	4	Out	R4 + R5
C	4	5	In	R5
D	4,5	4,5	Out	R5

* For all modes, terminals 2, 6, and 12 of the CA3004 and terminals 1, 7, and 12 of the CA3005 and CA3006 are grounded.

perature coefficient of the diffused emitter resistor, tends to decrease with an increase in temperature at a rate that is relatively independent of the bias supply voltage V^-. When the diodes are not used, however, variation of the current with temperature depends on the magnitude of the supply voltage V^-. The operating current then may remain constant or rise as the temperature is increased, depending upon the value of V^-. The positive supply voltages have no effect on the operating current, and the current-temperature curves are not changed by increases or decreases in this voltage. Some deviation in the current-temperature curves is to be expected because of normal variations in the absolute resistor values.

In general, when diodes are used in the base-bias network of the CA3004, the single-ended transconductance* decreases with increases in temperature. If the diodes are not used, the transconductance may decrease, increase, or remain constant as the temperature increases, depending on the value of the negative supply voltage V^-. With the diodes out, however, the collector operating point tends to shift when resistive loads are used. In applications that require a stable collector dc operating point, therefore, operating mode A or C (diodes in) should be used.

Fig. 119 shows transconductance-temperature curves for operation of the CA3005 or CA3006 in a differential-amplifier configuration in mode C. Fig. 120 shows the transconductance-temperature curves for cascode operation of the CA3005 or CA3006 in mode C. For each type of circuit configuration, the variation in trans-

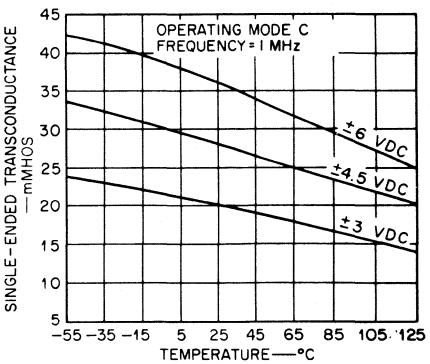


Fig. 119 — Single-ended transconductance of the CA3005 or CA3006 in a differential-amplifier configuration as a function of temperature for operating mode C.

* The single-ended transconductance is the incremental output current for one collector of the differential pair of transistors divided by the incremental input voltage. The curves shown of this parameter are obtained at an operating frequency of 1 MHz.

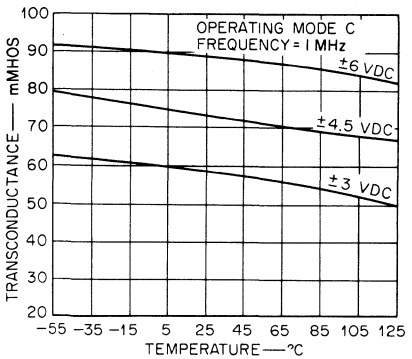


Fig. 120 — Transconductance of the CA3005 or CA3006 in a cascode configuration as a function of temperature for operating mode C.

conductance with temperature is even less for the other three operating modes than that shown for mode C. In general, the transconductance is higher when the diodes are included in the base-bias network (modes A and C) than it is when the diodes are not used (modes B and D).

The power dissipation of the CA3004, CA3005, or CA3006 is highest when the circuit is operated in mode C. Table XVI shows power dissipation and the single-ended transconductance of the circuits for each operating mode. These data may be used to determine the operating point that provides the highest

Table XVI — *Relationship Between the Transconductance and the Power Dissipation of the Integrated-Circuit RF Amplifiers in Each Operating Mode**

Operating Mode	Type of Circuit	DC Supply Voltages (volts)	Single-Ended Transconductance (millimhos)†	Power Dissipation (milliwatts)†
A	CA3004	±3	5.5	6.6
	CA3005 or CA3006		8.5	6.6
	CA3004	±4.5	6.7	15.0
	CA3005 or CA3006		12.8	15.0
	CA3004	±6	7.3	25.0
	CA3005 or CA3006		15.0	25.0
B	CA3004	±3	1.6	2.3
	CA3005 or CA3006		1.9	2.3
	CA3004	±4.5	4.0	7.2
	CA3005 or CA3006		4.9	7.2
	CA3004	±6	5.3	15.0
	CA3005 or CA3006		7.2	15.0
C	CA3004	±3	7.5	17.5
	CA3005 or CA3006		22.0	17.5
	CA3004	±4.5	8.5	40.0
	CA3005 or CA3006		29.0	40.0
	CA3004	±6	9.1	62.8
	CA3005 or CA3006		37.0	62.8
D	CA3004	±3	3.3	4.2
	CA3005 or CA3006		5.0	4.2
	CA3004	±4.5	6.0	17.4
	CA3005 or CA3006		13.0	17.4
	CA3004	±6	7.2	35.9
	CA3005 or CA3006		20.0	35.9

* Circuits are operated in differential-amplifier configurations. The transconductances and power dissipations shown are calculated values for nominal units.

† For operation at the same supply-voltage levels, transconductance and dissipation of the CA3028A and CA3028B are the same as those of the CA3005 and CA3006, respectively, operated in mode C. These characteristics for the CA3053 are also very similar to those for the CA3005 in mode C at frequencies up to 10.7 MHz.

value of transconductance per milliwatt of circuit dissipation for given design conditions.

Admittance Parameters—In the design of rf and if circuits, the four-terminal black-box short-circuit admittance parameters have become a valuable tool. The determination of stability criteria, input and output impedances as a function of load and source admittance, power gain, and voltage gain in iterative connectons are all facilitated by a knowledge of the "y" parameters.

The "y" parameters and their symbols are listed below:

1. Input admittance with the output voltage constant

$$y_i = g_i + jb_i$$

where y_i is the complex input admittance, g_i is the input conductance, and b_i is the input susceptance.

2. Output admittance with the input voltage constant

$$y_o = g_o + jb_o$$

where y_o is the complex output admittance, g_o is the output conductance, and b_o is the output susceptance.

3. Forward-transfer admittance with the output voltage constant

$$y_f = g_f + jb_f$$

where y_f is the complex forward-transfer admittance, g_f is the forward-transfer conductance, and b_f is the forward-transfer susceptance.

4. Reverse-transfer admittance with the input voltage constant

$$y_r = g_r + jb_r$$

where y_r is the complex reverse-transfer admittance, g_r is the reverse-transfer conductance, and b_r is the reverse-transfer susceptance.

In general, it is valuable to understand the essential differences between the "y" parameters of a conventional common-emitter stage and those of compound stages, such as differential and cascode amplifiers.

The differential amplifier, when used at radio frequencies, consists essentially of a common-collector stage that drives a common-base stage. In comparison to the common-emitter "y" parameters, the input admittance y_i, the output admittance y_o, and the forward-transfer admittance, y_f are decreased, almost exactly, by a factor of two when the differential-amplifier configuration is used.

The reverse-transfer admittance y_r is also less for the differential amplifier than for the single transistor in the common-emitter configuration. The ratio of the imaginary term in the differential-amplifier admittance to that of the single transistor is 1/140 at low frequencies and 1/10 at 100 MHz. Fig. 121 shows the ratios of imaginary parts b_{re}/b_{rDA} and real parts g_{re}/g_{rDA} of the reverse-transfer admittances as a function of frequency.

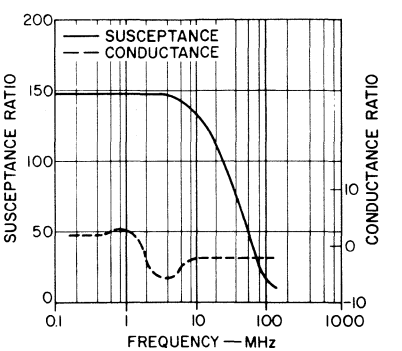


Fig. 121 — Ratio of real (conductance) and imaginary (susceptance) parts of the reverse-transfer admittance for a common-emitter stage to those for a differential-amplifier stage as a function of frequency.

In the cascode configuration of the rf amplifier circuits, a common-emitter stage drives a common-base stage. The input admittance y_i is, therefore, that of a common-emitter stage. The forward-transfer admittance y_f is that of a common-emitter stage times alpha. Because of the high-impedance drive source for the common-base stage, the output admittance y_o is very low (0.06×10^{-5} mho) at low frequencies and is both negative and low at high frequencies. Since the output admittance is low and may be negative, a conjugate match cannot be obtained at the output. Practical amplifiers are possible, however, provided that the sum of the output admittance y_o and the load admittance y_L is positive.

The reverse-transfer admittance y_r for the cascode circuit is less than that for the single-stage common-emitter circuit. The ratio of the imaginary terms of these admittances is 1/1200 at low frequencies and 1/35 at 100 MHz. The ratios of the real parts and of the imaginary parts as a function of frequency are shown in Fig. 122.

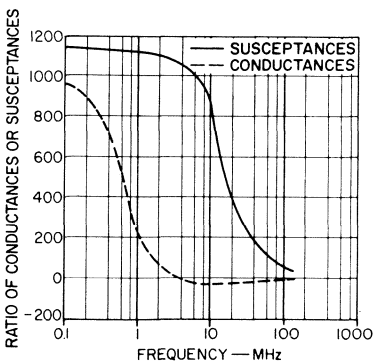


Fig. 122 — Ratio of real (conductance) and imaginary (susceptance) parts of the reverse-transfer admittance for a common-emitter stage to those for a cascode stage as a function of frequency.

Although the y_r is low for both the differential and cascode configurations, instability can occur in high-gain amplifiers. A further consideration in high-gain circuits is that the layout can contribute more feedback than the integrated circuit. Shielding and layout therefore are of prime importance if proper advantage is to be taken of the low feedback of these circuits.

The computed y parameters for the rf amplifiers are given in the individual RCA technical bulletins for these circuits.

Noise Figure—The noise figure of the CA3004, CA3005, and CA3006 integrated-circuit rf amplifiers is a function of the dc operating current and frequency, for both differential and cascode-amplifier configurations. The noise figure increases both with an increase in current and with an increase in frequency. For convenience, noise data are taken in a fixed configuration as the negative supply voltage is varied. On the data plots, the operating currents that correspond to the various supply voltages are included as a separate abscissa to show that the noise figure is a direct function of operating current. Figs. 123 and 124 show representative noise-figure data for tuned amplifiers in the differential and cascode configuration, respectively. In each case, the input and output are tuned, and the input is conjugately matched to a 50-ohm noise diode. Practically no change in noise figure occurs with variations of the positive supply voltage V+.

The curves in Figs. 123 and 124 show that for optimum single-stage noise performance the operating current should be low, which results in a low gain. Thus, in system applications of the tuned amplifiers, the operating current in each stage should be adjusted to obtain the op-

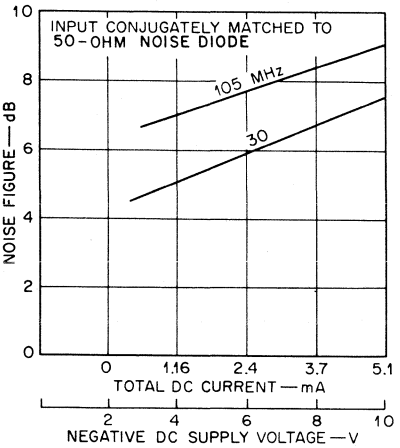


Fig. 123 — Representative noise performance of the CA3004, CA3005, or CA3006 operated in a differential-amplifier configuration (operating mode D).

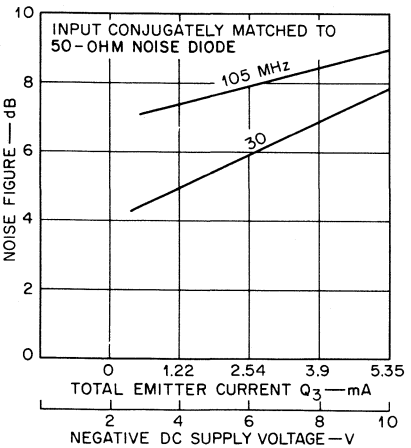


Fig. 124 — Representative noise performance of the CA3005 or CA3006 operated in a cascode configuration (operating mode D).

timum over-all noise figure by considering the gain and noise figure of the first stage and the noise figure of the second stage. The operating-current adjustment can be accomplished by a change in the negative-supply voltage (V^-) or by means of the bias connections that are available.

Fig. 125 shows the noise figure as a function of the source resistance R_S for a CA3005 or CA3006 used as a differential amplifier at an operating frequency of 12 MHz. The equation given in the figure can be used to predict noise performance as a function of source resistance for dc operating conditions. The load resistor R_L of the circuit is 2200 ohms, and the equivalent noise resistance R_N is 800 ohms.

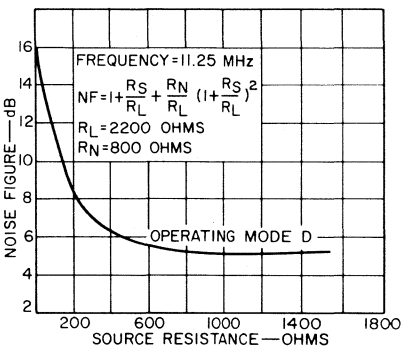


Fig. 125 — Noise figure of the CA3005 or CA3006 in a differential-amplifier configuration as a function of source resistance (operating mode D).

Gain Control—The gain of the CA3004, CA3005, and CA3006 circuits may be controlled in either of two ways: (1) the negative voltage applied to the base-bias resistor R1 can be adjusted to vary the current in transistor Q3, or (2) a differential offset voltage can be applied to transistors Q1 and Q2. In both techniques, the gain-control voltage has a ground reference in a two-supply system, and maximum gain is obtained at zero volts. The first method provides greater gain-control range but also requires more control voltage than the second method. Figs. 126 and 127 show the typical gain control as a function of voltage for the CA3005 or CA3006 for the two methods. Fig. 126 gives the

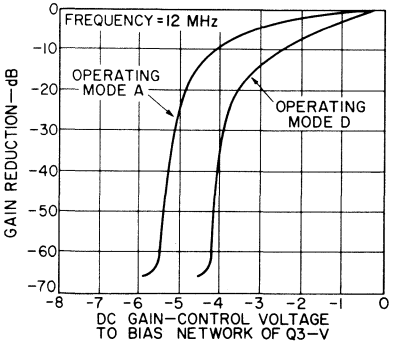


Fig. 126 — Gain-control characteristics of the CA3005 or CA3006 as a function of the dc gain-control voltage applied to the bias network of the constant-source transistor Q3.

gain-control characteristic for the CA3005 or CA3006 when the gain-control voltage is applied to the base-bias network of transistor Q3. Since the Q3 bias networks are the same, the gain characteristics for the CA3004 are nearly the same as those for the CA3005 and CA3006. Fig. 127 shows that in the offset method of gain control the gain range is dependent on the polarity of drive. For maximum gain-control range on a single-ended amplifier, the common-collector transistor should be cut off (negative voltage applied to its base). Because of the emitter resistors, R6 and R7, the CA3004 circuit will require more dc voltage for the same gain reduction as the CA3005 or CA3006, and the dc voltage required will be a function of the initial operating current.

The maximum gain-control range that can be provided by a reduction in the current of transistor Q3 varies with frequency, as shown in Fig. 128. The maximum gain-control range that can be obtained depends on the full gain used, the circuit loading, and the external-circuit layout.

A large part of the variation in the maximum gain control for the different circuits results from differences in the initial gain of the various circuits. Capacitive feedthrough appears less for the cascode than for the differential-amplifier configuration.

In the CA3028A, CA3028B, or CA3053 gain control is achieved by application of a positive voltage to the base (terminal 7) of the constant-current-source transistor Q3. A CA3028A or CA3028B operated in a differential-amplifier configuration, such as that shown in Fig. 118(a), can provide linear operation over a very wide input range with an agc

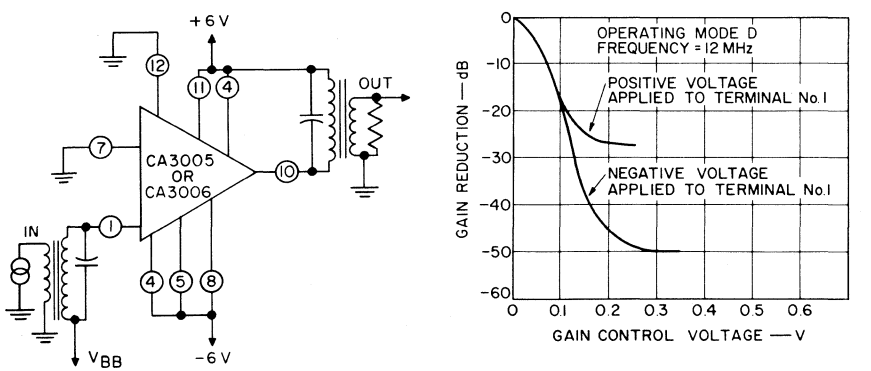


Fig. 127 — Gain-control characteristics of the CA3005 or CA3006 as a function of the dc offset voltage V_{BB} applied to the differential pair of transistors Q1 and Q2.

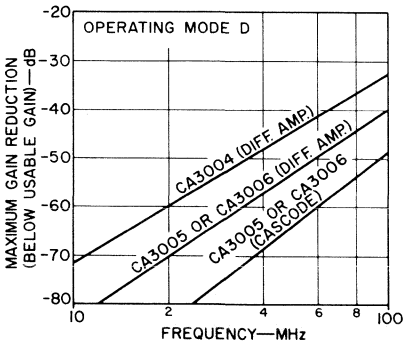
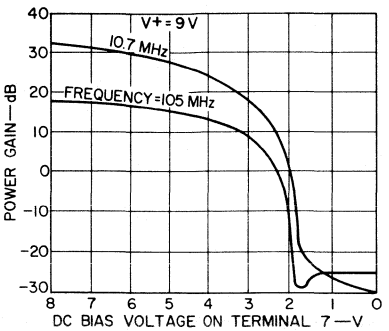


Fig. 128 — Maximum gain control provided by variations in the current through constant-source transistor Q3 as a function of frequency.

voltage applied to terminal 7. As shown in Fig. 129(a), the CA3028A or CA3028B operated in a differential-amplifier circuit has a gain-control capability of −60 dB at 10.7 MHz and of −46 dB at 100 MHz. Fig. 129(b) shows the power gain and noise figure of the circuit as a function of agc voltage. The combination of an optimum noise figure of 5.5 dB and a power gain of 15 dB at 100 MHz makes this circuit suitable for use as an rf amplifier in the commercial FM band.



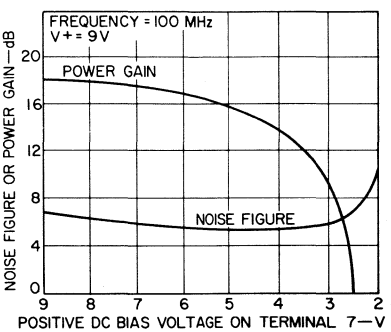


Fig. 129 — AGC characteristics of the CA3028A operated in a differential-amplifier configuration: (a) power gain as a function of agc voltage at 10.7 and 105 MHz; (b) power gain and noise figure as a function of agc voltage at 100 MHz.

Limiter Characteristics—The following paragraphs describe the limiter characteristics of the integrated-circuit rf amplifiers in both differential-amplifier and cascode configurations. (When the CA3028A, CA3028B, or CA3053 is used for limiting, it should be operated in the differential-amplifier configuration.)

Differential-Amplifier Configuration — The differential-amplifier, driven by a constant-current transistor, is probably the optimum circuit configuration for bipolar-transistor limiters. The advantage of such circuits in limiter applications is that collector saturation of either transistor Q1 or Q2 can be avoided because of the action of the constant-current transistor Q3. Figs. 115 and 116 show typical limiting characteristics for the CA3004 and for the CA3005 and CA3006, respectively. Fig. 130 shows the limiting characteristics for the CA3028A, CA3028B, and CA3053. For the CA3005, CA3006, CA3028A, CA3028B, and CA3053 (no emitter degeneration), "hard" limiting is achieved for a peak-to-peak input of 300 millivolts for all values of total dc current (I_{CC}). For the CA3004, the input voltage re-

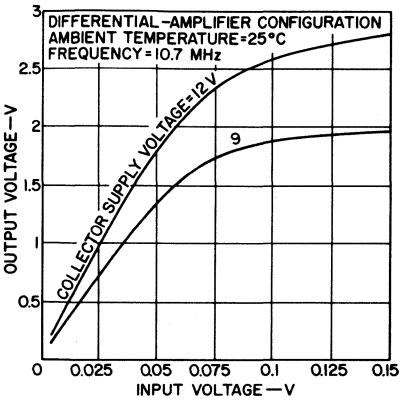


Fig. 130 — Limiting characteristics of the CA3028A operated in a differential-amplifier configuration.

quired for "hard" limiting is a function of I_{CC} because of the linearizing effect of the degenerative emitter resistors R6 and R7. As saturation must be prevented for good limiting, a maximum load resistor and low-level voltage gain exist for a given I_{CC} and positive supply voltage. Table XVII shows the maximum resistor values and voltage gains usable for $V^+ = 6$ volts, for the CA3004, CA3005, and CA3006. Table XVIII shows the maximum permissible load resistance for nonsaturating operation of the CA3028A, CA3028B, and CA3053 when single supply voltages of 9 or 12 volts are used. The low-level transconductance can be obtained from the slope near the origin for the curves shown in Figs. 115 and 116. The maximum voltage gain is independent of I_{CC} in the CA3005 and CA3006 and is dependent on I_{CC} in the CA3004.

Table XVII — *Limiter Performance of a CA3004, CA3005, or CA3006 Differential-Amplifier Circuit*

Supply Volts	$I_{C_1} + I_{C_2}$ (mA)	Max. Resistive Load (ohms)	Max. Tuned Load (ohms)	Voltage Gain With Emitter Degeneration (dB)		Voltage Gain Without Emitter Degeneration (dB)	
				Resistive Load	Tuned Load	Resistive Load	Tuned Load
6	0.5	12000	24000	31	37	35	41
6	1.0	6000	12000	28	34	35	41
6	2.0	3000	6000	25	31	35	41
6	3.0	2000	4000	22	28	35	41

$R_L = \frac{V_{supply}}{I_{C_1} + I_{C_2}}$ Resistive Load; $R_L = \frac{2\,V_{supply}}{I_{C_1} + I_{C_2}}$ Tuned Load; $g_m R_L$ = voltage gain

Table XVIII — *Maximum Load Resistance Permissible for Non-Saturating Operation of the CA3028A, CA3028B, or CA3053 with +9- and +12-Volt Single-Supply Voltages*

Supply Volts	$I_{C1} + I_{C2}$ (mA)	Maximum Tuned Load (ohms)	Maximum Resistive Load (ohms)
+9	5.0	3600	1800
+12	6.8	3500	1700

$R_L = V_{supply}/I_{C1} + I_{C2}$ for a resistive load
$R_L = 2V_{supply}/I_{C1} + I_{C2}$ for a tuned load

When the differential amplifier is used for limiting, the emitter-to-base breakdown voltage for transistors Q1 and Q2 cannot be exceeded without degradation in performance. For the CA3004, CA3005, and CA3006, this voltage including a safety margin should not exceed 2.5 volts rms. Either of two methods may be used to prevent this value being exceeded: (1) make sure the preceding stage limits before the input voltage reaches 2.5 volts (maximum voltage gain per stage approximately 20 dB), or (2) add one junction diode (D1), as shown in Fig. 131 (this addition allows a maximum usable voltage gain consistent with good limiting and stability).

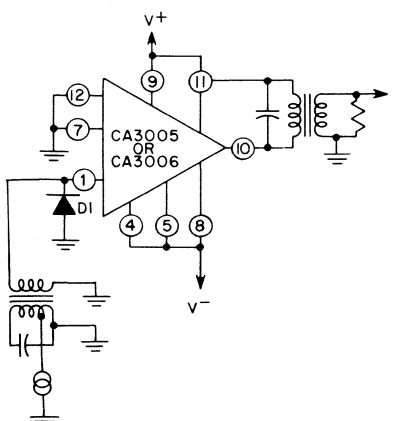


Fig. 131 — CA3005 or CA3006 differential-amplifier limiter that uses a diode to provide overload protection.

Cascode Amplifier—The limiting characteristics of the CA3005 or CA3006, when used as a cascode amplifier, are dependent on the current limiting in transistor Q3 or the voltage limiting of transistor Q1 (high-impedance output load). Limiting characteristics for both cases are shown in Figs. 132 and 133. The data in Fig. 132 are obtained with a collector load of 500 ohms. This limiting characteristic is "soft" and is acceptable over only a 20-dB range. The peak-to-peak voltage at the collector is never large enough to cause saturation. The

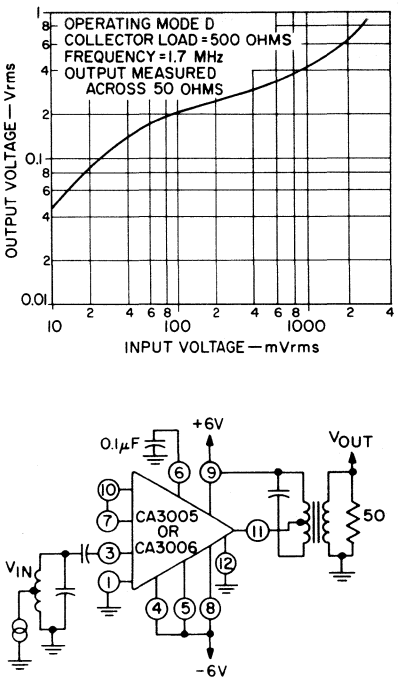
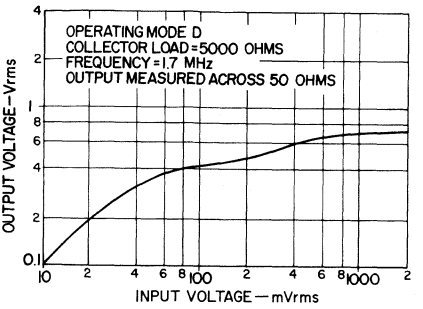


Fig. 132 — Limiting characteristics and circuit diagram of a CA3005 or CA3006 cascode limiter having a 500-ohm collector load impedance.

limiting characteristic shown in Fig. 133 is obtained with a collector load of 5000 ohms, and saturation of transistor Q1 occurs. The limiting is "harder" and covers a broader range, but severe tuned-circuit loading occurs.



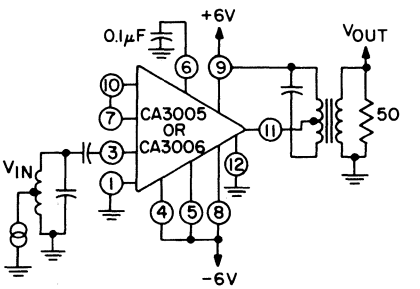


Fig. 133 — Limiting characteristics and circuit diagram of a CA3005 or CA3006 cascode limiter having a 5000-ohm collector load impedance.

RF- and IF-Amplifier Capabilities

The typical applications described in the following paragraphs illustrate the use of the integrated-circuit rf amplifiers in both the differential and cascode modes.

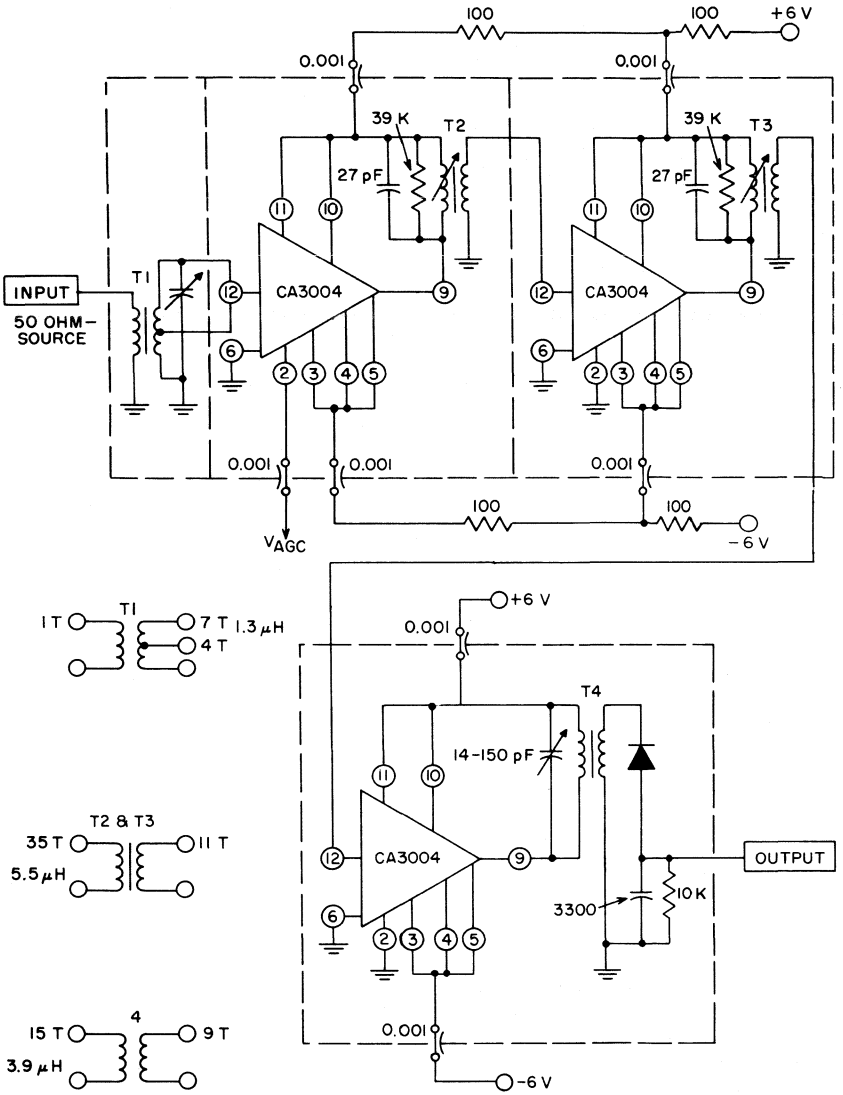
12-MHz IF Amplifier for AM Receiver—Fig. 134 illustrates the use of CA3004 integrated circuits in an if amplifier for an AM receiver. The amplifier is encased in a metal box, and adequate shielding and supply decoupling are provided. The if amplifier uses three CA3004 circuits and is designed to provide a stage gain of 25 dB. The source resistance to the input circuit was chosen as 800 ohms as a satisfactory compromise for gain, noise figure, and modulation-distortion performance. The input and output transformers, T1 and T4, have high unloaded Q's (200) to preserve good noise performance and to maximize the output power. The interstage transformers, T2 and T3, have low unloaded Q's (37) to achieve the required gain. The second detector has a 3-dB bandwidth of 5.0 kHz. Typical over-all performance characteristics are as follows:

Power drain = 83 milliwatts
Power gain (to second-detector input) = 76 dB
AGC range (1st stage) = 60 dB
Noise figure = 4.5 dB
3-dB bandwidth = 160 kHz

The signal-to-noise ratio of the circuit as a function of the input is shown in Fig. 135, and the frequency-response characteristic is shown in Fig. 136.

12-MHz Limiting IF Amplifier for FM Receiver—Fig. 137 shows the schematic diagram for a 12-MHz limiting if amplifier intended for FM applications. This circuit is housed in a metal box, with each stage well shielded and adequately decoupled from the dc power supply.

The amplifier uses three CA3005 (or CA3006) circuits and is designed to provide a gain per stage of 26 dB. At this gain per stage, diodes are required at the input to prevent base-to-emitter breakdown. For operation as a low-level limiter, the circuit input is matched, and the required gain fixes the unloaded Q of the



Transformers T1 and T4 are Ferramac* Q-2 Toroid Types (unloaded Q = 200).

Transformers T2 and T3 are slug-tuned with carbonyl IT-71 material▲ (unloaded Q = 70).

* Tradename of Indiana General Corporation, Keasbey, N. J.

▲ Manufactured by Magnetic Metals Co., Camden, N. J.

All resistance values in ohms unless otherwise specified.

Fig. 134 — Three-stage, 12-MHz, gain-controlled AM amplifier that uses CA3004 circuits in operating mode D.

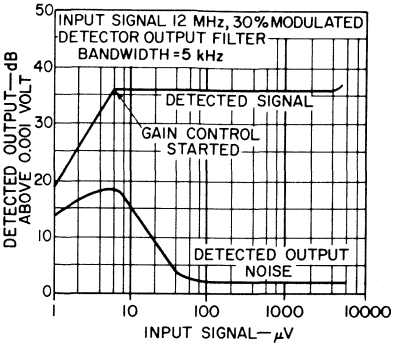


Fig. 135 — Output signal-to-noise ratio as a function of the input signal for the 12-MHz gain-controlled amplifier shown in Fig. 134 when gain control is used in only the first stage.

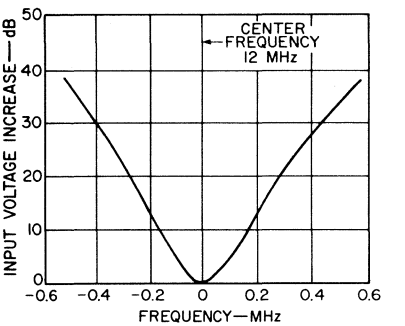


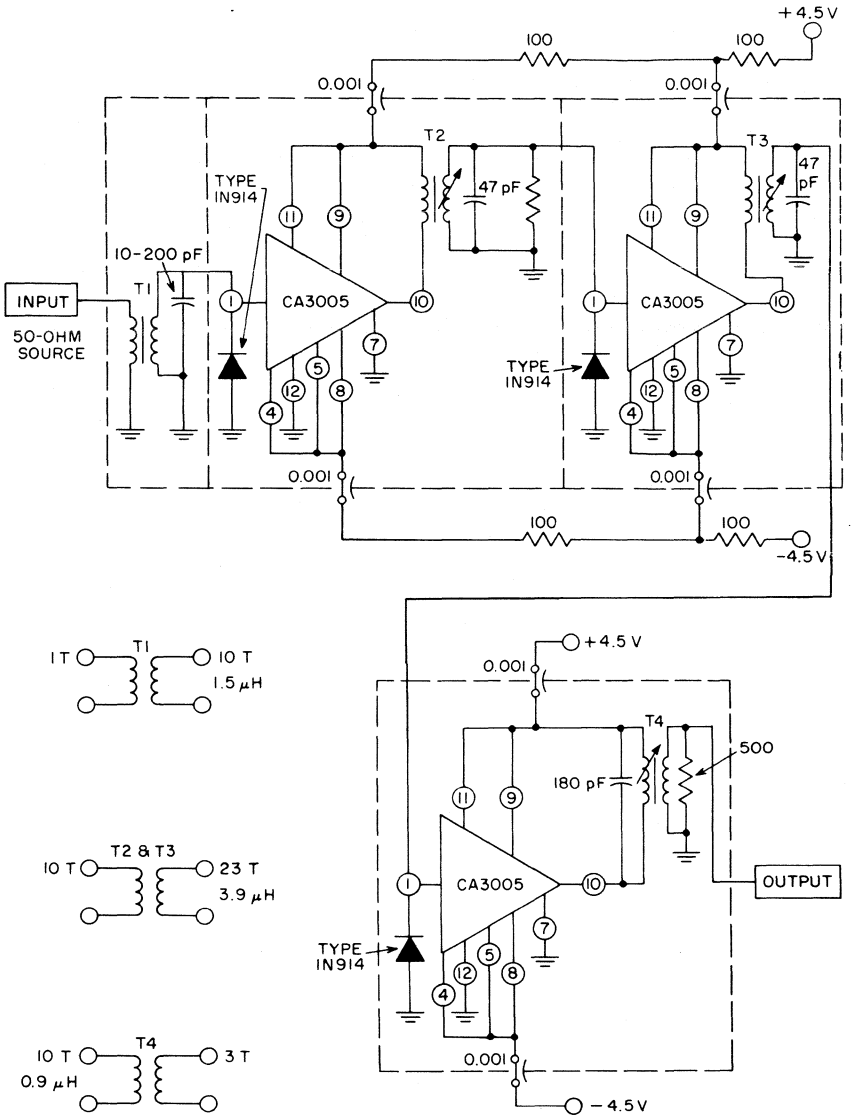
Fig. 136 — Frequency-response characteristics of the 12-MHz gain-controlled amplifier shown in Fig. 134.

tuned circuit and the collector load. Good noise performance for the first stage is obtained by the use of a high-Q (200) toroid inductor for input transformer T1. The other transformers are slug-tuned and have relatively low unloaded Q's (70 to 100), which contribute the necessary insertion loss for the required gain. A lower unloaded Q is required for transformer T2, so 10,000 ohms of resistance is added in parallel with this transformer. Little or no skew is detectable in the response characteristic for this circuit, shown in Fig. 138. The limiting characteristic of the circuit is shown in Fig. 139. Other typical over-all performance characteristics are:

Total power drain = 48 milliwatts
Over-all power gain = 77 dB
3-dB bandwidth = 300 kHz
Input limiting level = 30 microvolts.
Noise figure = 4 dB

10.7-MHz Cascode IF Amplifier— Fig. 140 shows an FM if strip in which the CA3028A is used in a high-gain, high-performance cascode configuration in conjunction with a CA3012 integrated-circuit wide-band amplifier. (The CA3012 circuit is discussed in detail in the section on **Special-Purpose Circuits.)** The CA3012 is used in the last stage because of the high gain of 74 dB it provides at the input to the 4000-ohm-load ratio-detector transformer T4. An input of approximately 400 microvolts is required at the base of the CA3012 for −3 dB below full limiting. An impedance-transfer device and filter must be connected between the CA3012 base (terminal 1) and the output of the CA3028A (terminal 6). The insertion loss of this filter should be kept near 6 dB (1:2 ratio of loaded to unloaded Q) so that all possible gain can be realized up to the CA3012 base. In addition to this insertion loss, a voltage step-down loss of 5.8 dB in the interstage filter is unavoidable. Therefore, the total voltage loss is approximately 9 to 14 dB, and an output of 1500 to 2000 microvolts must be available from the CA3028A to provide the required 400-microvolt input to the CA3012.

The voltage gain of the CA3028A into a 3000-ohm load is determined as follows:



Transformer T1 is a Ferramac* Q-2 Type (unloaded Q = 200). Transformers T2, T3, and T4 are slug-tuned with carbonyl IT-75▲ material (unloaded Q = 75).

* Tradename of Indiana General Corporation, Keasbey, N. J.
▲ Manufactured by Magnetic Metals Co., Camden, N. J.

All resistance values in ohms unless otherwise specified.

Fig. 137 — Three-stage, 12-MHz, gain-controlled AM amplifier that uses CA3005 circuits in operating mode D.

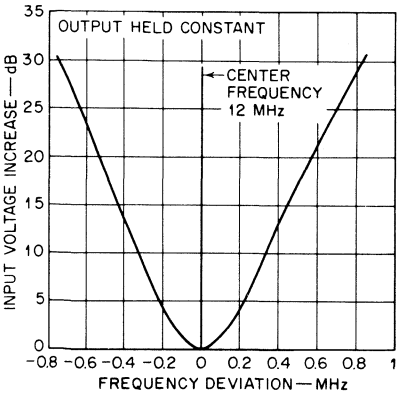


Fig. 138 — Frequency-response characteristics of the 12-MHz limiting amplifier shown in Fig. 137.

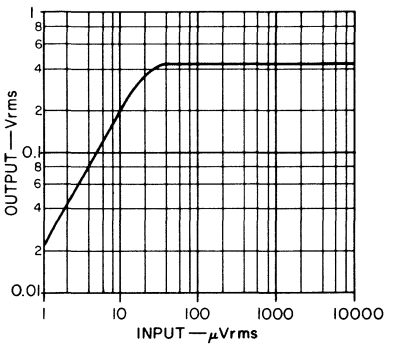


Fig. 139 — Limiting characteristics of the 12-MHz limiting amplifier shown in Fig. 137.

$$VG = \frac{-y_f}{y_o + y_L}$$

$$= \frac{100 \times 10^{-3}}{0.33 \times 10^{-3}}$$

$$= 300 = 49 \text{ dB}$$

This calculation indicates a sensitivity of 6.6 microvolts at the CA3028A base (terminal 2). This value cannot be realized, however, because the CA3012 limits on noise peaks so that the gain figure is reduced.

A sensitivity of 7.5 microvolts was realized in the amplifier shown in Fig. 140. The filter used with high-gain integrated circuits differs from that for single, cascaded transistor stages in that lumped selectivity is required rather than distributed selectivity.

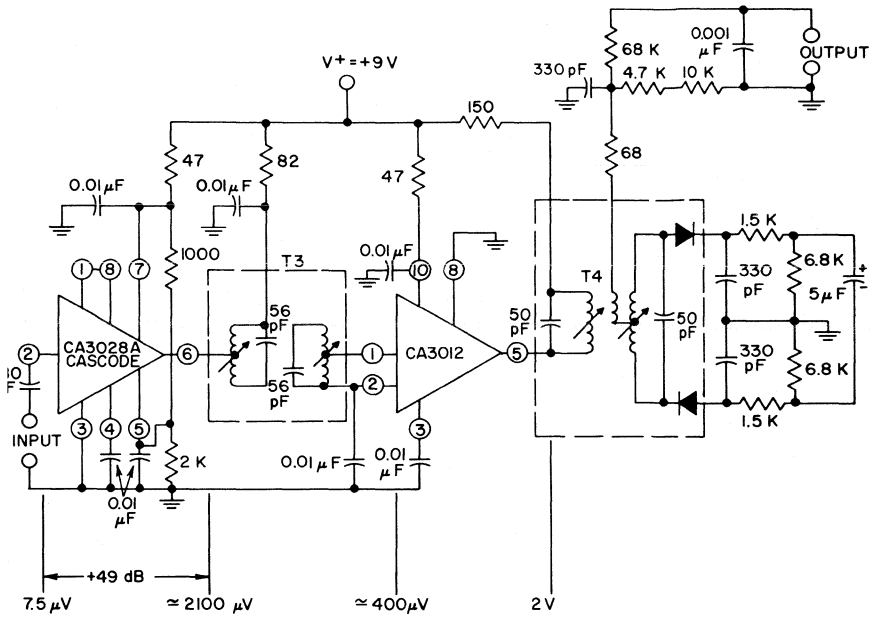
Special care must be exercised when second-channel attenuation in the order of 45 dB is required. Selectivity is then proportioned as follows:

Interstage filter: double-tuned; bandwidth, 220 kHz at −3 dB; coefficient of critical coupling, 0.7; voltage loss, 8 dB

Converter filter: triple-tuned; bandwidth, 220 kHz at −3 dB; coefficient of critical coupling, 0.8; voltage loss, about 28 dB

Because of input limiting in the CA3012, the interstage filter exhibits a somewhat wider bandwidth than the 220 kHz indicated. Therefore, a coefficient of critical coupling near 0.8 is realized, which is optimum for minimum deviation from constant time delay. The triple-tuned converter filter alone provides second-channel attenuation of 30 to 33 dB, while the interstage filter contributes 8 to 10 dB. The filters described meet requirements of both performance and economy.

The large collector swing that can be obtained in cascode operation of the CA3028A makes it desirable to take the agc voltage from the collector (terminal 6) or "hot" end of the if transformer for front-end gain control. The cascode stage then operates primarily in its linear region, and excellent selectivity (40 dB) is maintained even for large signal inputs of approximately 0.4 volt. Front-end gain reduction is between 40 and 50 dB.



T3 = Interstage transformer, TRW No. 22486 or equiv.
T4 = Ratio-detector transformer, TRW No. 22516 or equiv.
Audio Output = 155 mV rms for 7.5 μV ± 75 kHz input 3 dB below knee of transfer characteristic.

All resistance values in ohms unless otherwise specified.

Fig. 140 — 10.7-MHz if amplifier using a CA3028A in a cascode configuration.

10.7-MHz Differential-Amplifier IF Strip—Fig. 141 shows a 10.7-MHz medium-gain if strip consisting of a CA3028A connected as a differential amplifier and a CA3012 wideband amplifier. An input of approximately 1500 microvolts is required to the interstage filter. The differential-mode voltage gain of the CA3028A into a 3000-ohm load is determined as follows:

$$VG = \frac{y_f}{y_o + y_L}$$

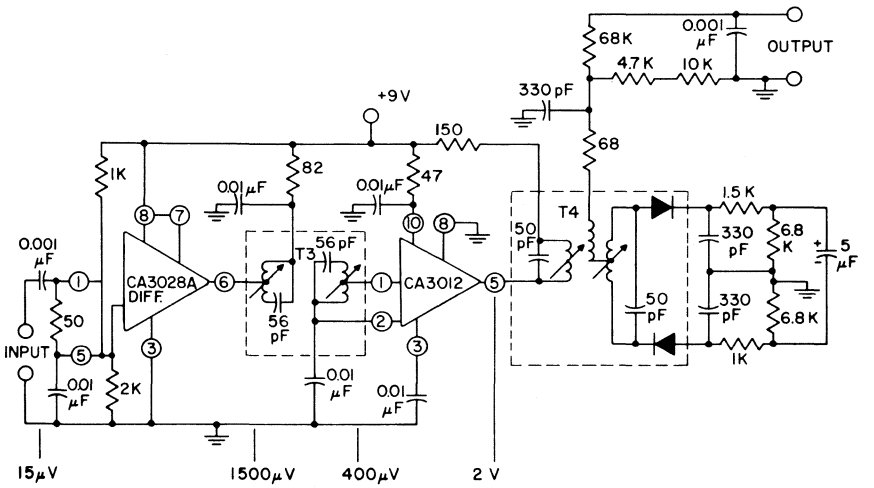
$$= \frac{0.38 \times 10^{-3}}{35 \times 10^{-3}}$$

$$= 92.5 = 39.3 \text{ dB}$$

This voltage gain requires that an input of approximately 15 microvolts be available at the base of the CA3028A differential amplifier.

Even if a triple-tuned filter having a voltage insertion loss of 28 dB is used in a low-gain front end, a receiver having an IHFM * sensitivity of 5 microvolts results. If 26-dB second-channel attenuation is permissible, a 3-microvolt-sensitivity IHFM receiver can be realized.

* Rating based on Institute of High Fidelity Manufacturer's standard No. 1HF-A-201 (1966).



T3 = Interstage transformer, TRW No. 22486 or equiv.
T4 = Ratio-detector transformer, TRW No. 22516 or equiv.
Audio Output = 155 mV rms for 15 μV ± 75 kHz input 3 dB below knee of transfer characteristic.

All resistance values in ohms unless otherwise specified.

Fig. 141 — 10.7-MHz if strip using a CA3028A in a differential-amplifier configuration.

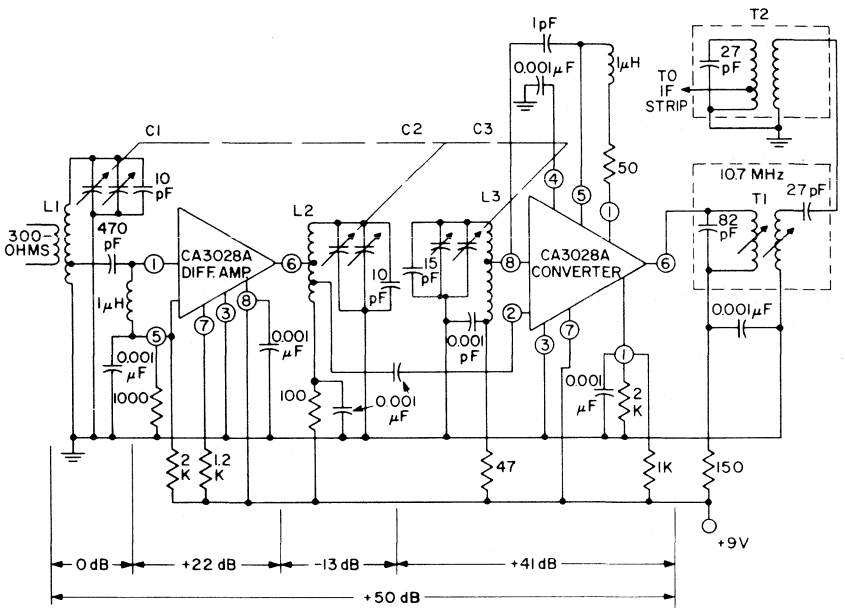
88-MHz-to-108-MHz FM Front End—Fig. 142 illustrates the use of the CA3028A as an rf amplifier and a converter in an 88-to-108-MHz FM front end. For best noise performance, the differential mode is used, and the base of the constant-current-source transistor Q3 is biased for a power gain of 15 dB. The rf amplifier input circuit is adjusted for an insertion loss of 2 dB to keep the noise figure of the front end low. Because the insertion loss of the input transformer adds directly to the integrated-circuit noise figure of 5.5 dB, the noise figure for the front end alone is 7.5 dB, as compared to noise figures of about 6 dB for commercial FM tuners.

Although a single-tuned circuit may be used between the output of the rf-amplifier stage and the input of the converter stage, a double-tuned circuit (as shown) is preferred to reduce spurious response of the converter. If the double-tuned circuit is critically coupled for the same 3-dB bandwidth as the single-tuned circuit, the insertion loss remains the same.

The output (collector) of the rf stage is tapped down on the interstage coil at approximately 1500 ohms, and the input (base) of the converter stage at 150 ohms. RF voltage gain is computed as follows:

Antenna to base	0 dB
Base to collector	22 dB
Voltage insertion loss of interstage coil	−13 dB
Net rf voltage gain	9 dB

If an if converter transformer having an impedance of 10,000 ohms is used, the calculated voltage conversion gain is



C1, C2, C3 = Variable capacitor, $\Delta C \approx 15$ pF
L1 = 3-3/4 turns of No. 18 tinned copper wire; winding length 5/16" on 9/32" form; tapped at 1-3/4 turns; primary — 2 turns No. 30 SE
L2 = 3-3/4 turns of No. 18 tinned copper wire; winding length 5/16" on 9/32" form; tapped at 2-1/4 turns, and 3/4 turn
L3 = 3-1/2 turns of No. 18 tinned copper wire; winding length 5/16" on 9/32" form
T1 = Mixer transformer, TRW No. 22484 or equiv.
T2 = Input transformer, TRW No. 22485 or equiv.

All resistance values in ohms unless otherwise specified.

Fig. 142 — 88-MHz-to-108-MHz front-end circuit for an FM receiver.

$$VG_C = \frac{y_f}{y_o + y_L}$$
$$= 112 = 41.3 \text{ dB}$$

Measured gain into the collector of the converter is 42 dB. The measured voltage gain of the rf amplifier and converter into a 10,000-ohm load is 52 dB; calculated gain is 50 dB. When the converter is tuned for the commercial FM band (88 to 108 MHz), the following parameters apply:

Input resistance R_{in}	170	ohms
Input capacitance C_{in}	6.3	pF
Output resistance R_{out}	80	K ohms
Output capacitance C_{out}	3.5	pF
Conversion transconductance	13	mmhos

The rf amplifier and converter shown in Fig. 142 were combined

with the if amplifier shown in Fig. 140, and the following performance data were measured at 100 MHz:

30-dB (S + N)/N	
IHFM Sensitivity	3 μV
Image Rejection	46 dB

Receiver noise figure is the limiting factor that permits a sensitivity of only 3 microvolts to be realized.

Mixer Capabilities

The CA3004, CA3005, CA3006, CA3028A, and CA3028B integrated circuits may be used as mixers, modulators, and product detectors. The schematic diagram in Fig. 143 illustrates the use of the CA3005 or CA3006 in mixer applications. The oscillator input is injected at the base of transistor Q3. The rf input is injected single- or double-ended to the bases of transistors Q1 and Q2. The use of a center-tapped inductor for the output tuned circuit (double-ended) allows the common-mode signal of the oscillator to be balanced out so that the oscillator will not overload subsequent stages, and provides carrier suppression for modulators.

The gain performance and generation of harmonics in the CA3004, CA3005, CA3006, CA3028A, and CA3028B mixer circuits are dependent on the amplitude of the oscillator drive signal and the dc bias. The expression for product detection or frequency multiplication in the CA3005 or CA3006 (consult Fig. 144) is determined as follows:

$$e_o = e_1 \, g_m \, Z_L$$

where e_o is the output voltage, e_1 is the differential input voltage, g_m is the transconductance of the differential pair of transistors (Q1 and Q2), and Z_L is the load impedance (total between collectors). For a balanced circuit, the transconductance is given by

$$g_m = \frac{\alpha q}{2KT} \; I_o$$

where q is the electron charge, K is Boltzmann's constant, and T is temperature in degrees Kelvin. The term I_o represents the collector current of transistor Q3 and may be expressed as

$$I_o = g_{m2} \, e_2$$

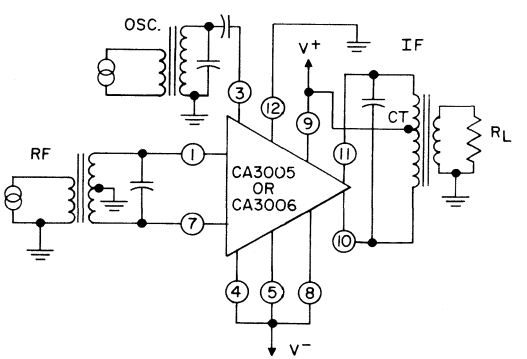


Fig. 143 — Circuit diagram for use of the CA3005 or CA3006 as a mixer (operating mode D).

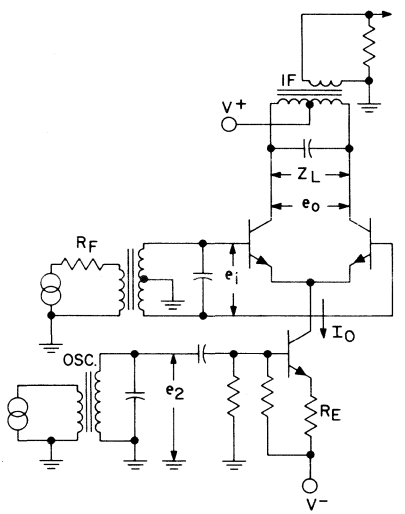


Fig. 144 — Circuit diagram of a CA3005 or CA3006 balanced mixer (operating mode D). The equations for product detection or multiplication are based on this circuit.

where g_{m2} is the transconductance of transistor Q3 and e_2 is the input voltage applied to transistor Q3. The output voltage, e_o, therefore, is given by the following equation:

$$e_o = \frac{\alpha q}{2KT} e_1 e_2 g_{m2} Z_L$$

This equation is a general expression for the output voltage of the mixer having input signals e_1 and e_2. With emitter degeneration in the constant-current transistor (Q3), g_{m2} is essentially constant for a sufficiently large emitter current (greater than 1 milliampere); the current I_o, therefore, follows the applied voltage e_2.

When e_1 and e_2 are sinusoidal and g_m is constant, the input signal voltages are given as follows:

$$e_1 = E_1 e^{j\omega_1 t} + \overset{*}{E}_1 e^{-j\omega_1 t}$$

$$e_2 = E_2 e^{j\omega_2 t} + \overset{*}{E}_2 e^{-j\omega_2 t}$$

($\overset{*}{E}_1$ is the conjugate of E_1, and $\overset{*}{E}_2$ is the conjugate of E_2.)

With the substitution of these relationships, the equation for the output voltage for the CA3005 or CA3006 then becomes

$$e_o = \frac{\alpha q}{2KT} g_{m2} Z_L [E_1 E_2 e^{j(\omega_1 + \omega_2)t} + \overset{*}{E}_1 \overset{*}{E}_2 e^{-j(\omega_1 + \omega_2)t}] + \frac{\alpha q}{2KT} g_{m2} Z_L [\overset{*}{E}_1 \overset{*}{E}_2 e^{j(\omega_1 - \omega_2)t} + E_1 \overset{*}{E}_2 e^{-j(\omega_1 - \omega_2)t}]$$

The equation above gives the output voltage for a CA3005 or CA3006 used as a product detector or multiplier. (It should be noted that only the two sideband frequencies are included in the output.) The requirements for product detectors or multipliers are that the circuit should be biased in a linear region with a small signal voltage applied. Because $\alpha q g_{m2}/2KT$ is essentially constant, the gain of the mixer is determined from Z_L and the $e_1 e_2$ product. The linearity of the CA3006 is illustrated by the curve of the conversion transconductance as a function of the oscillator voltage, shown in Fig. 145. (Although the curve is plotted on logarithmic scales because of the wide range, the relationship is linear.) The gain reaches a maximum value at approximately 2.5 volts rms. Because measurement inaccuracies prevent the use of this curve to determine harmonic generation, spurious-signal measurements were taken on CA3005 and CA3006 mixer circuits. For these measurements, the

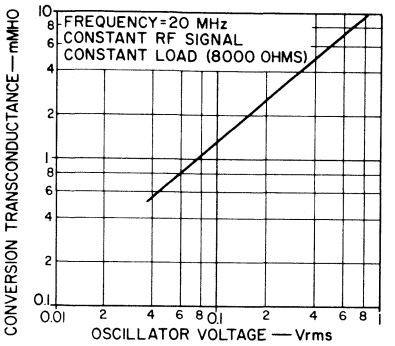


Fig. 145 — Conversion gain of a CA3005 or CA3006 mixer circuit as a function of oscillator voltage.

rf input was untuned and the oscillator and if frequencies were held constant. For a fixed amplitude of oscillator injection on terminal 3, the rf input signal was varied in frequency, and the amplitude of the responses was recorded. The results are shown in Table XIX. The spurious signals generated are a function of oscillator drive. A low oscillator drive (0.1 volt rms) produced only three spurious signals for which the rejection was less than 70 dB down.

These measurable spurious responses were third-order products that involved the second harmonic of either the oscillator or rf signal. The relative if gain increases with decreasing oscillator drive because of lower mixer gain.

The common-mode cancellation of the oscillator signal at the collector outputs is indicative of the carrier suppression that can be provided in modulators. The carrier suppression is a function of output tuned-circuit balance and the transistor offset voltage. The contribution of the offset is illustrated in Fig. 146, which

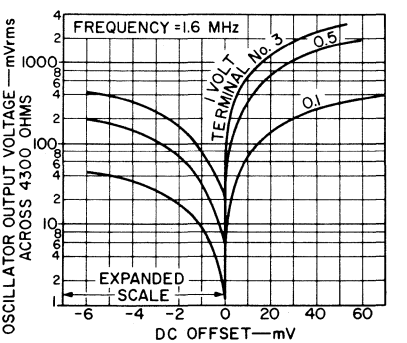


Fig. 146 — Cancellation of the oscillator signal at the output of a CA3005 or CA3006 mixer as a function of dc offset voltage.

Table XIX — *Response of a CA3005 or CA3006 Mixer to Spurious Harmonics*

Frequency	Signal Frequency f_x (MHz)	Difference-Frequency Output (dB relative to $f_o - f_x$) for V_{osc} (V rms) at Term. 3 of 1	0.7	0.3	0.1
$f_o - f_x$	1.0	0	0	0	0
f_{if}	0.659	7.5	10	18	27
$2f_x - f_o$	1.159	—53.1	—53.1	—54.9	—52.3
$2f_o - 2f_x$	1.329	—76.1	—	—	—
$2f_x - 2f_o$	1.988	—75.5	—	—	—
$f_x - f_o$	2.318	0	0	0	0
$2f_o - f_x$	2.659	—31.7	—35	—39.7	—47.8
$2f_x - 3f_o$	2.813	—79.6	—	—	—
$f_x - 2f_o$	3.977	—31.7	—35	—39.7	—47.8
$3f_o - f_x$	4.309	—35.8	—59.3	—74.7	—
$f_x - 3f_o$	5.627	—38.5	—57	—74	—
$4f_o - f_x$	5.977	—38.9	—63	—	—

f_o = 1.659 MHz; V_{osc} = oscillator injection voltage.

All blank spaces indicate difference-frequency output more than 70 dB below the $f_o - f_x$ output.

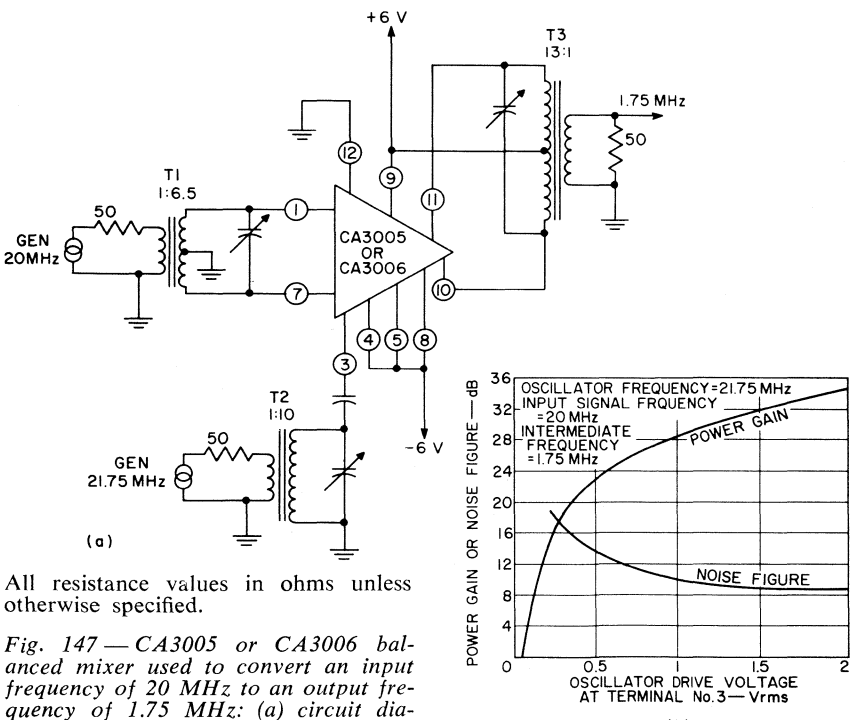
shows the output signal as a function of the offset voltage for the CA3005 or CA3006. These data were obtained on circuits operated with a balanced output tuned to the oscillator frequency.

Balanced Mixer—The use of the CA3005 or CA3006 as a balanced mixer to convert 20 MHz to 1.75 MHz is shown in Fig. 147(a). The input impedance of the CA3005 or CA3006 is typically 2200 ohms. The output load impedance between collectors is approximately 8000 ohms. The conversion power gain and noise figure as a function of the oscillator drive are shown in Fig. 147(b). Power gain increases and noise figure decreases with increases in oscillator drive.

Suppressed-Carrier Modulator and Product Detector—The CA3005 and CA3006 can be used in a suppressed-carrier double-sideband modulator and product detector. The double-sideband modulator is a convenient vehicle to evaluate carrier suppression and product detection. With the two circuits coupled together, the relation between modulation distortion and drive levels is readily established.

Feedback may cause oscillation or unbalance; care must, therefore, be taken in the external-circuit layout design. Shielding must also be provided for both the double-sideband modulator and the product detector.

The circuit diagram of the double-sideband modulator is shown in Fig. 148. The modulating signal is applied

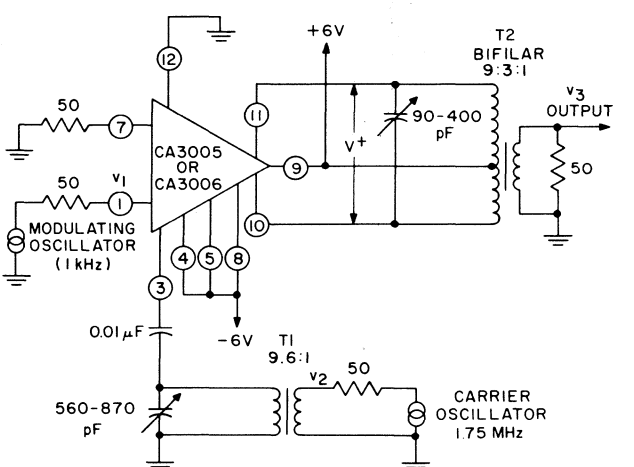


All resistance values in ohms unless otherwise specified.

Fig. 147 — CA3005 or CA3006 balanced mixer used to convert an input frequency of 20 MHz to an output frequency of 1.75 MHz: (a) circuit diagram; (b) conversion power gain and noise figure as a function of the oscillator drive voltage.

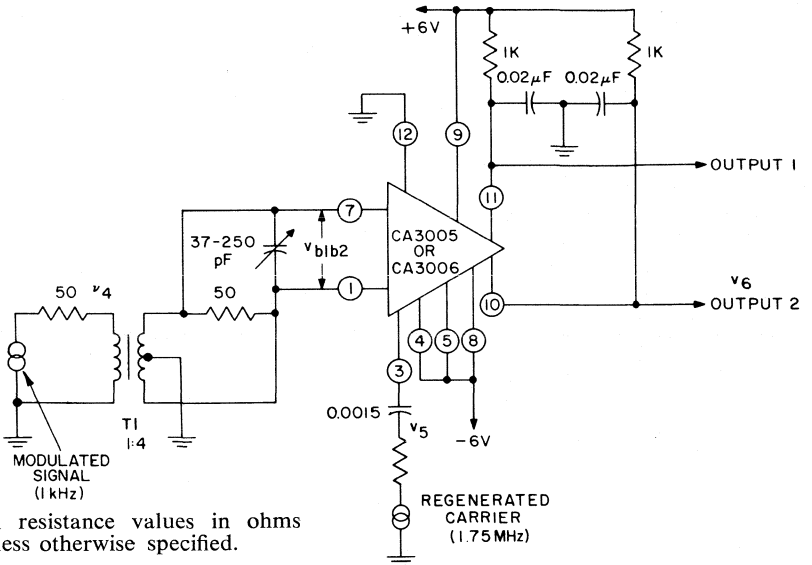
single-ended to the differential pair of transistors, Q1 and Q2, and the oscillator signal is applied to the base of transistor Q3. The output is taken double-ended from the balanced transformer, T2. The carrier suppression is a function of bilateral symmetry (offset, output-transformer balance, and modulation drive circuits) and the modulation-to-carrier drive ratio. With the external-circuit bilateral symmetry carefully preserved, the carrier output is approximately 25 dB below the double-sideband output for CA3006 units (offset $\leqq$ 1 millivolt) operated with a drive v_1 of 10 millivolts rms and v_2 of 31.5 millivolts rms. Although the signal-to-carrier ratio of 25 dB represents an inadequate rejection for most systems (40 to 60 dB is usually required), this value relaxes the filter requirements from those necessary on more commonly used single-sideband modulators. An improvement over the 25-dB ratio is obtained if the modulation drive v_1 is increased and the carrier drive v_2 is decreased, because the output is a function of the product of v_1 and v_2.

The circuit diagram for a product detector is shown in Fig. 149. The product detector, which provides the advantage of a double-ended out-of-phase output, is driven through a 50-ohm adjustable feed by the double-sideband signal from the modulator. The levels of v_1, v_2, v_4, and v_5 are altered to establish the relationship between the harmonic distortion and drive levels as well as gain values for typical operation. The results are shown in Table XX. Overdrive by the modulation (v_1) or the modulated signal (v_4) results in third-harmonic distortion of the detected signal. It should be noted that gain is a function of either the product of v_1 and v_2, or the product of v_4 and v_5.



All resistance values in ohms unless otherwise specified.

Fig. 148 — Double-sideband, suppressed-carrier modulator using the CA3005 or CA3006.



All resistance values in ohms unless otherwise specified.

Fig. 149 — Product detector using the CA3005 or CA3006.

Table XX — *Gain and Distortion as a Function of Different Drive Levels for a Double-Sideband Modulator and Product Detector Using the CA3006*

Variable	Term. 3	Voltages ▲ (mV rms) V_{CC}	v_s	$v_{b_1b_2}$	v_6	3rd Harmonic Distortion (dB below fundamental) *
v_1 varied, v_2 = 31.5 mV, v_4 = 1 mV, v_5 = 0.5 mV						
5	296	46	4.95	4	36	54
10	296	80	8.9	4	36	54
30	296	250	26.6	4	36	37.5
v_2 varied, v_1 = 10 mV, v_4 = 1 mV, v_5 = 0.5 mV						
31.5	296	83	8.9	4	36	54
100	960	262	28	4	36	51
315	2960	830	8.9	4	36	50
v_4 varied, v_1 = 10 mV, v_2 = 31.5 mV, v_5 = 0.5 mV						
0.5	296	83	8.9	2	17.5	54
1	296	83	8.9	4	36	52
3	296	83	8.9	12	110	47.5
5	296	83	8.9	20	188	37■
v_5 varied, v_1 = 10 mV, v_2 = 31.5 mV, v_4 = 1 mV						
0.315	296	83	8.9	4	23	54‡
0.5	296	83	8.9	4	36	54
1.0	296	83	8.9	4	86	50

▲ Explanation of voltage designations is provided by Figs. 148 and 149.
* 2nd, 4th, and 5th harmonics more than 60 dB down, except as noted.
■ 2nd harmonic 51 dB down; 5th harmonic 59 dB down.
‡ 2nd harmonic 56 dB down.

Video-Amplifier Capabilities

The CA3004, CA3005, and CA3006 integrated circuits may be used as video amplifiers, as shown in Figs. 150(a) and (b). A relatively large number of external components is required, and the availability of internal-circuit connections for these external components provides a large degree of flexibility to the user with respect to such factors as bandwidth, gain, power dissipation, and peaking. In the circuit shown in Fig. 150(a), R1 should be equal to R2 to preserve the circuit balance, and C2 should be an adequate bypass so that the noise factor and gain are not degraded. For the cascode configuration shown in Fig. 150(b), C2 is an emitter bypass, and its reactance should be less than 1.5 ohms at the lowest video frequency to be handled.

In either cascode or single-ended differential-amplifier configurations, the feedback is low. Each configuration provides good isolation from output to input; the high-frequency performance therefore can be approximated from the input and output parallel R and C for a single stage or from the total shunt R and C between stages for an iterative connection. The mid-frequency voltage gain can be computed from the familiar $g_m R_L$ product. As an aid to such calculations, Table XXI gives the input and output parallel R and C and the absolute values of g_m for the various circuits and configurations for operation at 1, 10, and 40 MHz. For more precise, but more elaborate calculations, the y parameters may be used for video-amplifier design.

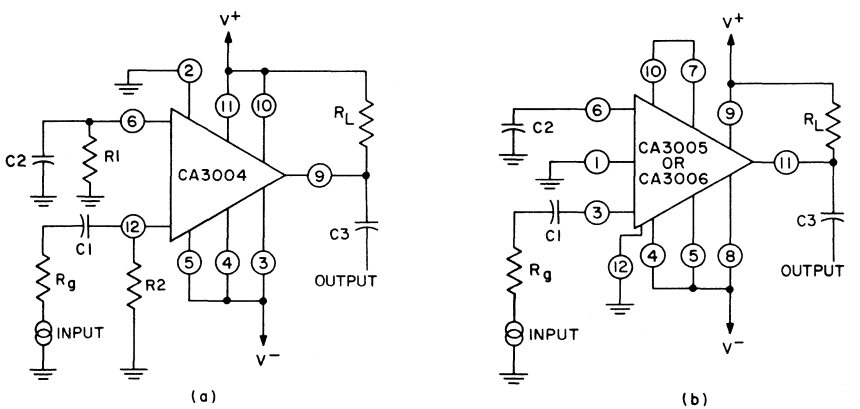


Fig. 150 — Video amplifiers using (a) the CA3004 in a differential amplifier configuration and (b) the CA3005 or CA3006 in a cascode configuration.

Table XXI — *Input and Output Parallel RC Network, Transconductance, and Video Performance Data for CA3004, CA3005, and CA3006 RF Amplifiers**

Frequency (MHz)	Input Parallel RC R_{in} (ohms)	Input Parallel RC C_{in} (pF)	Output Parallel RC R_{out} (ohms)	Output Parallel RC C_{out} (pF)	Transconductance g_m (mmhos)
CA3005 or CA3006 Cascode Operation					
1	500	42	-1.67×10^6	3	78
10	500	42	-1.67×10^6	3	77
40	180	22	-6×10^5	3	58
CA3005 or CA3006 Differential-Amplifier Operation					
1	2500	16	10^5	4	20
10	1800	13	4×10^4	4	20
40	670	10.5	2800	7.6	18.6
CA3004 Differential-Amplifier Operation					
1	6650	8	1.7×10^5	6.5	7.8
10	6650	6.2	10^5	6.1	7.8
40	2000	5	2×10^4	6.8	7.6

Video Performance (Simulated Iterative Connection)

Type	Operation	Interstage R_L (ohms)	High-Frequency 3-dB Point (MHz) Meas.	High-Frequency 3-dB Point (MHz) Calc.	Mid-Band Voltage Gain (dB) Meas.	Mid-Band Voltage Gain (dB) Calc.
CA3005 or CA3006	Cascode Differ. Ampl.	150	23	20	19.3	20.6
CA3005 or CA3006	Differ. Ampl.	500	18	16	19.5	20.0
CA3004	Differ. Ampl.	1000	18.4	15	17.2	18.0

* Data obtained for circuits operated from ±6-volt dc supplies in operating mode D.

Operational Voltage Amplifiers

The term "operational amplifier" was originally intended to denote an amplifier circuit that performed various mathematical operations such as integration, differentiation, summation, and subtraction. The application of the operational amplifier, however, has been so vastly extended that today this term suggests a device that finds the widest use in such applications as signal amplification and wave shaping, servo and process controls, analog instrumentation and system design, impedance transformation, and many other routine functions. This versatile circuit may also be used in many nonlinear applications such as voltage comparators, analog-to-digital and digital-to-analog converters, logarithmic amplifiers, and nonlinear function generators.

The great versatility and many advantages of operational amplifiers stem from the use of negative feedback to control response characteristics. If the amplifier circuit provides sufficient gain, the closed-loop amplifier characteristics become a function of only the feedback components. The versatility in the application of the operational amplifier, therefore, is limited primarily by only the ingenuity of the circuit designer in the selection and arrangement of feedback components.

"IDEAL" OPERATIONAL AMPLIFIER

An ideal operational amplifier would have infinite open-loop gain and bandwidth, and zero noise, offset, and drift. Although no amplifier has these ideal qualities, practical integrated-circuit operational amplifiers are generally characterized by the following properties:

1. extremely high dc voltage gain, generally in the range from 10^3 to 10^6;
2. wide bandwidth that starts at dc and rolls off to unity gain at from one to several hundred megahertz with a slope of 6 dB per octave or at most 12 dB per octave;
3. positive and negative output voltage over a large dynamic range, usually from $\pm$ 10 to $\pm$ 100 volts;
4. very low input dc offset and drift with time and temperature;
5. high input impedance so that amplifier input current can be largely neglected.

Basic Configuration

The configuration most commonly used for operational voltage ampli-

fiers consists of one or two differential-amplifier circuits, together with an appropriate output stage. The differential-amplifier stages not only fulfill the operational-amplifier requirement for a high-gain direct-coupled amplifier circuit, but also provide significant advantages with respect to the application of the operational amplifier.

From an applications standpoint, the versatility of an operational amplifier that has a differential input is substantially greater than that of the single-input type of operational amplifier. The increased versatility of the differential-input operational amplifier results from the greater flexibility allowed in the selection of the feedback configuration. In the single-input operational amplifier, only the inverting type of feedback configuration can be employed. When differential inputs are employed, the operational amplifier may use either an inverting feedback configuration or a noninverting feedback configuration, which is dependent upon the common-mode rejection for its negative feedback. The characteristics of an operational amplifier may differ significantly depending upon the type of feedback used. The two types, therefore, tend to complement each other. Moreover, because the characteristics provided by each feedback configuration are required equally often, the differential-input operational amplifier is, from an applications standpoint, twice as versatile as the single-input operational amplifier.

The differential-input operational amplifier is readily adapted to integrated-circuit construction techniques. As pointed out in preceding sections, a differential-amplifier circuit is a stable dc-amplifier configuration that lends itself particularly well to the monolithic diffusion process used in the construction of silicon integrated circuits. In addition, symmetrical differential-amplifier stages can be dc-cascaded readily, provided that each succeeding stage is driven push-pull by the preceding stage. The common-mode effects that result from this arrangement make possible stable, direct-coupled cascades.

Basic Design Equations

The capabilities and limitations of operational amplifiers are firmly defined by a few simple "classical" design equations and rules based on a certain set of design criteria that any operational amplifier must meet. Effective use of these simple relationships, however, requires knowledge of the conditions for which each is applicable so that errors which may result from various approximations are held to a minimum. The precise formulations for the transfer functions, the input impedances, the output impedances, and the loop gains and the defining conditions used to derive the classical design equations have been published previously in many theoretical treatments of operational amplifiers. In the following paragraphs, precise relationships and the "classical" design equations for both the inverting- and noninverting-feedback configurations are briefly reviewed, and the effects of a finite load impedance and common-mode gain on each type of configuration are pointed out. No attempt is made to present rigorous derivations which are readily available from other sources. (RCA Application Note ICAN-5290, "Integrated-Circuit Operational Amplifiers," published by RCA Electronic Components, Harrison, N. J., provides detailed derivations of the design equations for differential-input operational amplifiers.)

Inverting Feedback Configuration—The basic design model for a differential-input operational amplifier operated with an inverting feedback configuration is shown in Fig. 151. The load resistor R_L is assumed to be large enough so that its effect on the transfer characteristic is negligible, i.e., $I_{OUT} = 0$. (The effects of a finite R_L are investigated and evaluated subsequently in the discussion of the **Equivalent-Circuit Model** of an operational amplifier.)

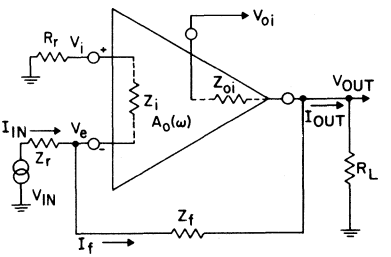


Fig. 151 — Inverting operational-amplifier configuration.

Certain differential-input operational amplifiers require a significant flow of bias current at each input. For this condition, the dc paths to ground for each input must be equal so that a minimum dc offset voltage (error) is developed at the output. Thus, for the terminology employed in Fig. 151, R_r must equal the parallel combination of $Z_r(\omega = 0)$ with the series combination of $Z_f(\omega = 0)$ and Z_{oi} $(\omega = 0)$.

In the circuit of Fig. 151, the drive-source impedance affects the feedback in the inverting configuration and, therefore, must be considered part of the Z_r term. For brevity, the symbol Z_r is defined to include the source impedance as well as certain feedback design elements. The impedances Z_i and Z_{oi} are the open-loop **intrinsic** input and output impedances of the operational amplifier. Ordinarily, these impedances are assumed in the amplifier symbol. In Fig. 151, however, they are identified to emphasize their importance. The term A_o (ω) is the **open-loop differential voltage gain** of the operational amplifier; this parameter is frequency-dependent. The terminals on the operational-amplifier symbol labeled minus (−) and plus (+) refer to the inverting and noninverting input, respectively. Table XXII lists the precise equations and the classical design approximations of these equations (for $R_L \rightarrow \infty$) for the inverting-feedback configuration of the differential-input operational amplifier.

Table XXII — *Basic Design Equations for an Operational Amplifier Operated in the Inverting-Feedback Configuration*

CLOSED-LOOP GAIN (Voltage Transfer Function)

Precise Equation:

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_{oi}(Z_i + R_r) - A_o(\omega)Z_iZ_f}{(Z_f + Z_{oi})(Z_i + R_r) + Z_r(Z_f + Z_{oi} + Z_i + R_r) + A_o(\omega)Z_iZ_r}$$

Classical Form: In the normal case, $A_o(\omega)$ is very large, Z_i is much greater than the equivalent value of Z_r in parallel with $Z_f + Z_{oi}$, and Z_{oi} is much smaller than Z_r. The precise equation for the closed-loop gain then simplifies to the following familiar expression:

$$\frac{V_{OUT}}{V_{IN}} \xrightarrow{A_o(\omega)\rightarrow\infty} -\frac{Z_f}{Z_r}$$

Table XXII — *Basic Design Equations for an Operational Amplifier Operated in the Inverting-Feedback Configuration (Cont.)*

LOOP GAIN (Ratio of Open-Loop Gain to Closed-Loop Gain)

Precise Equation:

$$LG = -\frac{Z_f + Z_r}{Z_f} - \frac{A_o(\omega)}{\frac{Z_f}{Z_r}}$$

Classical Form: When $A_o(\omega)$ is very large, the loop gain is essentially equal to this parameter divided by the ideal closed-loop gain, as follows:

$$LG \doteq \frac{-A_o(\omega)}{\frac{Z_f}{Z_r}}$$

INPUT IMPEDANCE

Precise Equation:

$$Z_{IN} = Z_r + \frac{(Z_f + Z_{oi})(Z_i + R_r)}{(Z_f + Z_{oi} + Z_i + R_r) + A_o(\omega)Z_i}$$

Classical Form: If it is assumed that $A_o(\omega)$ is very large, that Z_{oi} is very small, and that R_r is much smaller than Z_i (all of which are common conditions), the equation for the input impedance may be written in the following simplified form:

$$Z_{IN} \xrightarrow{A_o(\omega)\to\infty} Z_r$$

OUTPUT IMPEDANCE $[Z_{OUT} = V_{OUT}(R_L \to \infty)/I_{OUT}(R_L \to 0)]$

Precise Equation:

$$Z_{OUT} = \frac{Z_{oi}[Z_r(Z_f + Z_i + R_r) + Z_f(Z_i + R_r)][A_o(\omega)Z_iZ_f - Z_{oi}(Z_i + R_r)]}{A_o(\omega)Z_iZ_f[Z_r(Z_f + Z_{oi} + Z_i + R_r) + (Z_f + Z_{oi})(Z_i + R_r) + A_o(\omega)Z_iZ_r]}$$

Classical Form: If $A_o(\omega)$ is dominant, the above equation simplifies to

$$Z_{OUT} \doteq \frac{Z_{oi}[Z_r(Z_f + Z_i + R_r) + Z_f(Z_i + R_r)]}{A_o(\omega)Z_iZ_r}$$

The equation for the output impedance does not simplify to its classical form unless Z_i is also dominant. For this condition, the equation becomes

$$Z_{OUT} \doteq Z_{oi}\frac{1 + \frac{Z_f}{Z_r}}{A_o(\omega)}$$

The assumption that Z_i is a dominant term is not always valid, particularly when bipolar-transistor inputs are employed. The first simplification of the precise equation, therefore, takes precedence over the classical expression. A number of RCA integrated-circuit operational amplifiers have an intrinsic input impedance Z_i in the range from 1 to 10 megohms. For these circuits, the classical equation for the output impedance provides an excellent approximation of this parameter.

The transfer function, or **closed-loop gain,** of an operational voltage amplifier is generally considered to express the relationship between input and output voltages. (It is relatively simple to convert the voltage transfer function to another desired transfer relationship.) The classical equation for the closed-loop gain shows that the gain of the operational amplifier is essentially dependent upon only the feedback elements.

The ratio of the open-loop gain to the closed-loop gain is also an important design parameter. This "gain throwaway," which is known as the **loop gain** (LG), can be used to predict the accuracy of the classical approximations for the operational-amplifier design relationships. In general the higher the loop gain, the more accurate are the results provided by the classical approximations.

The precise and classical equations for the **input impedance** imply the existence of a virtual ground $V_e = 0$) at the inverting-input (−) terminal of operational amplifier. That is, the terminal is at ground potential even though there is no electrical connection between this nodal point and ground. [This statement can be verified intuitively by use of the classical expression or directly if $A_o(\omega)$ is assumed to be infinite in the precise equation.] Moreover, no current flows into the negative terminal of the amplifier when $A_o(\omega)$ is infinite, as indicated by the fact that the nodal-assigned voltage V_e is zero and the impedance at the negative terminal ($Z_i + R_r$) is not zero.

The **closed-loop output impedance** for an inverting-feedback operational amplifier is defined as the ratio of the unloaded output voltage to the short-circuit output current. Although this impedance is in no way indicative of the output-current capabilities of the amplifier, it is a useful small-signal parameter that can be employed to determine the gain reduction that results when the operational amplifier is operated into a finite load impedance, as pointed out subsequently in the discussion of the **Equivalent Circuit Model** for a differential-input operational amplifier.

Noninverting Feedback Configuration—Fig. 152 shows the general-circuit model for a differential-input

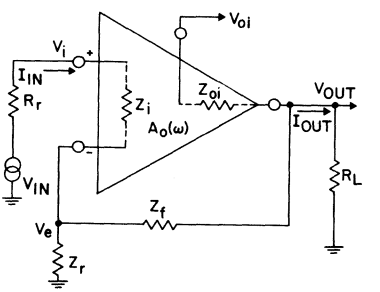


Fig. 152 — Noninverting operational-amplifier configuration.

operational amplifier operated with a noninverting feedback configuration. Table XXIII shows the basic design equations for this type of operational amplifier.

The model for the inverting-feedback configuration, as did that for the inverting circuit, assumes that the load resistance R_L is large enough so that its effect is negligible, i.e., $R_L \rightarrow \infty$ and $I_{OUT} = 0$. (The effects of a finite load resistance on the noninverting operational amplifier are evaluated in the discussion of the **Equivalent-Circuit Model** of an operational amplifier.)

A noninverting operational amplifier, unlike the inverting type, requires a differential-input arrangement because it uses the common-mode effect in its feedback scheme. The following basic requirements and

Table XXIII — *Basic Design Equations for an Operational Amplifier Operated in the Noninverting-Feedback Configuration*

CLOSED-LOOP GAIN (Voltage Transfer Function)

Precise Equation:
$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_r Z_{oi} + A_o(\omega) Z_i (Z_r + Z_f)}{(Z_i + R_r)(Z_r + Z_f + Z_{oi}) + Z_r(Z_f + Z_{oi}) + A_o(\omega) Z_i Z_r}$$

Classical Form: When $A_o(\omega)$ and Z_i are very large and Z_{oi} approaches zero (the usual conditions), the closed-loop gain can be expressed by the following classical relationship:

$$\frac{V_{OUT}}{V_{IN}} \underset{A_o(\omega) \to \infty}{=\!=} 1 + \frac{Z_f}{Z_r}$$

LOOP GAIN: (Ratio of Open-Loop Gain to Closed-Loop Gain)

Precise Equation:
$$LG = 1 + \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}}$$

Classical Form: It is apparent that the second term of the above equation is normally very large. The equation for the loop gain then reduces to the classical form, as follows:

$$LG \doteq \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}}$$

INPUT IMPEDANCE

Precise Equation:
$$Z_{IN} = Z_i + R_r + Z_r \frac{Z_f + Z_{oi} + A_o(\omega) Z_i}{Z_r + Z_f + Z_{oi}}$$

Classical Form: Because $A_o(\omega)$ and Z_i are usually very large and Z_{oi} is small, the input impedance can be approximated as follows:

$$Z_{IN} \doteq \frac{A_o(\omega) Z_i}{1 + \frac{Z_f}{Z_r}}$$

OUTPUT IMPEDANCE: $[Z_{OUT} = V_{OUT}(R_L \to \infty)/I_{OUT}(R_L \to 0)]$

Precise Equation:
$$Z_{OUT} = \frac{Z_{oi}[(Z_r + Z_f)(R_r + Z_i) + Z_r Z_f][Z_r Z_{oi} + A_o(\omega) Z_i (Z_r + Z_f)]}{[A_o(\omega) Z_i (Z_r + Z_f)][(Z_i + R_r)(Z_r + Z_f + Z_{oi}) + Z_r(Z_f + Z_{oi}) + A_o(\omega) Z_i Z_r]}$$

Classical Form: If $A_o(\omega)$ and Z_i are both very large, the equation for the output impedance becomes

$$Z_{OUT} \doteq Z_{oi} \frac{1 + \frac{Z_f}{Z_r}}{A_o(\omega)}$$

definitions that apply to the inverting circuit shown in Fig. 151 are also valid for the general noninverting circuit shown in Fig. 152:

1. The dc return paths to ground for the two inputs must be equal and finite for amplifiers that require a significant amount of input bias current.
2. The input and output impedances, Z_i and Z_{oi}, are inherent in the basic amplifier unit and are shown on the diagram to emphasize their importance in the determination of the classical design relationships.
3. The open-loop gain is frequency-dependent and is represented by the symbol $A_o(\omega)$.
4. The plus and minus labels on the input terminals designate the noninverting and inverting terminals, respectively.

In the noninverting circuit, however, the source impedance is included in the passive element R_r rather than the frequency-dependent parameter Z_r, as in the inverting circuit.

As with the inverting-feedback configuration, the **closed-loop gain** for the noninverting configuration expresses the relationship between input and output voltage. In the classical equation for this parameter, the term $1 + (Z_f/Z_r)$ represents the closed-loop gain for the ideal noninverting configuration. This term, which is referred to as the **ideal feedback characteristic,** is basic to operational-amplifier phase-compensation theory.

The classical equation for the noninverting **input impedance** states that this parameter is equal to the product of the intrinsic input impedance Z_i and the loop gain.

As with the inverting configuration, the **closed-loop output impedance** for the noninverting configuration is defined as the ratio of the open-circuit output voltage V_{OUT} to the short-circuit output current I_{out}. The classical expression indicates that the output impedance is equal to the intrinsic output impedance Z_{oi} divided by the loop gain. It should be noted that the classical expressions for the closed-loop output impedances are identical for both the inverting- and noninverting-feedback configurations.

Closed-Loop Equivalent-Circuit Model—Fig. 153 shows the equivalent circuit of a closed-loop operational amplifier. This equivalent circuit is valid for either the inverting or the noninverting configuration. In the inverting configuration, Z_r is used to represent the impedance in series

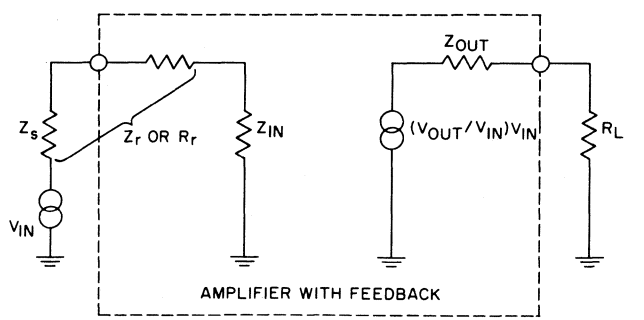


Fig. 153 — Equivalent-circuit model of a closed-loop operational amplifier.

with the closed-loop input impedance Z_{IN}. In the noninverting configuration, term Z_r is replaced by R_r to show that the components thus represented are independent of frequency.

One of the important features of the equivalent-circuit model is that it accurately accounts for the effects of a finite load impedance, R_L. This circuit model indicates that the equation for the output voltage developed across the load resistance $[V_O(R_L)]$ may be written as follows:

$$V_O(R_L) = \frac{\left(\frac{V_{OUT}}{V_{IN}}\right) V_{IN} R_L}{R_L + Z_{OUT}}$$

The transfer-function ratio (closed-loop gain) is given by

$$\frac{V_O(R_L)}{V_{IN}} = \frac{\left(\frac{V_{OUT}}{V_{IN}}\right) R_L}{R_L + Z_{OUT}}$$

For an operational amplifier that has a closed-loop gain of 164 with an open-circuit load and an output impedance Z_{OUT} of 37.4 ohms, the addition of a 2000-ohm load resistance would modify the closed-loop gain as follows:

$$\frac{V_O(R_L)}{V_{IN}} = \frac{(164)(2000)}{(2000 + 37.4)} = 162$$

This value corresponds to 44.15 dB as compared to 44.3 dB for an open-circuit load. This example indicates that only a small error results from the fact that the effect of a finite load impedance is not considered in the classical design equations.

Effect of the Common Mode Gain —In the preceding discussions of the inverting- and noninverting-feedback configurations of the operational amplifier, it was tacitly assumed that the common-mode gain was essentially zero (infinite attenuation). The validity of this assumption is considered separately in this section because the basic feedback equations become burdensome when common-mode effects are included. As a result, the salient features of these equations become obscured.

The common-mode gain is the ratio of the output voltage, V_{OUT}, to the input voltages, V_i and V_e, when V_i and V_e are identical in amplitude and phase. An examination of Figs. 151 and 152 shows that, in either the inverting or noninverting configuration, the differential gain acts on the difference between the voltages V_i and V_e. On the other hand, the common-mode gain acts on those portions of V_i and V_e that are in phase and identical in magnitude. That is, the common-mode gain acts on the smaller of the two in-phase signals (V_i or V_e). In the inverting configuration V_i is less than V_e, but in the noninverting configuration V_i is greater than V_e. These conditions are reflected by the output-voltage equations when the effects of the common-mode gain (CMG) are considered, as follows:

1. For the inverting configuration,

$$V_{o1} = A_o(\omega)(V_i - V_e) - (CMG)(V_i)$$

2. For the noninverting configuration,

$$V_{o_1} = A_o(\omega)(V_i - V_e) - (CMG)(V_e)$$

In each case, the criteria for the common-mode gain, CMG, to be negligible compared to the open-loop gain, $A_o(\omega)$, are as follows:

1. For the inverting configuration,

$$CMG \ll \frac{A_o(\omega)\, Z_i}{R_r}$$

2. For the noninverting configuration,

$$CMG \ll \frac{A_o(\omega)\, Z_i}{Z_i + R_r}$$

It is apparent that the gain of an inverting configuration is not affected by the common-mode gain when the input impedance Z_i is assumed to be infinite. However, when this same assumption is made for a noninverting configuration, the gain is dependent upon the common-mode gain provided the open-loop gain is finite.

The common-mode-gain inequalities may be given in terms of the common-mode rejection ratio CMRR, which is the open-loop gain, $A_o(\omega)$, divided by the common-mode gain CMG. The following inequalities are then obtained:

1. For the inverting configuration,

$$CMRR \gg \frac{R_r}{Z_i}$$

2. For the noninverting configuration,

$$CMRR \gg \frac{Z_i + R_r}{Z_i}$$

Neither of these inequalities places a stringent restriction on common-mode rejection.

GENERAL APPLICATION CONSIDERATIONS

Several basic factors must be considered in the successful application of an operational amplifier. For example, a major factor that must be taken into account for an operational amplifier operated in a negative-feedback closed-loop configuration is that the amplifier will attempt to balance the voltages at the two input terminals within the offset voltage. This factor and other important considerations of which the users of integrated-circuit operational amplifiers should be aware are discussed in following paragraphs.

Single-Supply Operation

If desired, all RCA integrated-circuit operational amplifiers may be operated from a single dc power supply, instead of from dual supplies as indicated on the diagrams shown in the published data on these devices. For this type of operation, any ground or supply return is connected to an external voltage-divider network that provides the same potential that normally exists at this point relative to the positive and negative terminals of the amplifier. Fig. 154 shows a typical connection for operation of the RCA-CA3015 integrated-circuit operational amplifier from a single 24-volt dc supply.

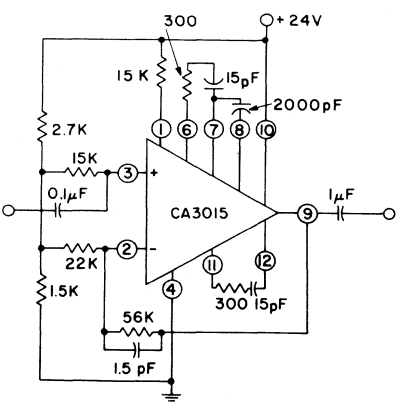


Fig. 154 — Operation of the CA3015 in a 10 dB Amplifier from a single 24-volt supply.

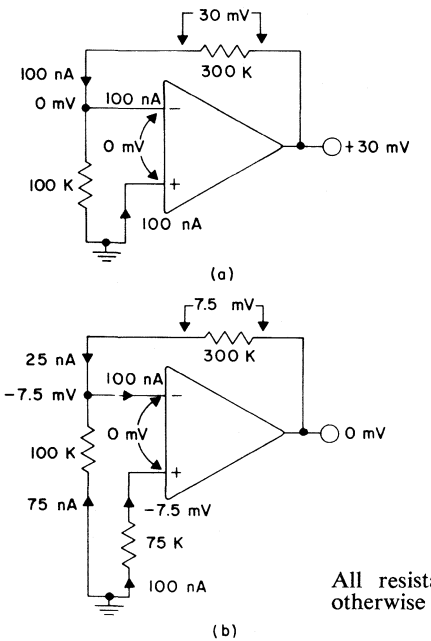
Common-Mode Restrictions

When an integrated-circuit operational amplifier is operated from a single dc supply, the voltages at the two inputs must be matched within the limits of the specified common-mode voltage range. For example, the range of the common-mode input voltage is typically +5 volts to −9 volts for a CA3033 integrated-circuit operational amplifier operated from dual positive and negative 12-volt supplies. For operation of this operational amplifier from a single 24-volt supply, the range of the common-mode input voltage is translated to +17 volts to +3 volts.

Bias Current and Offset Voltage

Another important factor that should be considered in the use of operational amplifiers is the effect of input bias current on the resulting output signal. In any feedback configuration, the effective offset terms are multiplied by the closed-loop gain. For example, if the closed-loop gain is 100 and the amplifier has an uncorrected offset voltage of 2 millivolts, the output would be offset 200 millivolts from the intended design point.

In addition to the offset voltage, another source of input error is introduced by the bias current. Fig. 155(a) dramatically demonstrates the error associated with input bias current. In this circuit, a 30-millivolt output offset voltage is produced by the input bias current. If the value of the resistance at the noninverting input is made equal to the parallel combination of the 300-kilohm feedback resistor and the 100-kilohm in-



V_{IO} = 0 mV
I_{IB} = 100 nA
I_{IO} = 0 nA

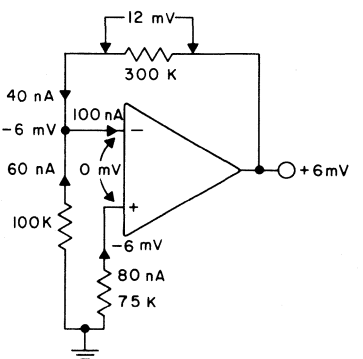
V_{IO} = 0 mV
I_{IB} = 100 nA
I_{IO} = 0 nA

All resistance values in ohms unless otherwise specified.

Fig. 155 — (a) Circuit showing effect of input bias current and (b) circuit that compensates for the input bias current.

put resistor, or 75 kilohms, the error associated with the input bias current can be eliminated, as shown in Fig. 155(b).

In the previous example, the offset current was considered to be zero. Fig. 156 illustrates a condition in which the bias current is 100 nanoamperes on the inverting (−) input and 80 nanoamperes on the noninverting (+) input for an offset current of 20 nanoamperes. This



V_{IO} = 0 mV

I_{IB} = 100 nA
(INVERTING INPUT)

I_{IB} = 80 nA
(NONINVERTING INPUT)

I_{IO} = 20 nA

All resistance values in ohms unless otherwise specified.

Fig. 156 — Circuit showing effect of an input offset current.

bias-current unbalance results in an output-voltage offset of 6 millivolts. If all resistances in the feedback network are reduced by a factor of 10, however, the output offset voltage is also proportionately decreased.

The following points are emphasized by the preceding examples:

1. The effective dc resistances at both inputs to the operational amplifier must be maintained equal.

2. The values of the feedback-network resistance should be small with respect to the bias-current term to help minimize the effects of bias-current offset. The curves of these parameters, shown in Fig. 157, aid in a quick assessment of the effects of resistance and bias current. It should be remembered that these equivalent input offset terms must be multiplied by the closed-loop voltage gain to assure that the output will be within the required linear output range (i.e., that the maximum output signal will not be clipped or limited because of offsets).

Another important point sometimes ignored in the application of operational amplifiers is the need for a dc bias-current return for the input transistors. This factor is most important for the voltage-follower configuration in which, even with low-input-impedance operational amplifiers, the input impedance can be tens or hundreds of megohms because of high common-mode input impedance and the boot-strapping effect of the feedback network. Usually, the bias resistor becomes the limiting factor on the actual input impedance.

Offset-Voltage Nulling

Offset-voltage may be nulled out in most operational amplifiers, even those without terminals specifically designed for this purpose.

Fig. 158 shows techniques used to null the offset voltage for both the CA3015 and the CA3033 families of operational amplifiers.

Phase Compensation

Phase compensation is required for almost all operational amplifiers to assure that the circuit remains

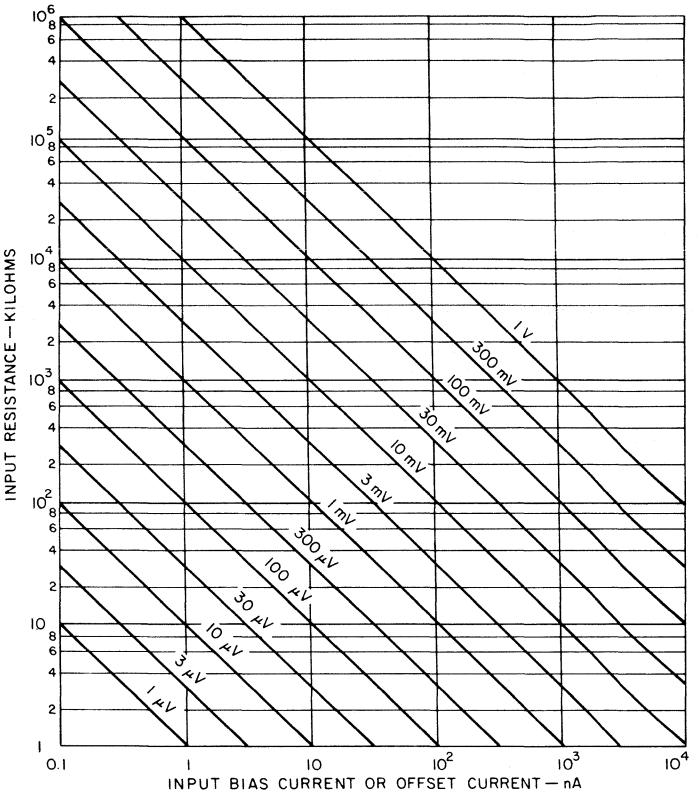
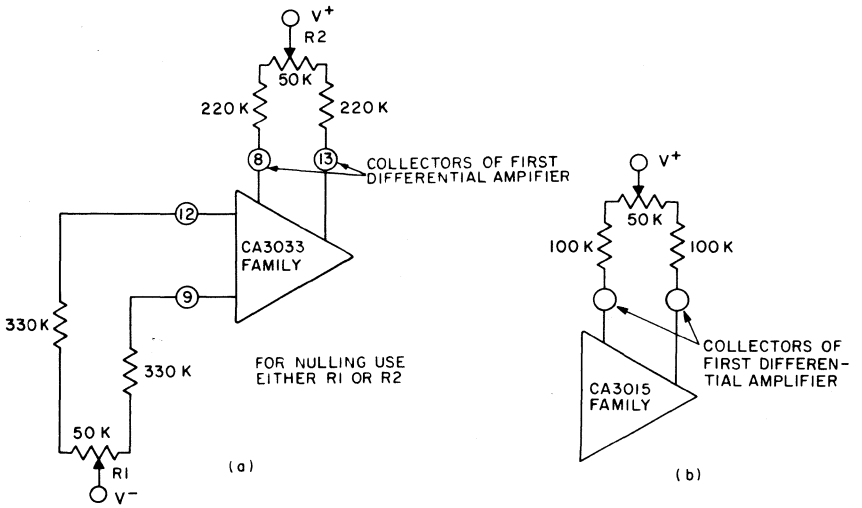


Fig. 157 — Feedback-network resistance as a function of input bias current or input offset current. (The voltage values on the curves indicate the effective offset voltage that results from the input offset current. The IR drop produced by the bias current is equal to the product of this current and the feedback resistance.)

stable as the closed-loop voltage gain approaches the critical unity-gain region. When no phase compensation is employed, the gain of the feedback signal may be greater than unity when the phase angle approaches 180 degrees. In such cases, feedback that is negative at low frequencies becomes positive at higher frequencies and results in circuit oscillation unless some form of phase compensation is employed to control the response of the amplifier. The required phase compensation may be included internally as an integral part of the amplifier circuit, or it may be applied externally. This latter approach allows much greater flexibility in the design of operational-amplifier circuits.

The gain and phase curves shown in Fig. 159 form an excellent starting point for an analysis of the phase-compensation requirements of an operational amplifier. Curves A and X show the gain and phase of a simple single-stage amplifier as a function of frequency. At the fre-



All resistance values in ohms unless otherwise specified.

Fig. 158 — Techniques for nulling the input offset voltage: (a) two methods for the CA3033 and CA3047 families of operatonal amplifiers; (b) method for the CA3015 family of operational amplifiers.

quency for which the gain is reduced, because of the load resistance and associated components, to 0.707 of (3-dB below) its low-frequency value, the phase of the feedback has shifted approximately 45 degrees. For a frequency ten times greater than that at the 3-dB point, the phase shift has increased to about 84.3 degrees. At one-tenth the 3-dB frequency, however, the phase shift is only 5.7 degrees. The phase shift is substantially less than 180 degrees (i.e., in a closed-loop system, the feedback would be negative) over the full operating-frequency range of the single-stage amplifier. Closure of the feedback loop around this amplifier, therefore, will not introduce any instability problems.

If a second similar stage is added to the single-stage amplifier, the additional RC time constant (load resistance and associated transistor and stray capacitances) produces a breakpoint (pole) in the circuit response at the same frequency for which the breakpoint occurs for the single-stage amplifier above. Curve B of Fig. 159 indicates the additional gain provided by the second stage, and curve Y shows the over-all phase response of the two amplifier stages. The phase shift in the two-stage amplifier approaches 180 degrees at a frequency only a decade higher than the 3-dB frequency. This response, together with the additional phase shifts introduced by external elements, indicates that oscillation results when the two-stage amplifier operates at closed-loop gains below 40 dB, (i.e., at a decade above the 3-dB frequency). This limitation substantially reduces circuit-design flexibility with respect to bandwidth capability because the designer is not allowed to extend the closed-loop bandwidth

any significant amount beyond the 3-dB frequency.

Phase compensation of an operational amplifier is usually accomplished by addition of a capacitor from collector to ground in one of the existing lower-frequency stages. In a differential-input operational amplifier, it is desirable to obtain the highest gain from the input differential amplifier; this stage, therefore, is usually the lowest-frequency stage in the operational amplifier. Because additional gain stages are usually included in the operational amplifier, the highest slewing rate is obtainable when the phase compensation is provided in the input differential amplifier, as discussed subsequently. In addition, this compensation arrangement does not introduce a third pole in the amplifier response; the lowest-frequency pole merely occurs at a smaller gain value. Curves C and Z show the gain and phase response of the two-stage amplifier when this method of phase compensation is employed. It should be noted that one of the 3-dB points is reduced three decades and that the phase shift at the unity-gain point is approximately 157 degrees. A margin of 23 (180 − 157) degrees is provided in the unity-gain noninverting configuration before oscillations occur.

Another form of phase compensation, referred to as Miller compensation, makes use of the capacitive multiplication effect obtained when a capacitor is connected between the collector and base of a transistor amplifier. The effective value of the capacitance at the input to the amplifier stage can be approximated as follows:

$$C_{eff} \approx C(1 + \text{stage gain})$$

This capacitive multiplication makes possible the use of a much smaller compensating capacitor to obtain the same roll-off point as that for a similar circuit in which the Miller effect is not used.

A resistor may be connected in series with a Miller phase-compensating capacitance to cancel the

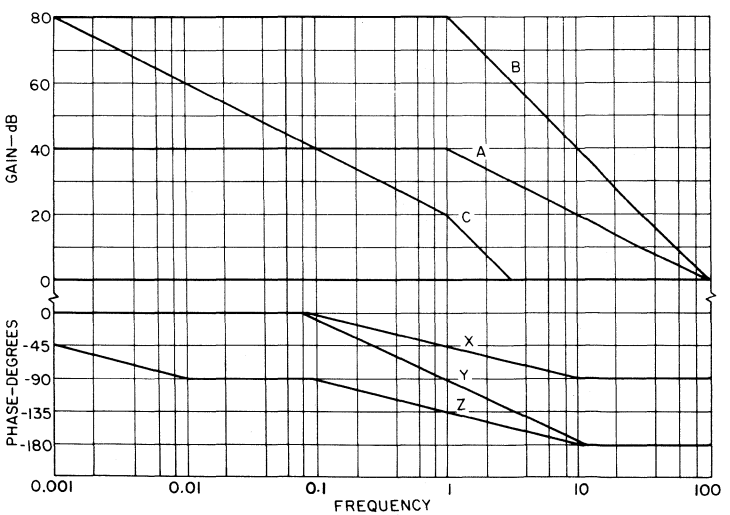


Fig. 159 — Gain and phase curves for a single-stage and a two-stage amplifier.

effect of the capacitor at the frequency for which $\omega = 1/RC$, where $\omega = 2\pi f$. This form of compensation is most effective when applied to the collector of the input amplifier stage. In this arrangement, a capacitor and resistor are connected in series from the collector at the first stage to the collector of the second stage to form an RC time-constant network with the collector load resistor of the first stage and the multiplied capacitance at the base of the second stage. The value of the capacitor is selected to reduce the amplifier response to the lowest corner (breakpoint) frequency and, therefore, to assure that the desired degree of stability is obtained for any given bandwidth. The value of the resistor is then chosen so that the RC product corresponds to the second highest corner frequency. The effect of this time-constant network, therefore, is removed from the circuit at the same point at which the second corner occurs. This compensation technique simultaneously provides the optimum bandwidth for the system and the desired degree of phase margin. Similar performance is not possible with internally compensated operational amplifiers because maximum compensation is applied to provide stability down to the critical unity-gain voltage-follower configuration.

In addition to the phase-retarding technique discussed in the preceding paragraphs, phase-advancing, or phase-lead, techniques may also be used to provide compensation of operational amplifiers. This method is explained subsequently in the section on **Applications of the Low-Power Operational Amplifiers.**

Crossover Distortion

Crossover distortion occurs, to some degree, in all class B output stages. In addition to the undesirable distortion components of operational amplifiers that employ such output stages, the open-loop system gain may be substantially reduced through the crossover region. The slope of the output transfer characteristic represents the system gain. At the flat zone in the center of the crossover region, therefore, the open-loop gain of the amplifier diminishes appreciably. This gain reduction is particularly noticeable when a load is placed on the amplifier. In many applications, the gain reduction in the crossover region may not be significant; the user, however, should be aware that this condition exists and may introduce errors in system calculations if it is not taken into account.

Slew Rate

Slew rate, when defined with respect to a sine-wave signal of a given amplitude, is equal to the product of the factor π, the sine-wave frequency (f) in megahertz, and the peak-to-peak excursion of the sine-wave voltage (V_{pp}), i.e.:

$$SR = \pi f V_{pp}$$

This term, therefore, is expressed in volts per microsecond. Fig. 160 shows a graphic representation of the equation for the slew rate.

The slew rate of an operational amplifier is usually an inverse function of the phase compensation included in the circuit. As the phase compensation is increased, the slew rate is reduced. Any increase in circuit gain provided beyond the point at which the phase-compensating capacitor is located, however, causes an increase in the slew rate. For example, if the output of the input differential amplifier of an operational amplifier has a rate of change

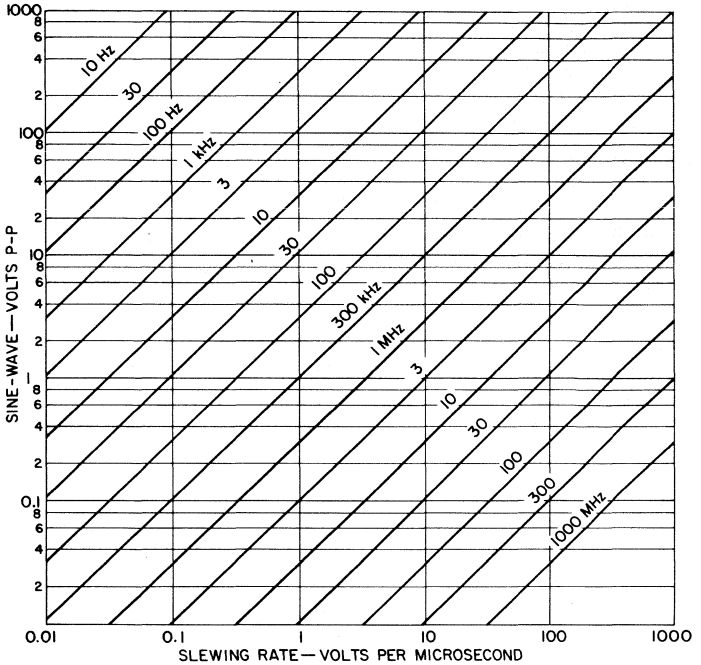


Fig. 160 — Slewing rate of a sine-wave signal.

of 0.5 volt per microsecond at the collector of this stage with the compensation applied at this point and a gain of 100 beyond this point and with no further degradation in the slew rate, the output of the amplifier has a rate of change of 50 volts per microsecond.

Slew rate is particularly significant in wide-band operational amplifiers. For example, the RCA-CA3015 operational amplifier can provide useful closed-loop gain characteristics at frequencies up to 50 MHz. The maximum amplitude of the response of this amplifier, however, is limited by the restriction on the slew rate imposed by the phase-compensating capacitor.

Output driving-current capability is also a major consideration in the achievement of a high amplifier slew rate. If there are no other rate-limiting factors, the rate of change of the output voltage depends upon the maximum rate at which the output load capacitance can be charged. Under such conditions, therefore, the maximum slew rate is limited by the driving current supplied by the amplifier (i.e., $SR = dv/dt = i/C$). For example, an amplifier that provides an output current of 10 milliamperes and drives a 1000-picofarad load capacitance would have a maximum slew rate of 10 volts per microsecond, provided that no other rate-limiting circuits were included in the

system. In the design of an amplifier that is required to have a high slew rate, the output driving current must be determined on the basis of the expected load capacitance and the desired slew-rate capability.*

Gain-Bandwidth Product

The product of the low-frequency open-loop gain of an operational amplifier and the 3-dB bandwidth is referred to as the gain-bandwidth product. This term is significant for operational amplifiers in which the small-signal response rolls off at 6 dB per octave (20 dB per decade) and, therefore, intersects the frequency axis at the unity-gain (0-dB) point, i.e., at the gain-bandwidth product. When the open-loop response of an amplifier rolls off at a slope greater than 6 dB per octave, the response intersects the frequency axis at a value less than that predicted by the gain-bandwidth product. For such amplifiers, the product of the open-loop gain and the 3-dB bandwidth has no special significance, and the unity-gain frequency is used to represent the gain-bandwidth figure of merit. In either case, however, the gain-bandwidth value provides only a limited indication of amplifier performance and provides very little information on small-signal performance that can be achieved with phase compensation at low gain settings.

* The curves shown in Fig. 216 in the section on the **Operational Transconductance Amplifier** provides graphic representations of the slew-rate equation for various values of load capacitance. These curves indicate the value of output driving current that must be supplied by the amplifier to obtain the desired slew rate for a given value of load capacitance. (The curves do not take into account other rate-limiting factors that may be included in the system.)

Output Impedance

In a closed-loop system, the output impedance of an operational amplifier approaches zero. Two basic methods are used to match operational voltage amplifiers to transmission lines. In one method, the low impedance of the operational amplifier is increased to match that of the transmission line by addition of an external resistor in series with the amplifier output. This approach provides an excellent match and is used in many generators for which power loss is not an important consideration. In the other approach, the output impedance of the operational amplifier is adjusted to match the transmission line by use of positive feedback.

A common error among designers inexperienced in the application of operational amplifiers is that they attempt to terminate the amplifier in a load impedance equal to the output impedance of the device. It is important for the designer to realize that the output impedance of an operational amplifier is a small-signal parameter useful for guidance in circuit design, but that this parameter in no way indicates the current-handling capability of the amplifier. This term is useful, however, in predictions of the reduction in open-loop voltage gain that results from external loading of the amplifier output. For example, the open-loop voltage gain of an operational voltage amplifier that has an output impedance of 100 ohms would be reduced to 0.9 of the open-circuit-load value if the amplifier were operated in a load termination that has a total impedance of 900 ohms. The effect of a finite load impedance on the open-loop voltage gain of an operational amplifier was discussed previously in the section on the **Equivalent Circuit Model.**

FEATURES AND APPLICATIONS OF RCA OPERATIONAL VOLTAGE AMPLIFIERS

RCA offers a broad line of monolithic integrated-circuit operational voltage amplifiers that feature exceptional gain-bandwidth capabilities (greater than 50 MHz for some types), low-frequency voltage gains of 60 to 93 dB, and common-mode rejection ratios of 94 to 105 dB. These devices operate at low dissipational levels, provide relatively large output-voltage swings, exhibit wide common-mode ranges, and have small input bias currents and voltage offsets. Table XXIV lists these operational amplifiers and indicates some of their distinguishing features. (More detailed information on ratings and operating characteristics of

Table XXIV — *RCA Integrated-Circuit Operational Voltage Amplifiers*

Type	Package	Supply Voltage (volts)	Voltage Gain (dB)	Output Voltage Swing (volts p-p)	Operating Dissipation (mW)	Open-Loop 3-dB Bandwidth (kHz)	CMRR (dB)	Operating Temperature Range (°C)
CA3008	14-term.	±6	60	6.75	40	300	94	−55 to +125
CA3008A	ceramic flat pack	±6	60	6.75	40	300	94	−55 to +125
CA3010	12-term.	±6	60	6.75	40	300	94	−55 to +125
CA3010A	TO-5-style	±6	60	6.75	40	300	94	−55 to +125
CA3015	12-term.	±12	66	14	175	320	103	−55 to +125
CA3015A	TO-5-style	±12	66	14	175	320	103	−55 to +125
CA3016	14-term.	±12	66	14	175	320	103	−55 to +125
CA3016A	ceramic flat pack	±12	66	14	175	320	103	−55 to +125
CA3029	14-term.	±6	60	6.75	40	300	94	0 to +70
CA3029A	dual-in-line plastic	±6	60	6.75	40	360	94	0 to +70
CA3030	14-term.	±12	66	14	175	320	103	0 to +70
CA3030A	dual-in-line plastic	±12	66	14	175	320	103	0 to +70
CA3033	14-term.	±12	90	22	120	230*	100	−55 to +125
CA3033A	dual-in-line ceramic	±15	93	25	160	350*	105	−55 to +125
CA3037	14-term.	±6	60	6.75	40	300	94	−55 to +125
CA3037A	dual-in-line ceramic	±6	60	6.75	40	300	94	−55 to +125
CA3038	14-term.	±12	66	14	175	320	103	−55 to +125
CA3038A	dual-in-line ceramic	±12	66	14	175	320	103	−55 to +125
CA3047	14-term.	±12	90	22	120	230*	100	0 to +70
CA3047A	dual-in-line plastic	±15	93	25	160	350*	105	0 to +70

* Bandwidth measured at an amplifier gain of 60 dB.

The RCA line of integrated-circuit operational amplifiers also includes the type CA3056A. This operational amplifier, which is interchangeable with the industry 741 series, operates from dual dc supply voltages up to +15 and −15 volts, is supplied in an 8-terminal TO-5-style package, and has an operating-temperature range of −55°C to +125°C. Ratings and characteristics for the CA3056A are given in the **Technical Data Section** of this Manual and in the RCA Technical Bulletin for this type.

the amplifiers are given in the **Technical Data** Section of this Manual or in the RCA Technical Bulletin for each type.)

Most of the twenty-one operational amplifiers listed in Table XXIV can be classified as extremely wide bandwidth devices that operate at the relatively low output-power levels typical of monolithic integrated circuits. The CA3033, CA3033A, CA3047, and CA3047A operational amplifiers, however, have power-output capabilities substantially greater than those normally achieved in monolithic circuits. The operational amplifiers in each classification differ in one or more of the following categories: type of package, supply-voltage rating, operating-temperature range, and electrical performance characteristics. The following paragraphs describe the significant features of the different devices and explain their use in a wide variety of circuit applications.

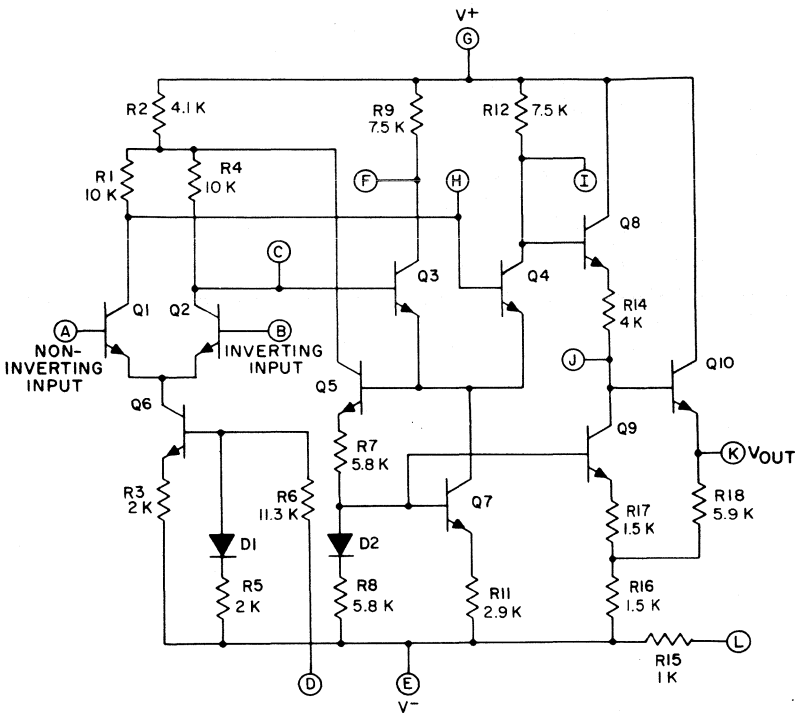
Low-Power Types

The CA3008, CA3008A, CA3010, CA3010A, CA3015, CA3015A, CA3016, CA3016A, CA3029, CA3029A, CA3030, CA3030A, CA3037, CA3037A, CA3038, and CA3038A have identical circuit configurations. The terminal numbers for the CA3010, CA3010A, CA3015, and CA3015A, which are supplied in 10-terminal TO-5-style packages, however, differ from those of the other circuits, which are supplied in 14-terminal (flat-pack or dual-in-line) packages. For convenience of reference in the following discussions, circuit terminals mentioned in the text or shown on diagrams are identified by alphabetical designations. Fig. 161 shows the circuit diagram for the operational voltage amplifiers and the alphabetical designation assigned to each terminal; the associated chart shows the corresponding terminal numbers for both 10-terminal and 14-terminal packages.

The operational-amplifier configuration shown in Fig. 161 is designed to operate primarily from symmetrical positive and negative dc power supplies at various levels of supply voltage. The devices that employ this configuration may also be operated from single supplies if desired, as explained previously in the section on **General Application Considerations.**

The operational amplifiers identified by the "A" suffix in their type-number designation have lower noise figures and improved input characteristics in comparison with the corresponding types without the "A" suffix. For applications in which low noise and exceptional dc balance are prime considerations, the "A"-version types are recommended. Fig. 162 shows the noise figure of the "A"-version operational amplifiers as a function of frequency for operation from dual 3-, 6- and 12-volt supplies.

Circuit Descripton—The operational-amplifier circuit consists basically of two differential amplifiers and a single-ended output circuit in cascade. The pair of cascaded differential amplifiers are responsible for virtually all the gain provided by the operational-amplifier circuit. The inputs to the operational amplifier are applied to the bases of the pair of emitter-coupled differential input transistors Q1 and Q2 in the first differential amplifier. The inverting input is applied to the base of transistor Q2, and the noninverting input is applied to the base of transistor Q1. These transistors develop the driving signals for the second differential amplifier. The constant-current source transistor Q6 provides bias stabilization for tran-



All resistance values in ohms unless otherwise specified.

Letter Designation	Corresponding Terminal Number	
	12-Term. Pkg.	14-Term. Pkg.
A	3	4
B	2	3
C	12	1
D	1	2
E	4	6
F	11	14
G	10	13
H	6	9
I	7	10
J	8	11
K	9	12
L	5	8
NOT USED	—	5
NOT USED	—	7

Fig. 161 — Circuit configuration for low-power integrated-circuit operational amplifiers (CA3008, CA3008A, CA3010, CA3010A, CA3015, CA3015A, CA3016, CA3016A, CA3029, CA3029A, CA3030, CA3030A, CA3037, CA3037A, CA3038, and CA3038A).

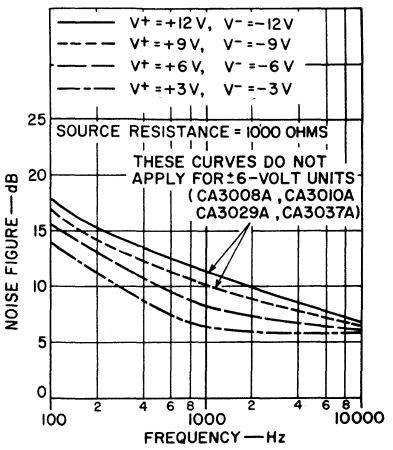


Fig. 162 — Noise figure for the "A" version integrated-circuit operational amplifiers.

sistors Q1 and Q2. Diode D1 provides thermal compensation for the first differential-amplifier stage.

The emitter-coupled transistors Q3 and Q4 in the second differential amplifier are driven push-pull by the outputs from the first differential amplifier. Bias stabilization for the second differential amplifier is provided by the constant-current-source transistor Q7. Compensating diode D2 provides the thermal stabilization for the second differential amplifier and also for the transistor Q9, in the output stage.

Transistor Q5 develops the negative feedback to reduce common-mode error signals that are developed when the same input is applied to both input terminals of the operational amplifier. Transistor Q5 samples the signal that is developed at the emitters of transistors Q3 and Q4. Because the second differential stage is driven push-pull, the signal at this point will be zero when the first differential-amplifier stage and the base-emitter circuits of the second stage are matched and there is no common-mode input. A portion of any common-mode, or error, signal that appears at the emitters of transistors Q3 and Q4 is developed by transistor Q5 across resistor R2 (the common collector resistor for transistors Q1, Q2, and Q5) in the proper phase to reduce the error. The emitter circuit of transistor Q5 also reflects a portion of the same error signal into the constant-current-source transistor Q7 in the second differential-amplifier stage so that the activating error signal is further reduced.

Transistor Q5 also develops feedback signals to compensate for dc common-mode effects produced by variations in the supply voltages. For example, a decrease in the dc voltage from the positive supply results in a decrease in the voltage at the emitters of transistors Q3 and Q4. This negative-going change in voltage is reflected by the emitter circuit of transistor Q5 to the bases of transistoars Q7 and Q9. Less current then flows through these transistors. The decrease in the collector current of transistor Q7 results in a reduction of the current through transistors Q3 and Q4, and the collector voltages of these transistors tend to increase. This tendency to increase on the part of the collector voltages partially cancels the decrease that occurs with the reduction in the positive supply voltage. The partially cancelled decrease in the collector voltage of transistor Q4 is coupled directly to the base of transistor Q8 and is transmitted by the emitter circuit of this transistor to the base of output transistor Q10. At this point, the decrease in voltage is further cancelled by the increase in the collector voltage of transistor Q9 that results from the decrease in current mentioned above.

In a similar manner, transistor Q5 develops the compensating feed-

back to cancel the effects of an increase in the positive supply voltage or of variations in the negative supply voltage. Because of the feedback stabilization provided by transistor Q5, the operational amplifier provides high, common-mode rejection and excellent open-loop stability, and has a low sensitivity to power-supply variations.

In addition to their function in the cancellation of supply-voltage variations, transistors Q8, Q9, and Q10 are used in an emitter-follower type of single-ended output circuit. The output of the second differential amplifier is directly coupled to the base of transistor Q8, and the emitter circuit of transistor Q8 supplies the base-drive input for output transistor Q10. A small amount of signal gain in the output circuit is made possible by the bootstrap connection from the emitter of output transistor Q10 to the emitter circuit of transistor Q9. If this bootstrap connection were neglected, transistor Q9 could be considered as merely a dc constant-current source for drive transistor Q8. Because of the bootstrap arrangement, however, the output circuit can provide a signal gain of 1.5 from the collector of differential-amplifier transistor Q4 to the output. Although this small amount of gain may seem insignificant, it does increase the output-swing capabilities of the operational amplifiers.

The output from the operational-amplifier circuit is taken from the emitter of output transistor Q10 so that the dc level of the output signal is substantially lower than that of the differential-amplifier output at the collector of transistor Q4. In this way, the output circuit shifts the dc level at the output so that it is effectively the same as that at the input when no signal is applied.

Resistor R15 increases the negative-going-signal capability of the operational amplifier, when terminal L is shorted to terminal K so that the resistor is connected between the output and the negative supply.

DC Characteristics—Table XXIV indicates that the low-power series of operational amplifiers may be classified, on the basis of the nominal upper limit of the supply voltages for dual-supply operation, as either ±6-volt types or ±12-volt types. The dc characteristics of the amplifiers included in each classification are summarized in the following paragraphs:

±6-Volt Types: The CA3008 and CA3008A, the CA3010 and CA3010A, the CA3029 and CA3029A, and the CA3037 and CA3037A integrated-circuit operational amplifiers have identical electrical characteristics, except for the improved noise and input characteristics of the "A" version types. These operational amplifiers are designed to operate from two symmetrical dc power supplies at supply voltages in the range from ±3 volts to ±6 volts. For operation with ±3-volt supplies, the power dissipation in the amplifiers is less than 7 milliwatts with terminal L open or 23 milliwatts with terminal L shorted to terminal K. When ±6-volt supplies are used, the dissipation level increases to either 40 or 92 milliwatts, depending upon whether terminal L is open or shorted to terminal K.

The input offset voltage for the operational amplifiers is typically 1.1 millivolts for the basic types and 0.9 millivolt for the "A"-version types for all symmetrical supply voltages. This parameter is relatively insensitive to variations in the supply voltages. When ±6-volt supplies are used, the variation in the input offset voltage with fluctuations in supply voltage is typically less than

300 microvolts per volt for either supply. For ±3-volt supplies, the variation is typically 700 microvolts per volt.

±12-Volt Types: The CA3015 and CA3015A, the CA3016 and CA3016A, the CA3030 and CA3030A, and the CA3038 and CA3038A operational amplifiers are identical to the ±6-volt types discussed previously, except for improved device breakdown voltage that permits operation from dual positive and negative 12-volt supplies. Operation of these types from power supplies of ±6 volts or ±3 volts is the same as for the lower-voltage types. When operated from ±12-volt power supplies, the operational amplifiers have a typical dissipation of 175 milliwatts with terminal L open. If terminals L and K are shorted, higher output-current capability can be achieved, but the dissipation increases to a typical value of 500 milliwatts. The input offset voltage for the CA3015, CA3016, CA3030, and CA3038 is typically 1.4 millivolts, and the variation in input offset voltage is typically less than 200 microvolts per volt for fluctuations in either supply voltage. For the "A"-version types, the input offset voltage is reduced to approximately 1 millivolt. The specification for changes in this parameter with supply-voltage fluctuations remains the same.

When the ±12-volt operational amplifiers are operated from ±12-volt supplies with terminals L and K shorted for greater output capability, the power dissipation is high enough so that the maximum operating temperature is decreased to 75°C. This decreased temperature value is calculated on the basis of the maximum dissipation (P_d) of 600 milliwatts in this mode of operation, the junction to ambient thermal resistance ($\theta_{J\text{-}A}$) of 150°C per watt, and the maximum allowable junction temperature (T_J) of 165°C, as follows:

$$T_A = T_J - P_d/\theta_{J-A}$$
$$= 165 - (600 \times 10^{-13})/150$$
$$= 75°C$$

AC Characteristics—Fig. 163(a) shows the gain characteristics of the low-power series of operational amplifiers for operation from dc supplies of ±3 volts to ±12 volts. For operation from ±6-volt supplies, the amplifiers provide an open-loop gain of 60 dB. The first break frequency occurs at 300 kHz and the second break frequency occurs at 3 MHz. The unity-gain frequency is 18 MHz.

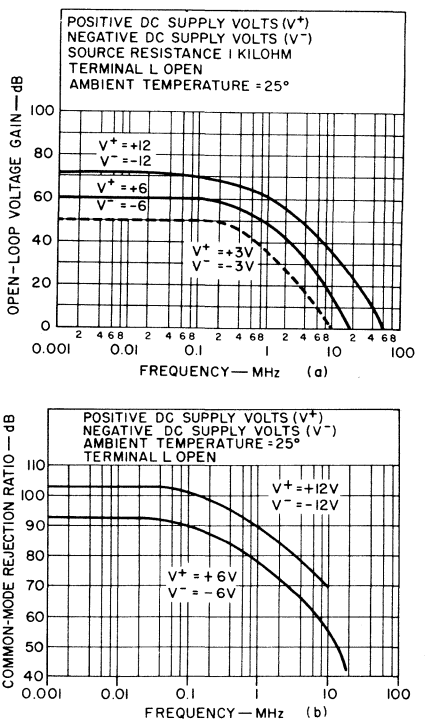
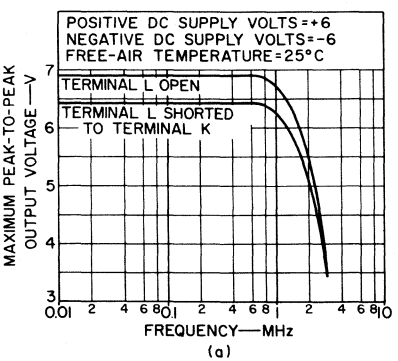


Fig. 163 — (a) Gain-frequency characteristics and (b) Common-mode rejection characteristics of the low-power operational amplifiers.

At supply voltages of ±12 volts, the first break frequency occurs at 320 kHz, the second break frequency moves to 10 MHz, the unity-gain frequency is 58 MHz, and the low-frequency open-loop gain is increased to 70 dB.

Fig. 163(b) shows the excellent common-mode-rejection characteristics of the operational amplifiers. Figure 164 shows the unloaded output swing as a function of frequency for operation from supply voltages of ±6 and ±12 volts. Fig. 165 shows the peak-to-peak output swing as a function of load impedance for various ambient temperatures. It should



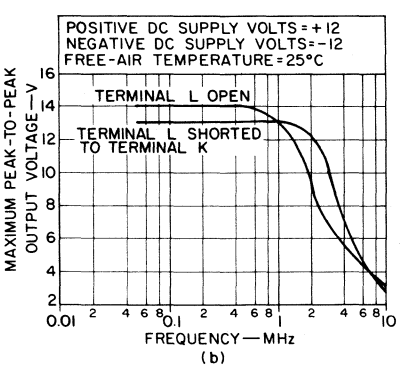
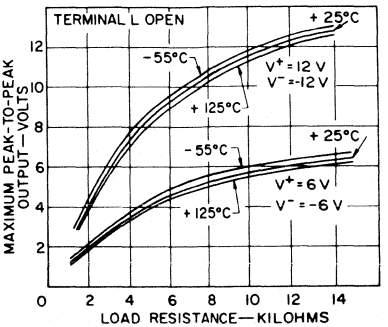


Fig. 164 — Output-swing capabilities as a function of frequency for low-power operational amplifiers: (a) for operation with ±6-volt supplies; (b) for operation with ±12-volt supplies.



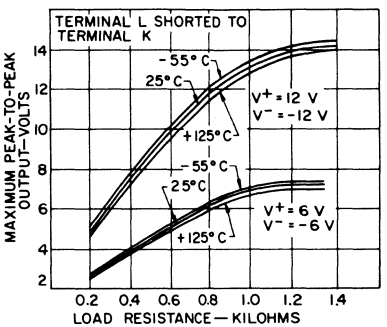


Fig. 165 — Peak-to-peak output swing as a function of load resistance.

be noted that, at the higher load currents, the internal 1000-ohm resistor is connected to the output terminal, i.e., terminal L is shorted to terminal K. For output swings that require only a flow of current out of the amplifier (positive-going outputs), the resistor need not be connected. When the output is expected to "sink" current, the 1000-ohm resistor R15 should be connected to the emitter-follower output. In all cases, the major consideration in the output-current capability of the amplifier is one of amplifier dissipation. The amplifiers should always be operated within the device dissipation ratings.

Phase Compensation—Several methods of phase compensation are readily applied to the operational amplifiers. The simplest compensation method, for those applications that require only low-frequency or dc operation, is to add a 22-ohm resistor in series with a 0.02-microfarad capacitor from ground to the base of the output emitter-follower Q10. This technique compensates the amplifier for all resistive loads for supply voltages from ±3 volts to ±12 volts.

The low input capacitance of the operational amplifiers (less than 10 picofarads) allows the use of input circuits that are compatible with input current and impedances without concern that another time constant (pole) will be introduced at the amplifier input.

In applications that require the extremely broad bandwidth capability of the operational amplifiers, the Miller compensation method is recommended. A simple Miller-type compensation is possible with two networks, each consisting of a 27-picofarad capacitor in series with a 2000-ohm resistor, connected from the collectors of the first differential amplifier to the bases of the second differential amplifier (one network from the collector of transistor Q1 to the base of transistor Q3 and the other network from the collector of transistor Q1 to the base of transistor Q4.). These networks provide ac stabilization for amplifiers operated from ±6-volt supplies. With this type of compensation, the gain-frequency response of the operational amplifiers has a 6-dB-per-octave slope to the unity-gain frequency; at this point it breaks to a 12-dB-per-octave slope. Fig. 166 shows the response of the amplifier with and without the compensating networks.

For operational amplifiers operated from ±12-volt supplies, the compensating networks must be modified to provide a capacitance of 18 picofarads and a resistance of 820 ohms. Fig. 166 shows the resulting response with this network. For both ±6-volt and ±12-volt operation, these networks provide stable operation for resistive feedback networks, but neither is sufficient to produce a flat (within ±1 dB) response for closed-loop gains below 15 dB for ±6-volt operation or below 20 dB for ±12-volt operation.

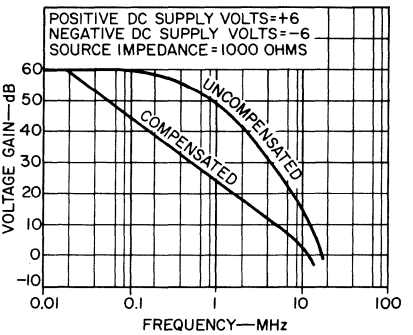


Fig. 166 — Open-loop gain as a function of frequency for both phase-compensated (27 pF + 2000 ohms) and uncompensated operational amplifiers.

Fig. 167 shows the value of phase-compensating capacitors necessary to obtain a flat (within ±1 dB) response for both ±6-volt and ±12-volt operation. Fig. 168 shows the expected response obtained for ±12-volt operation when the recommended compensation components are used.

Each curve in Fig. 167 shows two gain scales. The upper scale is the noninverting scale, which is used for voltage followers. In this connection, the maximum feedback obtainable, as far as the amplifier is concerned, is 100 per cent (all the output is applied to the input). This condition is the most critical gain relationship

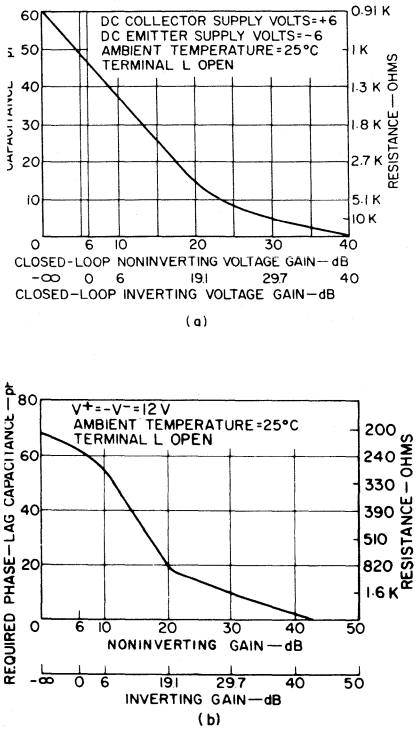


Fig. 167 — Phase-compensating capacitance required for a flat (±1 dB) response (a) for operation from ±6-volt supplies [select series resistor so that $1/(2\pi RC) = 3MHz$]; (b) for operation from ±12-volt supplies [select series resistor so that $1/(2\pi RC) = 10$ MHz].

with regard to system stability. For the inverting configuration, this condition can occur only if the value of the input resistor approaches infinity.

The next case to consider is that for a noninverting circuit in which the feedback resistor and the resistor from the inverting input to ground are equal. This configuration provides a closed-loop gain of 2 (or 6 dB). If the noninverting input is grounded and the signal is applied to the bottom of the previously grounded (inverting) input, the amplifier becomes an inverting type, and the gain is unity (or 0 dB). In both cases, the operational-amplifier feedback signal is the same; the external signals and outputs, however, are different. The curves in Fig. 167, therefore, relate to the feedback signal around the amplifier, and the gain scales are changed to reflect external conditions.

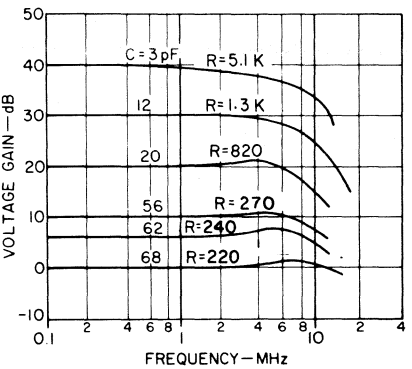


Fig. 168 — Typical response characteristics for a phase-compensated operational amplifier.

Besides the phase-lag compensation techniques described in the preceding paragraphs, phase-lead compensation is also possible with the operational amplifiers. This compensation is accomplished by addition of a capacitor from the base of transistor Q8 to the base of transistor Q9. The effect of this capacitor is to eliminate the break at 10 MHz in the open-loop response and thus extend the 6-dB-per-octave roll-off. The second break in the response then occurs at approximately 35 MHz for ±12-volt operation, and the unity-gain crossover occurs at 150 MHz. The phase-lead-compensated open-loop response is shown in curves (C) and (D) in Fig. 169 for various values of capacitance. For optimum performance, a minimum phase-lead capacitance of 47 picofarads is recommended.

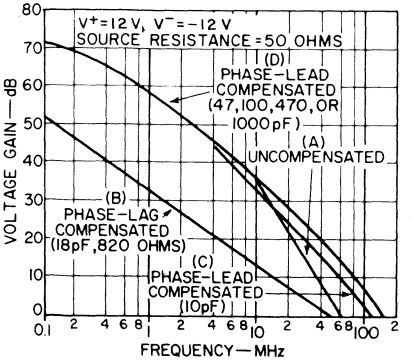


Fig. 169 — Open-loop gain as a function of frequency for compensated and uncompensated operational amplifiers.

For closed-loop gains greater than 30 dB, only a single phase-lead capacitor of 47 picofarads is required for a flat (within ±1 dB) response. Closed-loop gains less than 30 dB require both phase-lead and phase-lag compensation to obtain a flat (within ±1 dB) response. Fig. 170 shows the phase-lag capacitor required and the system response obtained with this compensation.

The phase-lead compensation is also applicable when ±6-volt power supplies are used, and provides a unity-gain crossover improvement of about one octave as compared to the uncompensated connection. As mentioned earlier, the phase-lag capacitance requirement for ±12-volt supplies shown in Fig. 167(a) is satisfactory for ±6-volt supplies, although smaller capacitors could be used with the lower voltages.

Applications of the Low-Power Operational Amplifiers

RCA integrated-circuit operational voltage amplifiers are highly versatile devices that may be adapted to perform a broad variety of circuit functions in telemetry, data processing, instrumentation, and communications equipment. Typical applications include narrow- or wide-band amplifiers, oscillators, multivibrators, comparators, scaling adders, integrators, and differentiators. These amplifiers are normally operated with externally applied negative feedback. An essential requirement in the application of the operational amplifiers is that both inputs have the same effective dc resistance. This condition is necessary to ensure that current offset components are held to a minimum and that maximum dc stability with temperature variations is attained, as discussed in the section on **General Application Considerations.**

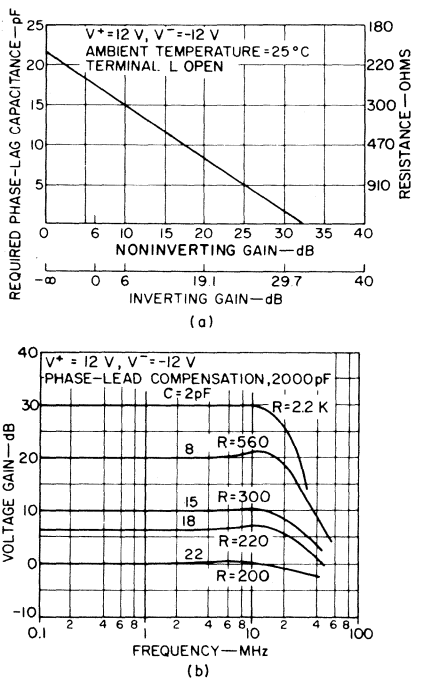
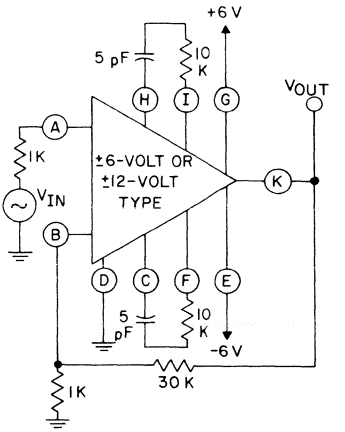


Fig. 170 — Amount of phase-lag capacitance required to obtain a flat (±1-dB) response when phase-lead compensation is used, and typical response characteristics [select series resistor so that $1/(2\pi RC) = 35$ MHz].

The applications described in the following paragraphs illustrate the use of the operational amplifiers for operation from ±6-volt or ±12-volt dc supplies. Operation at other voltages, within the limits of the maximum voltage ratings of the amplifiers, is also possible. The phase compensation shown for operation from ±12-volt supplies can also be used when the amplifiers are operated from ±6-volt supplies without change of the compensation because the amplifiers are conservatively compensated. For optimum performance, however, the compensation may be modified in accordance with the information given in the preceding discussion on **Phase Compensation.** If a circuit that operates from ±6-volt supplies is to be operated from ±12-volt supplies, modification of the phase compensation is usually necessary.



All resistance values in ohms unless otherwise specified.

Video Amplifiers—When the feedback is applied through a purely resistive network and suitable phase compensation is employed, flat gains are attainable from the operational amplifiers. Fig. 171 shows a 30-dB noninverting configuration of a video amplifier, together with the closed-loop response of the circuit. The phase compensation is provided by a 5-picofarad capacitor in series with a 10,000-ohm resistor. This arrangement provides the required amount of compensation, as predicted in Fig. 167(a). (For purposes of comparison, the uncompensated response of the 30-dB configuration is shown in Fig. 172. A 13-dB peaking effect is evident at 4.5 MHz.) An alternate method of phase compensation may be used when the intersection of the closed-loop characteristic and the open-loop response occurs in a two-slope (12-dB-per-octave) region. The technique is to cause the feedback ratio(Z_f/Z_r) to roll off at a slope of

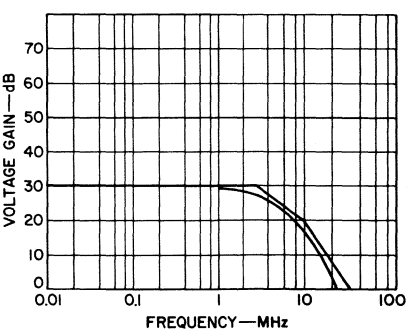
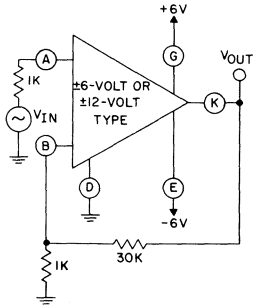


Fig. 171 — Circuit diagram and closed-loop response of a noninverting type of operational amplifier used as a 30-dB video amplifier.

one (6 dB per octave). Fig. 173 illustrates this alternate technique for the 30-dB gain circuit. The low-frequency input impedance of the 30-dB noninverting configuration is 480,000 ohms, as calculated from the appropriate equation in Table XXIII (Z_i = 14,000 ohms).



All resistance values in ohms unless otherwise specified.

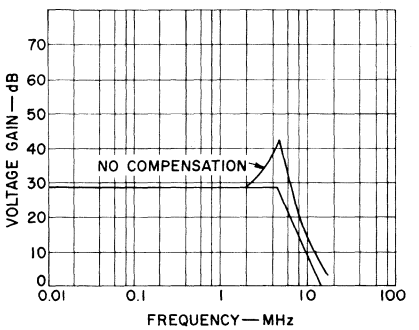
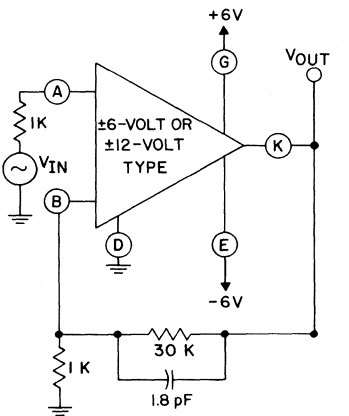


Fig. 172 — Circuit diagram and gain-frequency response of the 30-dB noninverting video amplifier operated without phase compensation.

Fig. 174 shows the configuration and the response of a 6-dB inverting type of video amplifier. The intersection of the closed-loop characteristic with the compensated open-loop response predicts the 3-dB bandwidth of the video amplifier provided the transfer phase shift of the open-loop amplifier is approximately −90 degrees. This relationship suggests a way to extend the bandwidth without peaking. In the 6-dB video amplifier shown in Fig. 175, the 3-dB bandwidth has been increased from 5.6 to 11 MHz by a decrease in the value of the phase-compensating capacitors from 56 to 33 picofarads.

A broad-band amplifier should be capable of handling digital signals. Figs. 176(a) and 176(b) illustrate the pulse-handling capabilities of the 30-dB noninverting circuit shown in Fig. 176. Fig. 176(a) shows the low-level (non-saturating) pulse response. The input is a 38-millivolt, 960-nanosecond pulse; the output is a 1.1-volt pulse having a 40-nanosecond delay time, a zero storage



All resistance values in ohms unless otherwise specified.

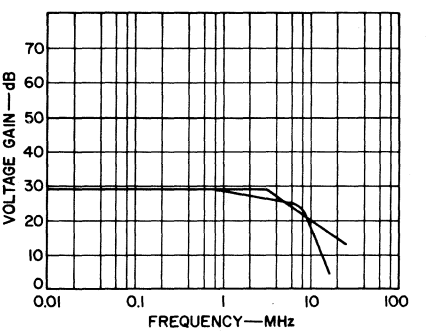
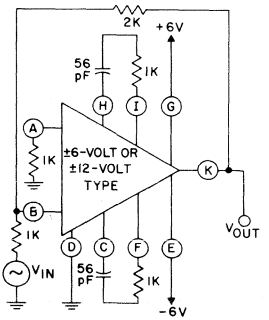


Fig. 173 — Circuit diagram and gain-frequency response of the 30-dB video amplifier when phase compensation is accomplished by addition of a capacitor in parallel with the feedback resistor.



All resistance values in ohms unless otherwise specified.

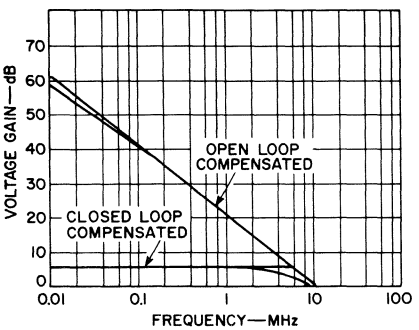
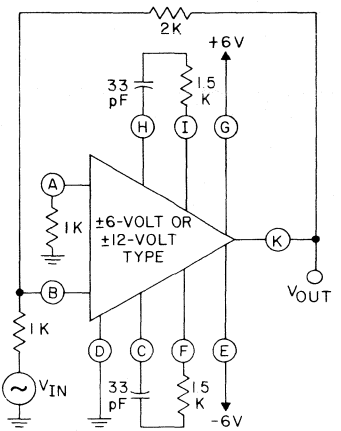


Fig. 174 — Circuit diagram and closed-loop response of an inverting type of operational amplifier used as a 6-dB video amplifier.

time, and 125-nanosecond rise and fall times. Fig. 176(b) shows the response of the amplifier for a 960-nanosecond input pulse under 20-dB overdrive conditions. The output pulse has an amplitude of 3.2 volts, a delay time of 32 nanoseconds, a storage time of 160 nanoseconds, a rise time of 500 nanoseconds, and a fall time of 160 nanoseconds.

50-db Amplifier—Fig. 177 shows the circuit configuration and frequency response for a noninverting, 50-dB amplifier that uses phase-lead compensation. This amplifier has a 3-dB bandwidth of 3.5 MHz, and a unity-gain crossover at 150 MHz.

10-dB, 42-MHz Amplifier—Fig. 178 shows the circuit diagram and frequency response for a 10-dB, noninverting amplifier that employs both phase-lead and phase-lag compensation. Slight peaking (2 dB) occurs for the phase compensation shown.



All resistance values in ohms unless otherwise specified.

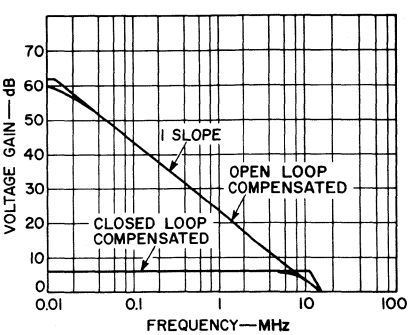


Fig. 175 — Effect of a decrease in phase-compensating capacitance from 56 picofarads to 33 picofarads on the response of the 6-dB video amplifier. (An increase in bandwidth in comparison to that of the circuit shown in Fig. 174 results from the decrease in phase-compensating capacitance.)

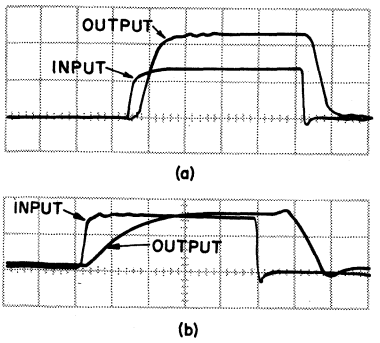
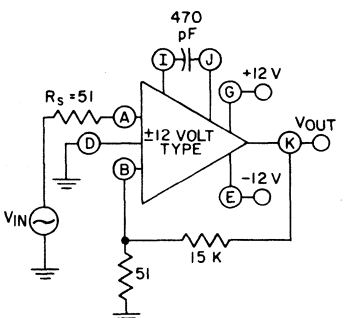


Fig. 176 — Pulse-handling characteristics of the noninverting 30-dB video amplifier: (a) low-level pulse response; (b) pulse response under overdrive conditions.



All resistance values in ohms unless otherwise specified.

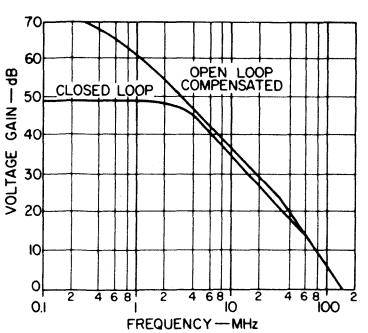
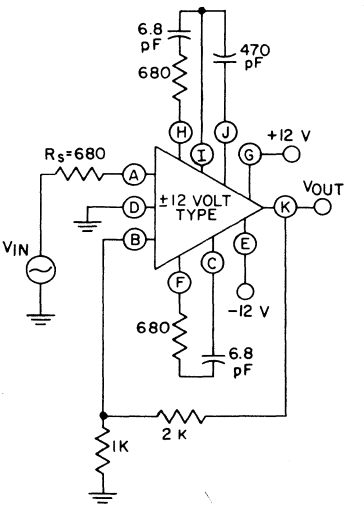


Fig. 177 — Circuit diagram and response for a 50-dB noninverting operational amplifier with phase-lead compensation.



All resistance values in ohms unless otherwise specified.

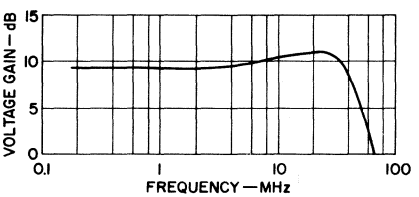
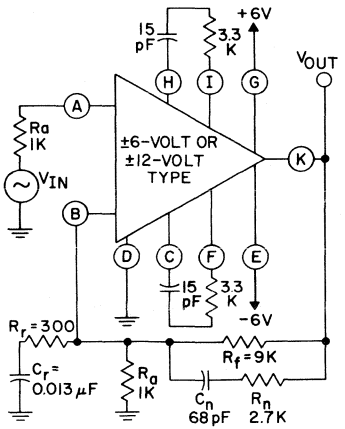


Fig. 178 — Circuit diagram and response for a 10-dB noninverting operational amplifier with phase-lead and phase-lag compensation.

Flat response with bandwidth reduction to 25 MHz may be obtained by use of a phase-lag capacitance of 15 picofarads.

Frequency-Shaping Applications— The operational amplifiers may be used to create simple frequency-shaped characteristics, such as those associated with band-pass, notched-response, and single-tuned narrow-band amplifiers.

Band-Pass Amplifier: Fig. 179 shows a noninverting amplifier that



All resistance values in ohms unless otherwise specified.

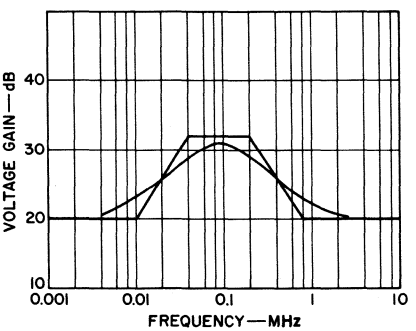


Fig. 179 — Circuit diagram and response of a noninverting type of operational amplifier used to synthesize peaked-response transfer functions.

may be used to synthesize the following peaked-response transfer function:

$$\frac{V_{OUT}}{V_{IN}} = 10\,\frac{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\,\frac{f}{f_4}\right)}{\left(1 + j\,\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

In terms of the notations employed in Fig. 178, the break-frequency equations for the amplifier may be expressed as follows:

$$f_1 = \frac{10}{2\pi C_r(R_f + 10R_r)} = 10\text{ kHz}$$

$$f_2 = \frac{1}{2\pi C_r R_r} = 40\text{ kHz}$$

$$f_3 = \frac{1}{2\pi C_n(R_n + R_f)} = 200\text{ kHz}$$

$$f_4 = \frac{40}{2\pi C_n(40R_n + R_f)} = 800\text{ kHz}$$

These break-frequency equations are the precise equations derived from the gain equation in Table XXIII. The amount of phase compensation required is that shown in Fig. 167(a) for a noninverting gain of 20 dB.

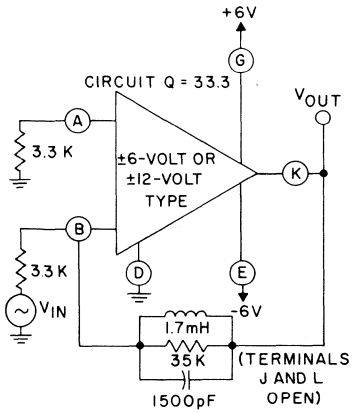
Tuned Amplifier: Fig. 180 shows the circuit configuration and the frequency response of a narrow-band, 100-kHz tuned amplifier. The circuit Q is 33.3. A true single-tuned response can be obtained from only an inverting circuit configuration, as shown by the gain equation for the two types of configurations given in Tables XXII and XXIII and repeated below:

1. For the inverting configuration, the gain equation is given as:

$$\frac{V_{OUT}}{V_{IN}} = -Z_f/Z_r$$

2. For the noninverting configuration, the following gain equation is used:

$$\frac{V_{OUT}}{V_{IN}} = 1 + Z_f/Z_r$$



All resistance values in ohms unless otherwise specified.

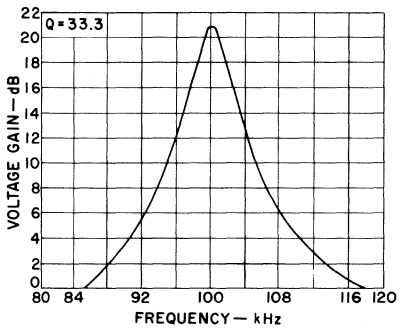
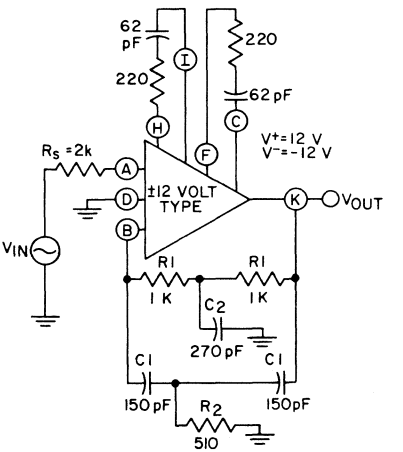


Fig. 180 — Circuit diagram and response of an inverting type of operational amplifier used as a narrow-band 100-kHz tuned amplifier.

The "1+" term in the gain expression for the noninverting configuration indicates that the gain of this type of circuit will never decrease to zero as required for a true single-tuned response. The amount of phase compensation required for the narrow-band 100-kHz amplifier is the value given in Fig. 167(a) for an inverting gain of $-\infty$ (infinite attenuation).

Twin-T Band-Pass Amplifier: Fig. 181 shows the circuit diagram and frequency response of a band-pass amplifier using a twin-T network in the feedback loop. The difference in resonant frequency between the band-pass-amplifier response and the twin-T network response is caused by device capacitances and loading effects. The unloaded Q (Q_O) of the twin-T network is 14.4; the Q_O of the band-pass amplifier is 12.8.



All resistance values in ohms unless otherwise specified.

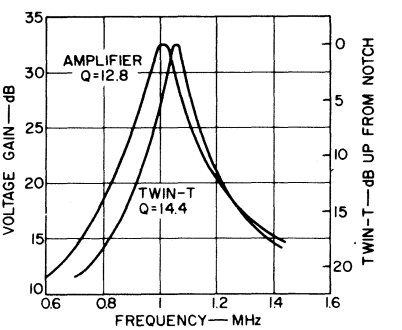


Fig. 181 — Circuit diagram and response for a band-pass amplifier using a twin-T network.

The symmetrical twin-T network can be designed by use of the following equations:

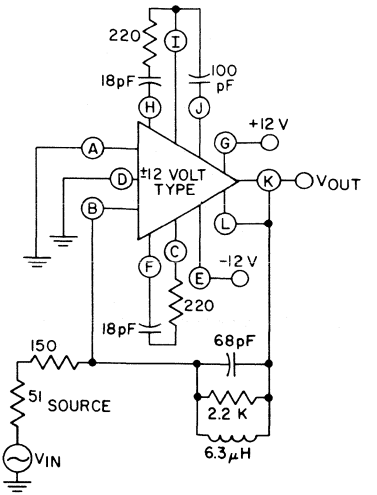
$$R1 = 2\ R2$$
$$C1 = \tfrac{1}{2}\ C2$$
$$f_0 = 1/(2\pi R1C1)$$

It is important in the design of this type of bandpass amplifier that the two inputs be returned to ground through equal resistances; in this case a value of 2000 ohms is used.

20-dB, 10-MHz Band-Pass Amplifier: Fig. 182 shows the circuit diagram and frequency response of an RLC band-pass amplifier. This amplifier is designed to have a Q_0 of about 10 ($R_p = X_c$, $Q_0 = 2200$ ohms) and a gain of about 20 dB at resonance (2200/200 = 11, or 20.9 dB). In this application, the inputs are effectively grounded.

Comparators — The low-power series of operational voltage amplifiers have excellent transfer characteristics for comparator applications. As shown in Figs. 183, there is no observable hysteresis effect; the trace (minus to plus) and retrace (plus to minus) excursions coincide. In addition, slew rates of 30 volts per microsecond are obtainable in the open-loop condition with ±6 volt supplies. Fig. 176 shows the pulse response under closed-loop conditions for a phase-compensated circuit, such as that shown in Fig. 171, with and without overdrive signals. Increased switching speeds will result without phase compensation. Output-stage clamping may also be employed to make the output amplifier compatible with most standard logic levels of digital circuits. Fig. 184 shows these connections.

When the operational amplifiers are operated in the open-loop comparator mode, it is important to observe the common-mode voltage restraints of the input amplifier. With ±6 volts supplies, this voltage is typically +0.5 volt to −4 volts. The differential input voltage may be 5 volts, while the input current should be held to a maximum of 1 milliampere. It must be realized that, if either differential amplifier is saturated, the resulting output may be out of phase with the expected output. This condition results from a



All resistance values in ohms unless otherwise specified.

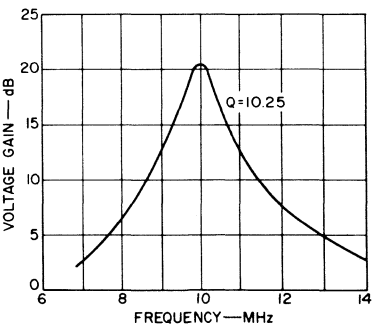


Fig. 182 — Circuit diagram and response for a 10-MHz band-pass amplifier.

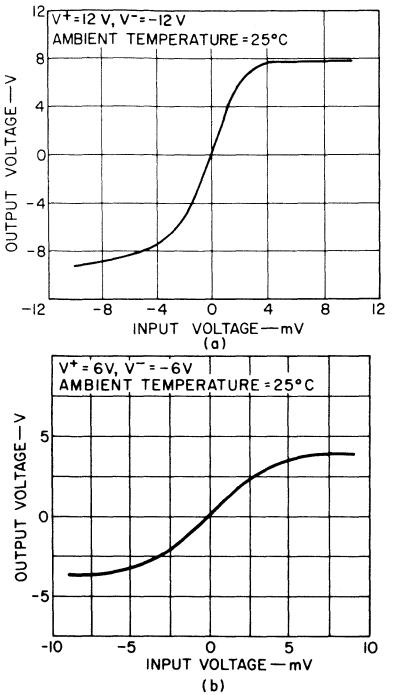


Fig. 183 — Open-loop transfer characteristics: (a) for operation from ±12-volt supplies; (b) for operation from ±6-volt supplies.

shift in the input to the differential amplifier from the normally inverting operation, with transistor action, to a noninverting amplifier under the saturation mode, in which the transistor operates essentially as a diode.

A series RC combination (1000 ohms + 470 picofarads) may be connected between the output and noninverting input (positive feedback) to enhance switching speed.

Integrators—The important design consideration when an operational amplifier is to be used as an integrator is that dc feedback be provided. This feedback is necessary so that an offset (error) voltage cannot continuously charge the feedback capacitance until the amplifier limits. The required dc feedback is normally provided by shunting the integrating capacitor with a resistor so that the resulting time constant is substantially longer than the periods for the frequencies of interest. Fig. 185 shows the circuit configuration for use of the operational amplifier as an integrator and the

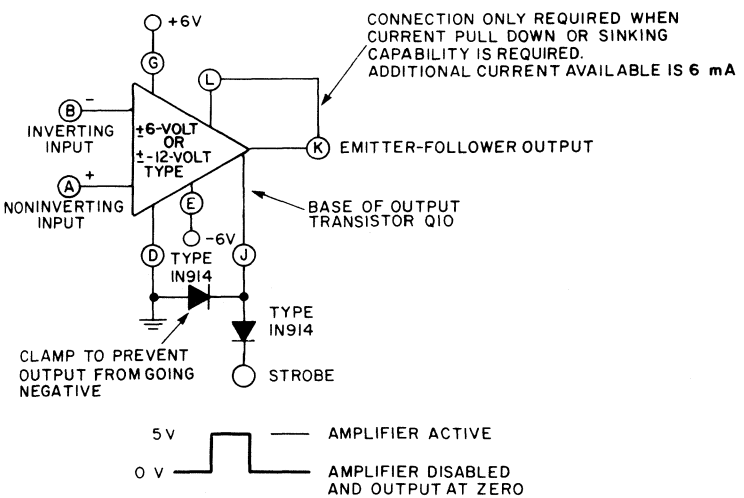
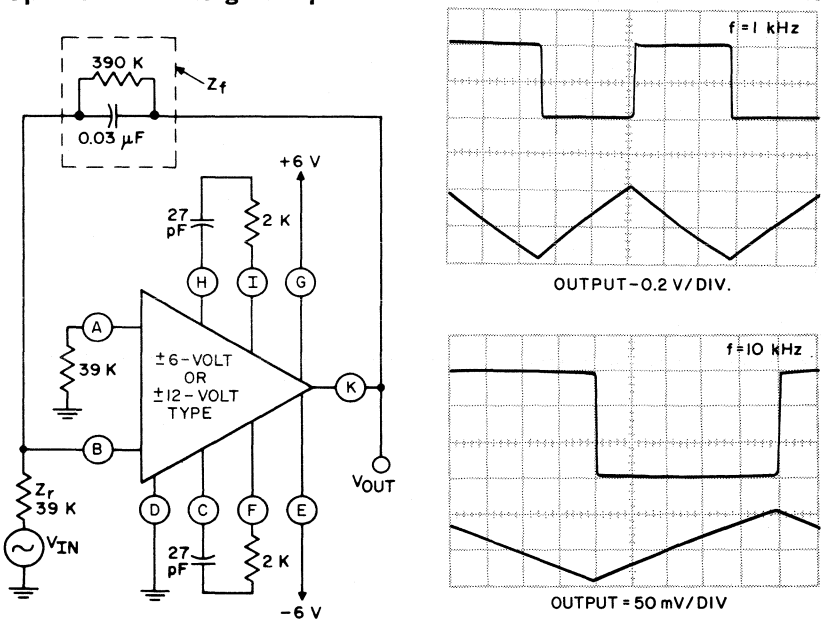


Fig. 184 — Use of output stage clamping to achieve an amplifier output compatible with digital-circuit logic levels.



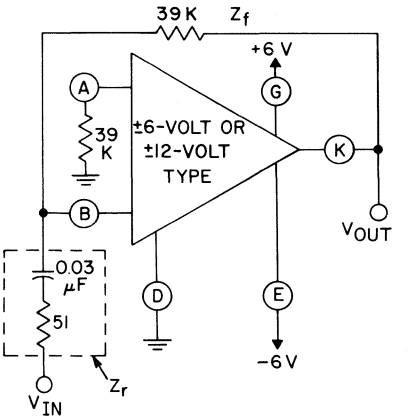
All resistance values in ohms unless otherwise specified.

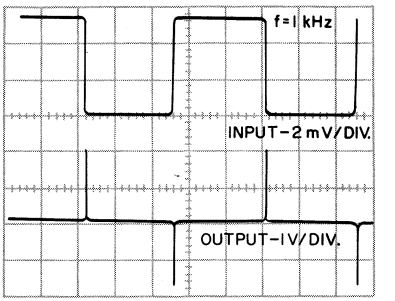
Fig. 185 — Circuit diagram and the input and output waveforms for an operational amplifier used as an integrator.

responses of the circuit for 1-kHz square-wave inputs. The dc gain of the circuit is limited to 20 dB by the 390,000-ohm feedback resistor. The effect of this resistor on the gain, however, becomes negligible for ac signals at frequencies above 13 Hz because of the 0.03-microfarad capacitor in parallel with it. The weighting factor of integration for the circuit is about 1 millisecond (R = 39,000 ohms; C = 0.03 microfarad).

Phase compensation must also be provided in an integrating amplifier circuit to assure ac stability. In general, the amount of compensation required is the maximum value given by Fig. 177(a), because the closed-loop characteristic of the integrator has rolled off completely at the frequency at which the intersection of the open-loop response and the closed-loop characteristic occurs.

Differentiators—The main problem in the design of differentiating amplifiers is that the gain of such amplifiers increases with frequency; as a result, they are susceptible to high-frequency noise. The classical remedy for this effect is to connect a small resistor in series with the input capacitor so that the high-frequency gain is decreased. Actually, the addition of the resistor results in a more realistic model of a differentiator because a resistance is always added in series with the input capacitor by the source impedance. The schematic diagram of an operational amplifier used as a differentiating circuit and the response of the circuit for 1-kHz square waves are shown in Fig. 186. A value of 51 ohms is selected for the gain-limiting resistor to illustrate that the effect of the source impedance is not necessarily negligible in differentiator ap-





All resistance values in ohms unless otherwise specified.

Fig.186 — Circuit diagram and the input and output waveforms for an operational amplifier used as a differentiator.

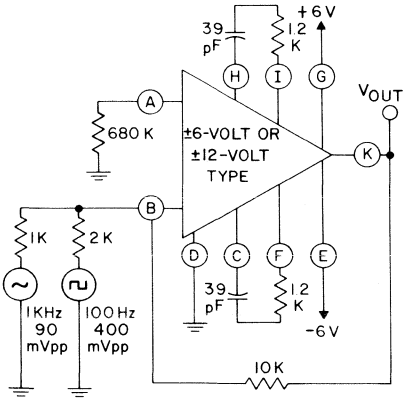
plications. This 51-ohm resistor limits the high-frequency numerical gain factor of the amplifier to 433.

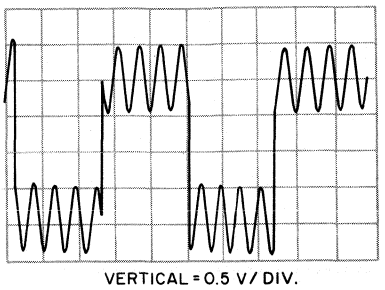
If the closed-loop gain of a differentiator rises to the open-loop value before the open-loop response has started to roll off, no phase compensation of the circuit is required. In order to assure that the intersection of the closed-loop characteristic with the open-loop respons occurs at a slope less than two, the RC time constant of the phase-compensating network must be adjusted so that the open-loop response does not roll off in the region of the intersection.

Scaling Adders—The inverting feedback configuration of the operational amplifiers lends itself not only to summing several different signals, but also to weighting each signal to be summed. The weighting operation is possible because the virtual ground (discussed in the section on the **Ideal Operational Amplifier)** that exists at the junction of the feedback resistor and the inverting input isolates each signal channel from the others. The weighting operation requires that each input signal enter the virtual-ground node through an impedance of such value that its ratio to the feedback impedance is equal to the desired weighting factor.

Fig. 187 illustrates the use of an operational amplifier as a scaling adder (weighting amplifier). This figure also shows the output waveform. The minimum phase compensation needed for this circuit is that required for the gain obtained when a single signal drives all the input channels in parallel.

Emitter-Follower Input—An emitter-follower input configuration, when used with the operational amplifier, offers both low bias current and a corresponding increase in input impedance. Input current decreases by a factor of $(\beta + 1)$, and the impedance rises by the same factor. Addition of another emitter-follower further extends the multiplying factor to approximately β^2. By use of a single RCA 3018A integrated-circuit transistor array, the minimum input impedance of the ±6-volt operational amplifiers can be increased to greater than 10 megohms and the input bias current can





All resistance values in ohms unless otherwise specified.

Fig. 187 — Circuit diagram and output waveform for an operational amplifier used as a scaling adder.

be decreased to less than 10 nanoamperes. These changes, however, cause both the offset voltage and the offset-voltage drift to increase. Drift rate of the amplifier at 25°C is about 0.5 microvolt per °C for the operational amplifier alone. The added emitter-followers should contribute an additional drift of 1 to 10 microvolts per °C. Fig. 188 shows this configuration.

The impedance levels are usually high because of the low current levels. The high-frequency response of the amplifier combination, therefore, decreases considerably, and another two time constants are introduced by the 10-picofarad input capacitance and low-operating-current emitter-follower output impedance. An additional time constant is also formed between the next input to the intermediate emitter-follower and the associated stray capacitance. The first pole in the amplifier response appears at 300 kHz, the next pole occurs at 3 MHz, and the external emitter-follower circuits contribute two more poles between 1 and 5 MHz.

An open-loop unity-gain crossing should appear between 0.5 and 1 MHz to assure stable unity-gain operation. The 3-dB bandwidth would then be set to 500 Hz. The Miller compensation capacitor would then be 1000 picofarads and the value of the series resistor should be selected so that $1/(2\pi RC)$ is equal

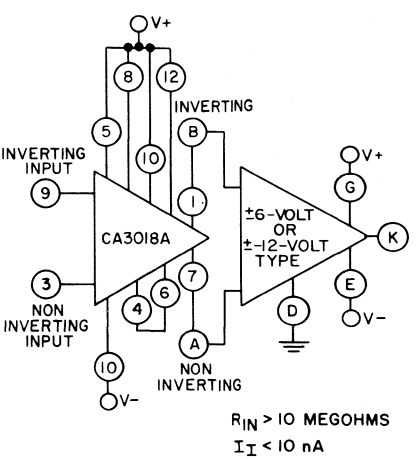
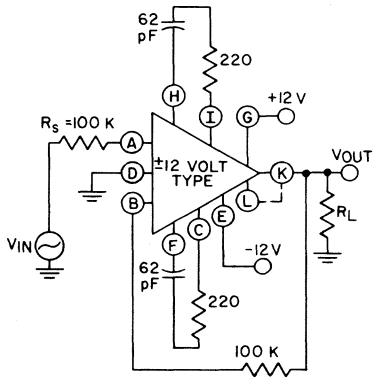


Fig. 188 — Use of a CA3018A transistor array to provide an emitter-follower input for the operational amplifier.

to 1 MHz, i.e., a resistance of 150 ohms. A single 0.2-microfarad capacitor added to the base of the operational-amplifier emitter-follower output to ground will also compensate the amplifier.

Voltage Follower—Impedance transformation and signal isolation are the main functions of the voltage follower. An operational amplifier used to provide this type of function is operated in the noninverting gain configuration. This type of circuit affords the highest input impedance of all operational-amplifier configurations. Input impedances of the operational-amplifier voltage follower can easily approach the megohm range. The resulting base current then becomes the limiting factor in the realization of this high impedance, because the base current must be supplied by the signal source or some resistance.

Fig. 189 shows a voltage follower with a calculated input impedance of 30 megohms. This circuit illustrates the case for which the base current is large with respect to the input impedance. In fact, the voltage drop across the two 0.1-megohm resistors produced by the base current provides the positive signal swing above the 0.5-volt positive common-mode range. As the base current decreases, the positive common-mode signal swing approaches the 0.5-volt level as a limit. If some signal gain is provided to this circuit, the input signal excursions are reduced, and the output swing then becomes the limiting factor. Gain is provided by placement of a resistor from the inverting input to ground. If this resistor is also made equal to 0.1 megohm, the stage gain will be two. The source resistance R_S should be made equal to the parallel combination of the other two resistors (i.e., 50,000 ohms) to insure that dc balance is maintained. Input impedance will decrease to 15 megohms.



All resistance values in ohms unless otherwise specified.

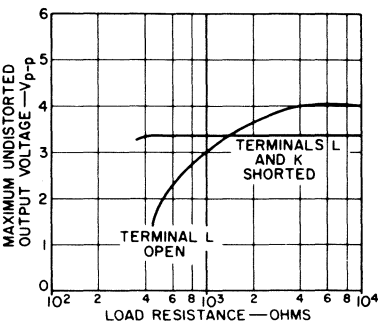


Fig. 189 — Circuit diagram for a voltage follower driven from a 100,000-ohm source, and curve showing maximum undistorted output voltage as a function of load resistance.

Higher-Power-Output Types

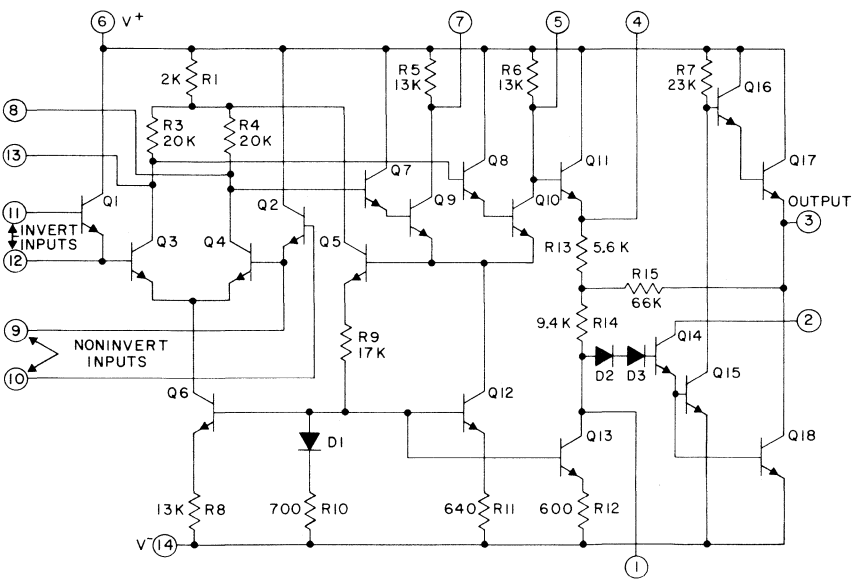
The CA3033 and CA3033A operational amplifiers, supplied in dual-in-line ceramic packages, and the CA3047 and CA3047A operational amplifiers, supplied in dual-in-line plastic packages, offer the user an improved amplifier with respect to breakdown voltages, higher input

impedance with reduced input current, and high power-output capability. These operational amplifiers allow the user to select either a ±12-volt device (CA3033 or CA3047) or a device (CA3033A or CA3047A) that can operate up to ±15 volts with power output up to at least 220 milliwatts. Input impedance is typically 1.5 megohms, and the corresponding bias current is 100 nanoamperes. With the exception of these differences, the four operational amplifiers are identical.

Circuit Description—The operational amplifiers consists of two differential-amplifier stages followed by a class B output stage, as shown in Fig. 190. Emitter-follower inputs provide the exceptionally high input impedance and low bias current. An additional advantage of the emitter-follower inputs is that the Miller capacitance of the differential amplifier is substantially reduced by the h_{fe} of transistors Q1 and Q2; therefore, the input capacitance of the amplifier is lower than if a similar single-transistor configuration were used.

The output of the first differential-amplifier stage (Q3 and Q4) is buffered from the input of the next differential-amplifier stage (Q9 and Q10) by emitter followers Q7 and Q8. This arrangement reduces the input-loading effects on the first stage and therefore maintains the first-stage gain.

A circuit is incorporated in this design to sense any change in the operating point of the first differential amplifier caused by variations in either the positive or the negative supply voltage. Any changes in the supply voltages are reflected to the base of transistor Q5, which detects



All resistance values in ohms unless otherwise specified.

Fig. 190 — Higher-power-output integrated-circuit operational amplifiers (CA3033, CA3033A, CA3047, and CA3047A).

changes in the collector voltage of the first differential amplifier and compensates for them. For example, a rise in the voltage at the emitters of Q9 and Q10 increases the bias voltage to Q5 and thus increases the collector current, countering the apparent rise in the collector voltage of either Q3 or Q4. At the same time, the emitter current of Q5 also increases, and increases the voltage drop across the diode D1, transistor Q9, and resistor R10 to increase the collector current of Q6. Thus, any apparent increase in the collector voltage of the first differential stage causes a correction both at the constant-current source Q6 and at the collector supply voltage through R1, the common load resistor for Q3, Q4, and Q5.

An emitter-follower Q11 buffers the output of the second differential-amplifier stage and drives the divider and summing network to the output stage. Resistor R13 may be considered the input resistance of an amplifier to the summing point, the junction of R13, R14, and R15. Resistor R14 shifts to the operating point of the output stage with little attenuation of the signal as a result of the high collector impedance of the constant-current source transistor Q13.

Diodes D2 and D3 provide further dc shifting of the signal to the base of emitter-follower Q14. This emitter-follower provides further level shifting and a low driving impedance to transistors Q15 and Q18.

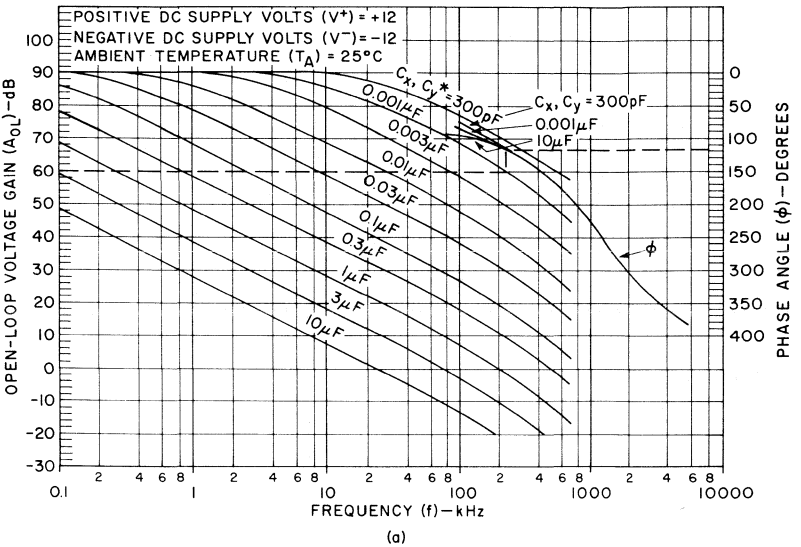
The excellent matching of the base-to-emitter voltage of the integrated-circuit transistors makes it possible to establish the idling current of the output stage accurately. Because the collector-current characteristics of Q15 and Q18 as a function of base-to-emitter voltage are matched, the collector current in Q15 determines the idling current in Q18. For example, if the operating current of Q15 is set at 1 milliampere for a given base-to-emitter voltage, the operating current of Q18 is also 1 milliampere because the base-to-emitter voltages of both transistors are the same. This type of design results from the excellent transistor matching that is possible with monolithic processing.

Thermal stabilization of the output stage is accomplished by a proper choice of resistor values to offset the thermal variations in the input bias voltages at the bases of transistors Q11 and Q13 as well as the inherent variations in the output stage.

The use of a negative feedback resistor in the output stage aids in thermal stabilization, sets the voltage gain, and enables the use of a wide range of power-supply values. Feedback resistor R15 is placed between the output and the virtual ground in the level-shift circuitry (junction of R13 and R14). The voltage gain with R15 in place is essentially R15/R13, regardless of which channel is conducting, provided the positive-negative channel open-loop gains are larger than the ratio.

The output stage will operate properly over a wide range of power-supply values because the collector voltage of Q13 is essentially clamped to the negative supply through the diodes D1 and D2 and transistors Q14, Q15, and Q18. Only a few millivolts are required at the collector of Q13 to cover the entire range of Q15 and Q18, from cutoff to saturation. The feedback can effect this change of a few millivolts, forcing a balance between output transistors Q17 and Q18.

Phase Compensation—Basic phase compensation of the higher-power-output types of operational amplifiers is relatively simple. Fig. 191(a) shows typical phase-compensation



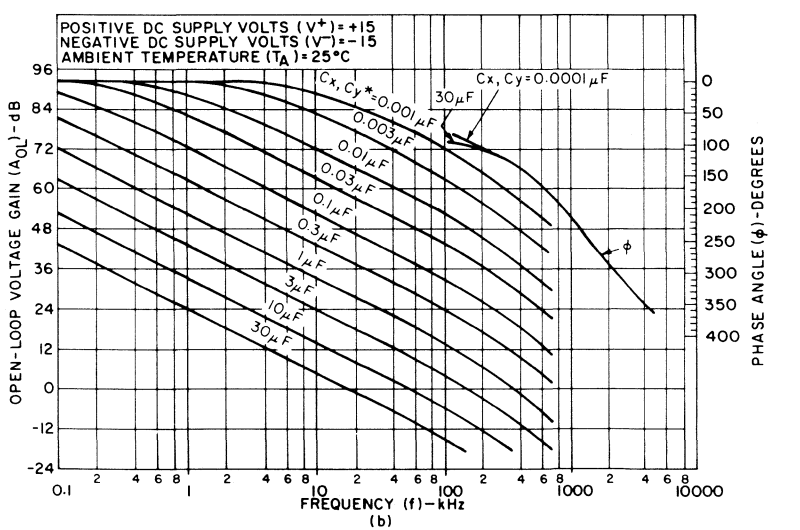


Fig. 191 — Typical phase compensation characteristics: (a) for the CA3033 or CA3047; (b) for the CA3033A or CA3047A.

characteristics for the CA3033 and CA3047; data for the CA3033A and CA3047A are as shown in Fig. 191(b). The two compensating capacitors C_x and C_y are connected from the collectors of the first differential amplifier (terminals 8 and 13) to ground. When capacitance values greater than 0.1 microfarad are used, however, a lower-voltage capacitor that has a value equal to half that given on the curves may be connected between terminals 8 and 13, and a 0.001-microfarad capacitor connected from either terminal 8 or 13 to ground or V^- (terminal 14). This arrangement provides the same gain-phase roll-off shown on the curves and permits the use of lower-voltage ceramic disc capacitors now available. For linear operaton, the maximum expected difference voltage between the two collectors is less than 1 volt.

The dashed lines in Fig. 191(a) illustrate the use of the curves for design of a 60-dB amplifier. First, the intersection of the various gain-frequency curves is followed out to the curve for a capacitor value of 0.001 microfarad. At this point, the expected 3-dB amplifier response is approximately 230 kHz, and the phase angle ϕ is 118 degrees. The phase margin ($180° - \phi$), therefore, is 62 degrees. For a capacitance value of 300 picofarads, the expected 3-dB response is 580 kHz, but the phase angle is 175 degrees. The resulting phase margin of only 5 degrees is a most undesirable situation. In the other direction, the use of 0.003-microfarad compensating capacitors provides a 3-dB response of 90 kHz and a phase angle of approximately 90 degrees, with a phase margin of 90 degrees.

In some systems, large parasitic supply impedances prevent effective compensation. In such systems, it is recommended that the phase-compensating capacitors be returned to V^- (terminal 14) instead of to ground.

Slewing Rate—As mentioned in the section on **General Application Considerations,** slewing rate is an important consideration of an operational amplifier, particularly in relation to the limitation it imposes on the operating frequency for full power output (for a sine wave, $SR = \pi f V_{pp}$). If the maximum peak-to-peak value of a sine-wave output voltage is known at some high frequency at which the full dc peak-to-peak output is not realizable, the slewing rate can be used to predict the peak-to-peak output at some other frequency. Fig. 160 in the section on **General Application Considerations** shows a graphic representation of the equation for slewing rate.

Slewing rate is a function of the phase-compensation circuit, the operational-amplifier design in terms of the gain after phase compensation, and the output-stage design. The phase-compensation circuit is usually placed around the input stages of an operational amplifier. This approach offers two advantages. First, it reduces the amplitude of any higher-frequency components that may overload the following stages. (For example, the residual rf carrier remaining on the output of a video detector with a single RC roll-off could cause serious overload and a distorted output if it were allowed to continue through the amplifier). Second, because of the relatively high gain that follows the compensating circuit in the input stage, the compensating capacitors charge and discharge on a smaller and faster portion of the RC time constant associated with the collector load resistors and compensation capacitors.

Another consideration that influences the slewing rate is the signal-

handling capability of the output stage. It is evident that, regardless of how fast the first portion of an amplifier responds to a step input, the output stage can limit the rate of rise and fall.

Fig. 192 shows a curve of the maximum full-power-output frequency of the operational amplifiers as a function of the phase-compensation capacitance. This curve may be used with the curve of Fig. 160 to

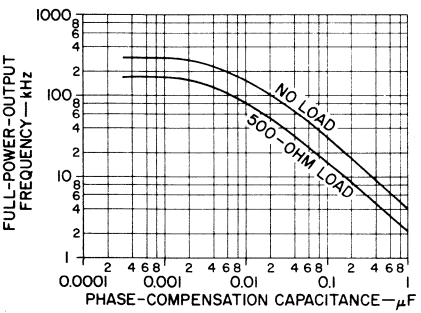
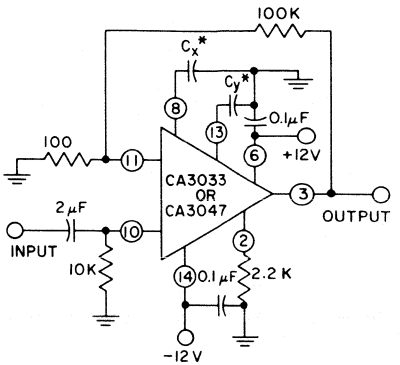


Fig. 192 — Frequency for full power output as a function of phase-compensating capacitance.

determine the amplifier slewing rate. In the case of the 60-dB amplifier shown in Fig. 193, for example, two 0.002-microfarad capacitors are used for phase-compensation. The curves of Fig. 190 indicate that the 3-dB bandwidth is 120 kHz. Fig. 192 shows that full output swing with no load may be expected up to a frequency of 280 kHz. Therefore, the design is capable of full power output up to the 3-dB point.

A similar approach may be used for a pulse amplifier. Two 0.01-microfarad phase-compensating capacitors are used to yield a 3-dB response of 30 kHz. The expected rise time in microseconds is equal to 0.35 divided by the 3-dB fre-



All resistance values in ohms unless otherwise specified.

Fig. 193 — 60-dB test amplifier for CA3033 or CA3047.

quency in MHz, or 11.7 microseconds. The power-output curve of Fig. 192 shows that the maximum frequency for full power output is 155 kHz; thus the slewing rate is 10.6 volts per microsecond. For the 20-volt input-signal swing specified for the CA3033 and CA3047, the rise time based on this slewing rate would be (1 microsecond/10.6 volts) x 20 volts, or 1.9 microseconds. Because this value is greater than the rise time estimated from the 3-dB point, the design is not slewing-rate limited, and the 3-dB rise time will be met. Thus, for maximum high-frequency output, the lowest value of phase-compensation capacitors must be used; therefore, high closed-loop gains are implicit. Waveforms for the 60-dB amplifier are shown in Fig. 194.

Applications—Fig. 195 illustrates the use of the CA3033A and CA3047 in a 20-dB, 255-milliwatt power amplifier operating from a single 30-volt supply. Fig. 196 shows the pulse response of this amplifier under no-load conditions and with a resistive

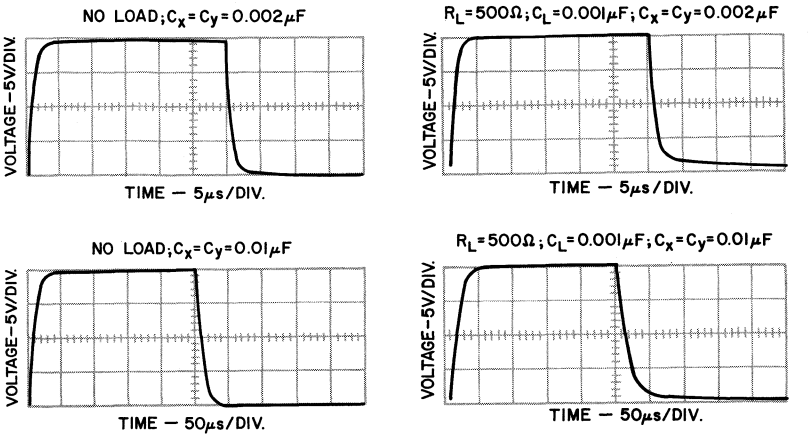
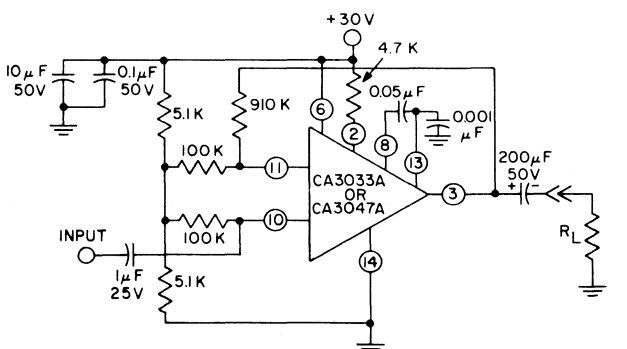


Fig. 194 — Waveforms for the 60-dB amplifier shown in Fig. 193.

load of 500 ohms; also shown are curves of distortion as a function of frequency. The waveforms show that the pulse response of the amplifier is limited by slewing rate rather than frequency response. Some crossover distortion is evident in the response for the 500-ohm load.

The impedance of the feedback network can have a significant effect on the pulse response of a given amplifier design, particularly when higher-frequency performance is required. The response is influenced by the stray capacitance of the associated wiring, the shunt capacitance of the feedback resistors, and the input impedance of the operational amplifier. Because these operational amplifiers have higher input impedance as a result of the emitter-follower inputs, the input capacitive loading is reduced considerably and higher-impedance feedback networks can be used.

The CA3033, CA3033A, CA3047 and CA3047A operational amplifiers have extremely high peak pulse-cur-



All resistance values in ohms unless otherwise specified.

Fig. 195 — 20-dB, 255-milliwatt power amplifier using a CA3033A operating from a 30-volt supply.

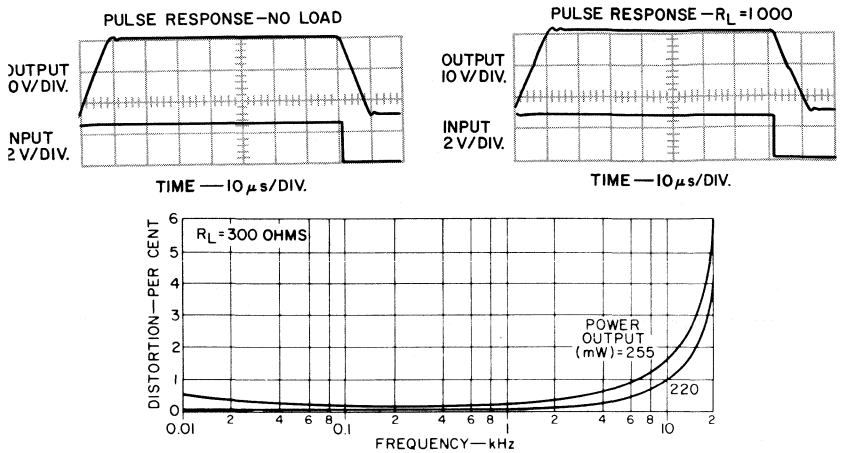


Fig. 196 — Pulse-response waveforms and distortion curves for the amplifier shown in Fig. 195.

rent capability; no means, therefore, are provided for protection of the output circuit of these devices. Typical open-loop output impedance is less than 30 ohms at 10 kHz. Peak short-circuit currents can exceed 100 milliamperes. An external series current-limiting resistor, usually 51 ohms, is employed to assure that the output circuit does not substain prolonged shorts. The next consideration then is to assure that the amplifier dissipation remains within its ratings. When high peak output currents are required of the amplifier, it is desirable to provide a current-limiting resistor of about 2200 ohms in series with the collector of transistor Q14. This resistor may be returned to ground, or, if its value is increased to 4700 ohms, it may be returned to the V^+ terminal.

A simple system is described in the following paragraphs to illustrate the ease with which these operational amplifiers may be applied. The basis of the system is the rudiments of a digital voltmeter, using the linear staircase approach, without the associated totalizing circuitry.

Fig. 197 shows a block diagram of the system, together with the waveforms of all interfaces. A squelchable integrated-circuit multivibrator is used as the clock. As described later, the clock frequency is independent of supply voltage. Although this independence is not a necessary condition for circuit operation, it is inherent in this type of operational-amplifier multivibrator circuit and may be considered an integrated-circuit bonus.

The output from the clock drives a linear staircase generator. Input voltage to this circuit is applied directly from the multivibrator to minimize the effects of diode temperature coefficients. The output from the staircase generator is applied to a comparator that compares the staircase with the voltage to be measured.

The comparator output fires a monostable multivibrator that controls the display time, which is variable from about 100 milliseconds to one second. An inverter following the multivibrator supplies drive of the correct polarity to the integrator capacitor-discharge switch and the multivibrator squelch circuit.

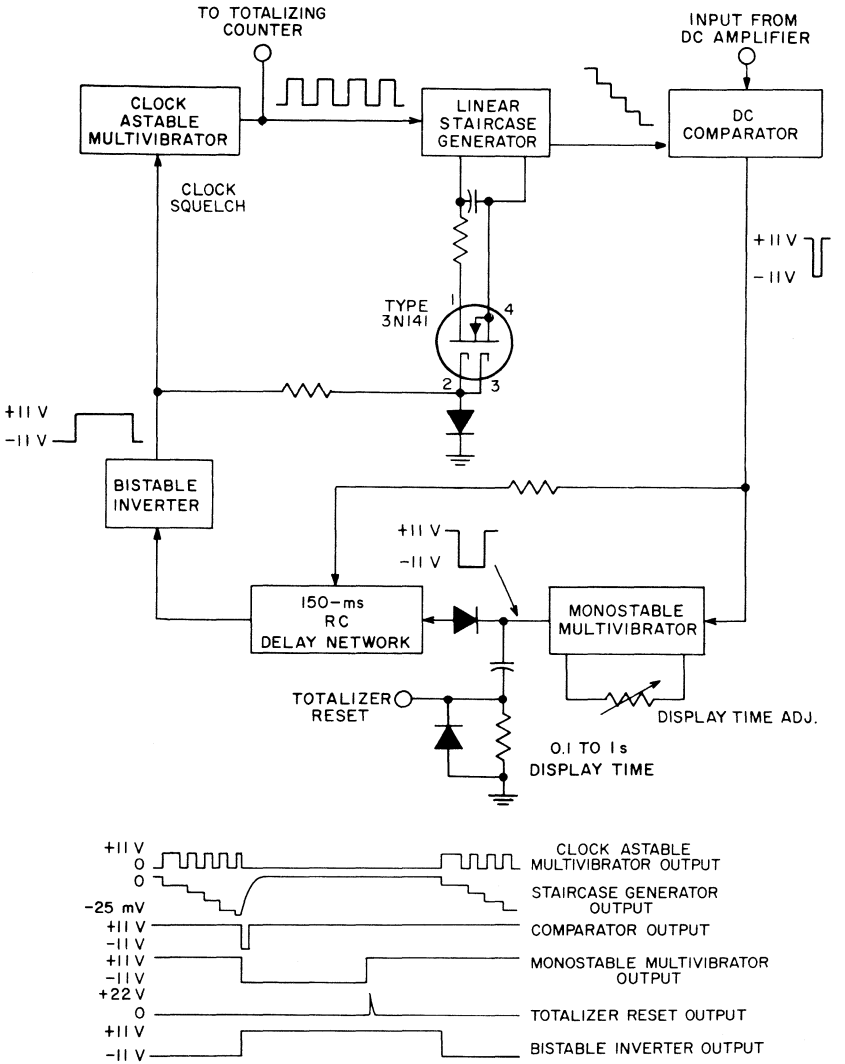


Fig. 197 — Block diagram and waveforms of digital voltmeter system using five CA3033 or CA3047 integrated circuits.

Circuit operation begins with the staircase generator ramp running down until its voltage is equal to the unknown voltage on the input of the comparator. When the two voltages are equal, the monostable multivibrator is triggered by the output from the comparator. The output of the monostable multivibrator squelches the astable multivibrator and discharges the integrating capacitor through the bistable multivi-

brator. The wait, or display time, set by the monostable multivibrator allows sufficient time for full discharge of the integration capacitor and appears as a steady reading on the display device.

A schematic diagram of a squelchable multivibrator is shown in Fig. 198. The only requirement that must be met by the squelch circuit is that the amplitude of the output pulse not change as a result of the squelch operation; otherwise, the amplitude of the final steps would be different from that of the initial steps and staircase linearity would suffer.

Freedom of the circuit from supply-voltage variations results from the excellent saturation characteristics of the integrated circuit at both positive and negative output swings. The positive and negative thresholds of the circuit are given by

Positive threshold =

$$(V^+ - V_{(+sat)})\frac{R1}{R1 + R2}$$

Negative threshold =

$$(V^- + V_{(-sat)})\frac{R1}{R1 + R2}$$

where V^+ and V^- are the positive and negative supply voltages and $V_{(+sat)}$ and $V_{(-sat)}$ are the positive and negative saturation voltage drops of the amplifier. Because these saturation voltages are low and have temperature coefficients less than 5 millivolts per °C, they can be neglected for ease of computation. If the charging current is considerably greater than the base current, the frequency f may be expressed as follows:

$$f \approx \frac{1}{2\,RC \ln\left(\frac{2R1}{R2} + 1\right)}$$

The design of a linear staircase generator is nearly identical to that of a linear ramp or sawtooth generator. Fig. 199(a) shows a linear ramp generator (an integrator) in which the noninverting input of an operational amplifier is grounded and a switch S1 returns the output to the inverting input. When S1 is closed, the amplifier is in the unity-gain configuration, and the output is at ground less the input offset volt-

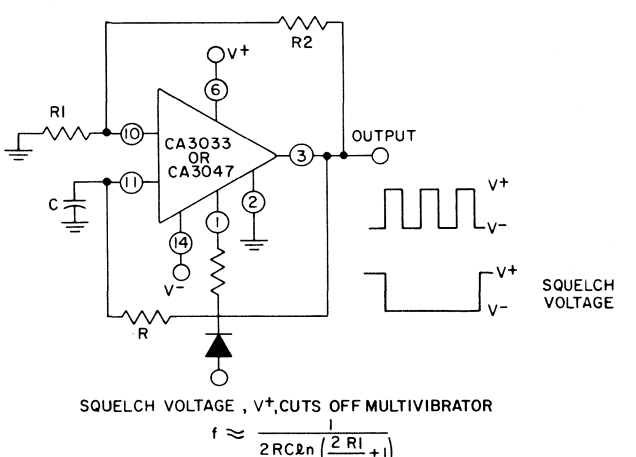


Fig. 198 — CA3033 or CA3047 squelchable astable multivibrator.

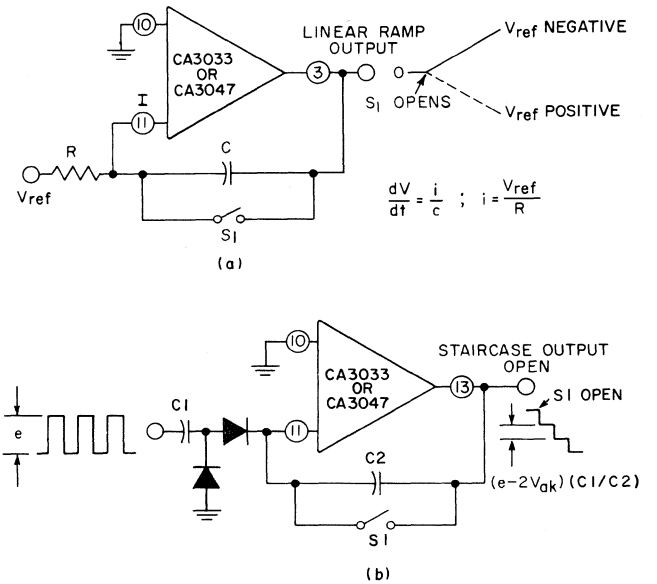


Fig. 199 — Diagrams of (a) linear ramp generator and (b) linear staircase generator.

age. When S1 is opened, the output moves in the positive direction when the reference voltage V_{ref} is negative, or in the negative direction when V_{ref} is positive. Because the output under closed-loop conditions tries to maintain the input terminal at zero voltage, the charging current to the capacitor is constant at a rate of $dV/dt = i/C$, where $i = V_{ref}/R$. It is apparent that this analysis is valid as long as the input current to the first stage is considerably less than the charging current.

Fig. 199(b) shows the circuit for a linear staircase generator. In this circuit, a pulse of amplitude e couples a charge Q to the amplifier input. The charge Q is equal to $C1\ (e - 2V_{ak})$, where $2V_{ak}$ is the forward voltage drop across the two diodes. Again, if the amplifier input current is small compared to the effective charging current, capacitor C2 is incrementally charged in steps of $(e - 2V_{ak})\ C1/C2$. If the pulse height is made sufficiently large compared to the expected temperature variations of the diodes, a reasonable degree of temperature independence results.

Regeneration is added around the comparator circuit in this system to accelerate the transition time when the two input voltages are equal. Fig. 199 shows a complete schematic diagram of the entire system. Waveforms at critical points are shown in Fig. 201. The 470-picofarad capacitor and 1000-ohm resistor between terminals 3 and 10 of the CA3033 in the comparator circuit provide the regeneration. Two 0.001-microfarad capacitors on each input filter any externally generated noise.

The monostable multivibrator circuit shown in Fig. 200 makes use of the extremely low input bias currents of the CA3033 by using small timing capacitors and large timing

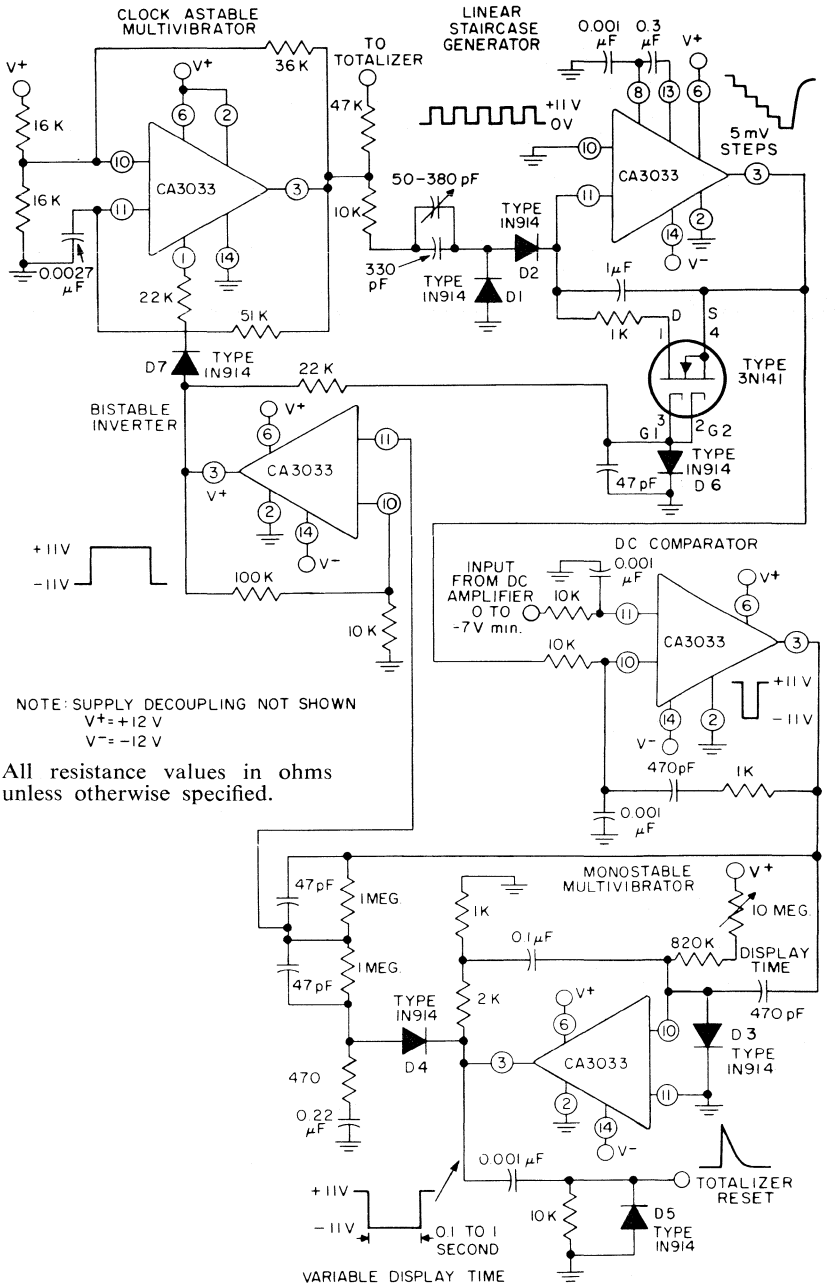


Fig. 200 — Schematic diagram of a digital voltmeter using CA3033 (or CA3047) integrated circuits.

resistors to obtain the long (one-second) display time. The small timing capacitor in conjunction with the diode D3 permits the fast recycling time necessary for the one-step case. Triggering of the circuit is accomplished by the 470-picofarad capacitor to the non-inverting input (terminal 10).

An RC timing network is incorporated at the output of the monostable multivibrator to add an additional 150-millisecond delay that performs two functions. First, the added delay allows more time to complete the timing-capacitor recycling mentioned above. The second and more important function of this network is the generation of a reset pulse at the trailing edge of the monostable multivibrator. Diode D4 couples the negative output of the multivibrator to the next stage and rapidly charges the 0.22-microfarad network timing capacitor through the 470-ohm resistor. After the monostable multivibrator completes the cycle, diode D4 disconnects, and the 0.22-microfarad capacitor charges to the 1.1-volt switching threshold of the next stage through the two one-megohm resistors. This cycle is approximately 150 milliseconds.

The output from the monostable multivibrator is coupled to the next stage, a bistable multivibrator or inverter. The switching thresholds are determined by the 100,000- and 10,000-ohm resistors in the positive feedback loop. The primary function of this stage is to invert the signals from both the comparator and the monostable multivibrator to drive the clock-astable-multivibrator squelch circuit and the staircase capacitor-discharge switch, an RCA-3N141 dual-gate MOS field-effect transistor. Diode D6 protects the gates of the MOS transistor; the 47-picofarad capacitor reduces the rise time of the negative-going output of the bistable multivibrator and prevents it from coupling into the beginning of staircase and obscuring the first few steps by this negative transition.

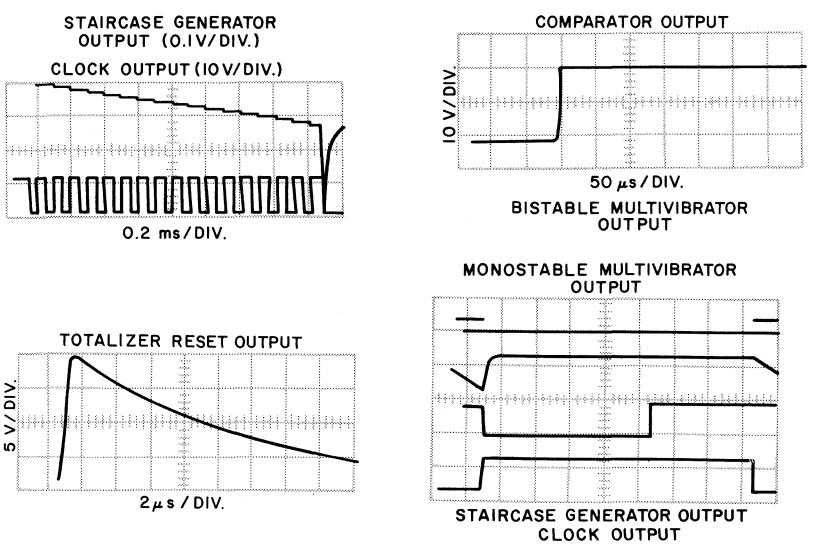


Fig. 201 — Waveforms for the digital voltmeter shown in Fig. 200.

Operational Transconductance Amplifier

The RCA integrated-circuit operational transconductance amplifier (OTA) represents an entirely new concept for operational-amplifier devices. This circuit has all the generic characteristics of the operational voltage amplifier (OVA) described in the preceding section except that the forward transfer characteristic is best described by transconductance rather than voltage gain. The output of the operational transconductance amplifier is a current, the magnitude of which is equal to the product of transconductance and the input voltage (i.e., $i_{out} = g_m e_{in}$). The output circuit of this amplifier, therefore, may be characterized by an infinite-impedance current generator, rather than the zero-impedance voltage generator used to represent the output circuit of an operational voltage amplifier. The low output conductance of the operational transconductance amplifier permits the circuit to approach the ideal current generator.

When the operational transconductance amplifier is terminated in a suitable resistive load impedance and provisions are included for feedback, its performance is essentially identical in all respects to that of an equivalent operational voltage amplifier. The electrical characteristics of the OTA circuits, however, are functions of the amplifier bias current. In the integrated-circuit OTA, therefore, access is provided to bias the amplifier by means of an externally applied current. As a result, the transconductance, amplifier dissipation, and circuit loading may be externally established and varied at the option of the user. This feature adds a new dimension to the design and application of operational-amplifier circuits. The brief summary of the goals of ideal OTA and OVA circuits shown in Table XXV points out the basic similarities and the significant differences of these amplifiers.

BASIC OTA CIRCUIT

The basic circuit for an operational transconductance amplifier is shown in Fig. 202. An understanding of this circuit is best obtained by analysis of voltages and currents with almost complete disregard for voltage gain and impedance levels.

Transistors Q1 through Q4 perform conventional functions, serving as a current mirror, a constant-current source, and a differential pair An amplifier bias current is exter

Table XXV — *Comparison of OTA and OVA Circuits*

	OTA		OVA
INPUT IMPEDANCE	———	HIGH	———
INPUT BIAS CURRENT	———	LOW	———
OFFSET VOLTAGE	———	0	———
GAIN	HIGH TRANSCONDUCTANCE		HIGH VOLTAGE GAIN
BANDWIDTH	———	INFINITE	———
SLEW RATE	———	INFINITE	———
OUTPUT VOLTAGE	——— LIMITED BY SUPPLIES ———		
OUTPUT CURRENT	——— LIMITED BY SUPPLIES ———		
OUTPUT IMPEDANCE	INFINITE		0
OPERATING CURRENT	ADJUSTABLE		ADJUSTABLE

nally developed and applied to the current mirror Q1 and Q2 to bias the differential pair of transistors Q3 and Q4. The differential output-signal currents of Q3 and Q4 are amplified by the beta of the differential p-n-p transistor pair Q7 and Q8. The current mirror Q10 and Q11 then transforms the double-ended output of the p-n-p transistor network Q5 through Q9 into a single-ended output. The entire circuit functions in a class A mode. The amplifier bias current (ABC) level establishes bias for all transistors in the amplifier.

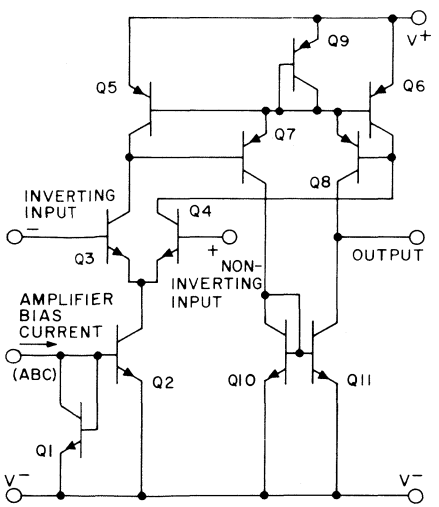


Fig. 202 — Basic OTA circuit.

Ideally, there is no need for a signal ground because the input signal is differential and the output signal is a current. The input and output terminals may operate at most ac and dc potentials within the range of the supply voltages.

RCA-CA3060 OTA CIRCUIT CONFIGURATION

The lateral p-n-p transistors Q7 and Q8 used in the differential output stage of the basic OTA circuit shown in Fig. 202 inherently exhibit a low output impedance. As a result, these transistors tend to degrade the supply rejection ratio and the output impedance of the over-all circuit. Operation of these transistors in cascode stages, as shown in Fig. 203, results in a substantial improvement of these factors. Transistors Q13 and Q14 then perform the driving functions previously provided by transistors Q7 and Q8. Because transistors Q13 and Q14 are operated in a common-base configuration, the transistor output impedance is improved by a factor equal to the beta of the p-n-p transistors. A similar increase in circuit supply-rejection ratio and output impedance is also obtained. Transistors Q15, Q16, and Q17 provide a bias potential for the bases of transistors Q13 and Q14; transistor Q12 provides the current that establishes the bias potential.

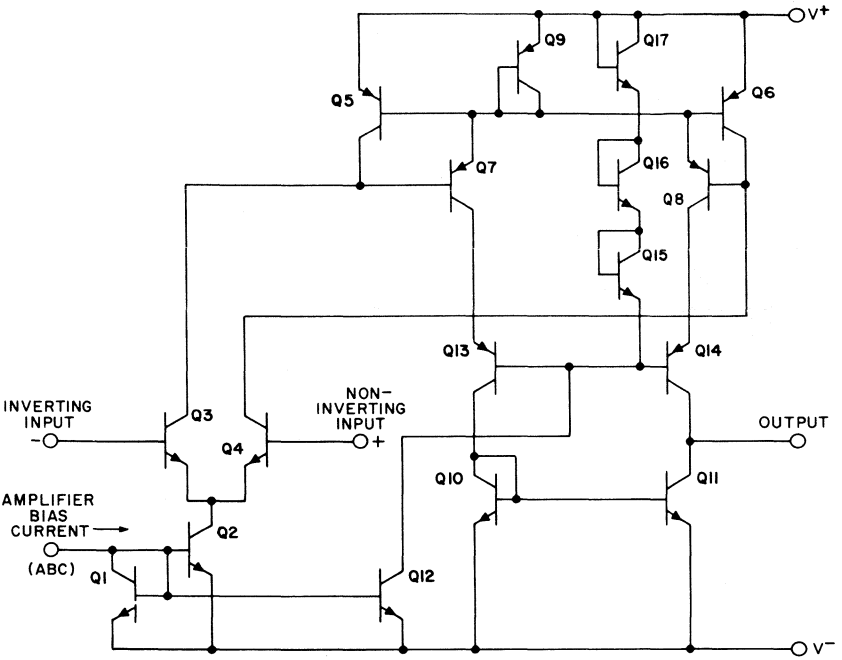


Fig. 203 — Circuit configuration for operational transconductance amplifiers in the CA3060 array.

The circuit configuration shown in Fig. 203 is used for the operational transconductance amplifiers included in the RCA-CA3060 integrated-circuit array.

CHARACTERISTICS AND APPLICATIONS OF THE RCA-CA3060 OTA ARRAY

Fig. 204 shows the over-all functional diagram for the RCA-CA3060 array of three identical independent operational transconductance amplifiers. This integrated-circuit array is supplied in a hermetically sealed, 16-terminal, dual-in-line package, and can be operated over the temperature range from −55°C to +125°C. In addition to the three OTA circuits, the CA3060 array includes a zener diode that regulates the ABC level and a p-n-p current mirror that permits regulation at lower supply voltage than the minimum level allowed by a simple zener-diode circuit. Fig. 205 shows the schematic diagram for the regulator circuit.

Operating Requirements and Characteristics

The three identical OTA circuits in the CA3060 array can be independently biased to achieve a wide range of characteristics for specific applications. The electrical characteristics of each amplifier are a function of the amplifier bias current I_{ABC}. This feature offers the system designer maximum flexibility with regard to output-current capability,

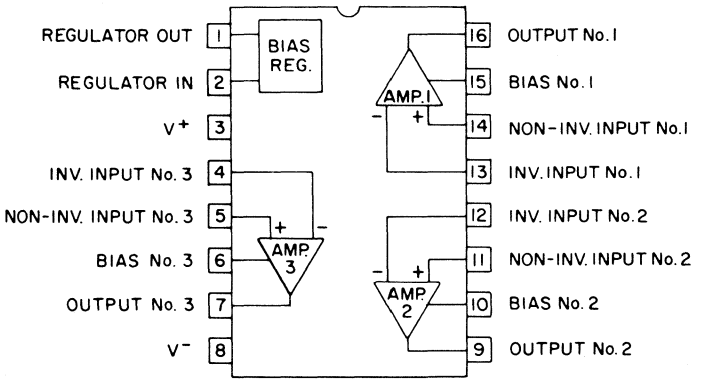


Fig. 204 — Functional block diagram of CA3060 OTA array.

power consumption, slew rate, input resistance, input bias current, and input offset current. The OTA circuits in the CA3060 are designed to operate primarily from symmetrical dual dc supply voltages of ±2 volts to ±6 volts, although single-supply operation is also feasible.

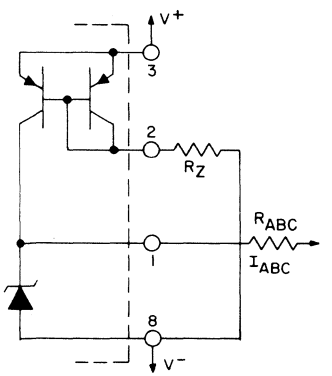


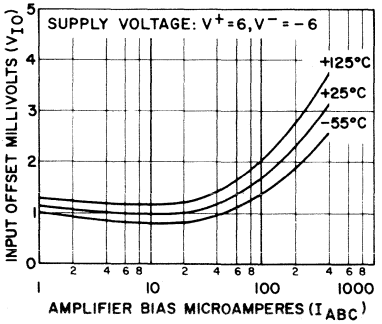
Fig. 205 — Voltage-regulator circuit in the CA3060 OTA array.

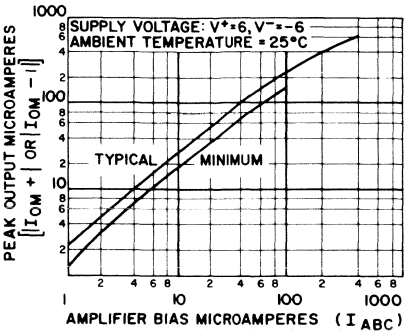
Amplifier Bias Current—The amplifier bias current I_{ABC} is normally provided from a resistive feed, and the current tends to vary as the voltage across the resistor changes. The built-in regulator circuit of the CA3060 regulates the bias current to suppress this variable.

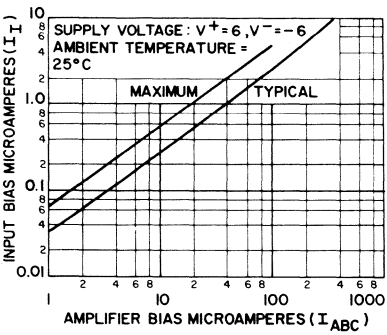
The curves in Figs. 206 through 209 show the performance of a CA3060 OTA circuit as a function of the amplifier bias current I_{ABC}. It is apparent from these curves that the user may select the optimum circuit conditions for a specific application by variation of the bias-current level for each amplifier. If low power consumption, low bias and offset current, or high input impedance are primary design requirements, then low bias-current levels may be selected. Conversely, if the capability to operate into a moderate load impedance is the primary consideration, then higher levels of bias current may be used.

Determination of Bias Conditions—Determination of the bias conditions for an OTA circuit is best illustrated by use of a design example. Fig. 210 shows a 20-dB inverting amplifier that has the following requirements:

Closed-loop voltage
gain (A_{CL}) ..... 10 (or 20 dB)
Equivalent input offset voltage .... as close to zero as possible







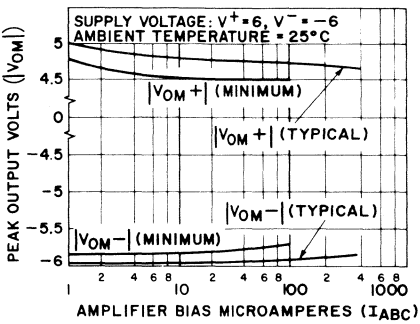
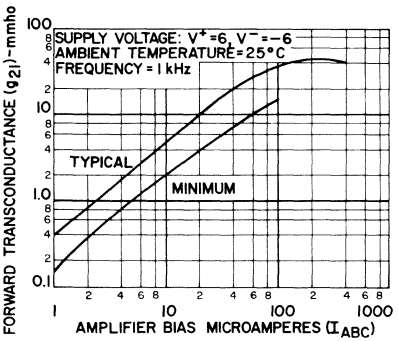


Fig. 206 — (a) Input offset voltage and (b) input bias current as a function of amplifier bias current.

Fig. 207 — (a) Peak output current and (b) peak output voltage as a function of amplifier bias current.



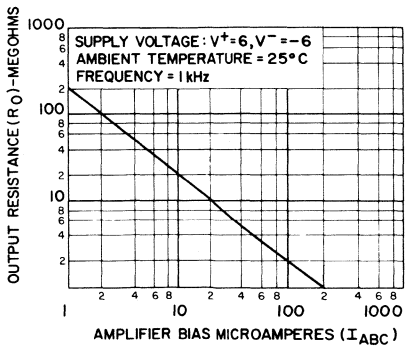


Fig. 208 — Forward transconductance as a function of amplifier bias current.

Fig. 209 — Output resistance as a function of amplifier bias current.

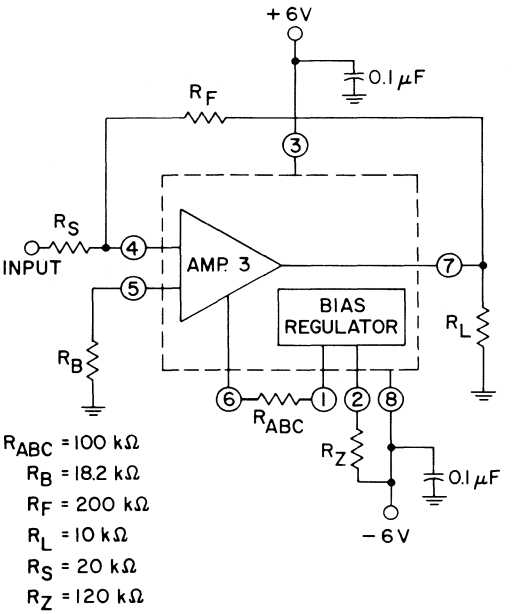


Fig. 210 — Typical 20-dB inverting amplifier circuit using the CA3060.

Current drain ..... not critical
Supply voltages
(V^+ and V^-) .... +6 V and −6 V
Maximum input voltage
(V_{IM}) ..... 100 mV P-P
Input resistance (R_S) ..... 20 kΩ
Load resistance (R_L) ..... 10 kΩ

The following analysis is performed for operation at an ambient temperature at 25°C; only approximate operational-amplifier equations are used to simplify calculations.

Because current drain in this example is not critical, the zener regulator of the CA3060 can be used to provide bias for the amplifiers. Use of the regulator reduces the sensitivity of the input-offset voltage to supply-voltage variations. This use of the regulator is particularly important when unregulated power supplies are employed because the amplifier parameters vary in accordance with amplifier bias current.

The equivalent offset voltage, measured at the input terminal, is a function of the input offset current plus the input offset voltage, and is expressed as $V_{(equiv\ offset)} = V_{IO} + R_S I_{IO}$. For optimum performance, the equivalent offset voltage should have the lowest value possible. Achievement of a minimum equivalent offset voltage requires that the amplifier bias current (I_{ABC}) be held to a low value, because I_{IO} and I_I are also functions of I_{ABC}. Therefore, the values of I_{ABC} should be no larger than that necessary to provide sufficient open-loop gain and sufficient output swing for the specific application.

The following procedure is used to determine the bias conditions for the 20-dB inverting amplifier:

1. *Calculation of required value of transconductance:* The open-loop gain A_{OL} must be at least 10 times

the closed-loop gain A_{CL} (i.e., $A_{OL} = 10 \times 10 = 100$). This value is used in the calculation of the required value of the forward transconductance g_{21}, as follows:

$$\begin{aligned} g_{21} &= A_{OL}/R_L \\ &= 100/(10 \text{ kilohms}) \\ &= 10 \text{ millimhos} \end{aligned}$$

2. *Selection of the amplifier bias current:* The amplifier bias current I_{ABC} is selected from the minimum-value curve of transconductance in Fig. 208 to assure that the amplifier will provide sufficient gain. For the required transconductance of 100 millimhos, this curve provides an I_{ABC} value of 60 microamperes. For this value of amplifier bias current, Fig. 207(a) indicates that the peak output current, I_{OM+} or I_{OM-}, is 100 microamperes.

3. *Determination of output-swing capabilities:* For a 20-dB amplifier, the output-voltage swing V_{OM} is 10 times the input voltage, or 1 volt peak-to-peak for the circuit used in this example. The peak-to-peak load-current swing I_L may be calculated as follows:

$$\begin{aligned} I_L &= V_{OM}/R_L \\ &= (1 \text{ volt p-p})/(10 \text{ kilohms}) \\ &= 100 \text{ microamperes} \end{aligned}$$

4. *Calculation of feedback loading:* The value of the feedback resistor R_F can be calculated by use of the classical design equation for the closed-loop gain A_{CL} of an inverting operational amplifier, as follows:

$$A_{CL} = E_O/E_I \approx R_F/R_S$$

Therefore,

$$\begin{aligned} R_F &\approx (E_O/E_I)R_S \\ &\approx 10 \times 20 \text{ kilohms} \\ &\approx 200 \text{ kilohms} \end{aligned}$$

The current through the feedback resistor, I_F, is then determined from the following calculation:

$$\begin{aligned} I_F &= E_O/R_F \\ &= (1 \text{ volt p-p})/200 \text{ kilohms} \\ &= 5 \text{ microamperes} \end{aligned}$$

5. *Determination of total load current:* The total peak load current is the sum of I_L and I_F, or 105 microamperes. The magnitude of the peak output current, I_{OM+} or I_{OM-}, therefore, is 52.5 microamperes. The required load current is less than the available current shown in step 2. The value of 60 microamperes selected for the amplifier bias current, therefore, is adequate.

6. *Calculation of bias resistances:* After the amplifier bias current I_{ABC} is established, it is possible to design the bias circuit. The zener-diode bias regulator should provide sufficient current to maintain proper regulation. A value of bias-regulator current I_2 that is 1.5 times the amplifier bias current I_{ABC} satisfies this requirement. The value of the bias resistor may be determined by use of Ohm's law, as follows:

$$R_Z = \frac{V^+ + V^- - (0.7 \text{ volt})}{1.5(I_{ABC})}$$

$$= \frac{+6 \text{ volts} + (-6 \text{ volts}) - (0.7 \text{ volt})}{1.5(60 \text{ microamperes})}$$

$$= 125 \text{ kilohms}$$

In a practical circuit, a standard-value 120-kilohm resistor may be used. In the above calculation, the value of 0.7 volt represents the voltage drop across the diode in the bias regulator, which is connected in series with the resistor R_Z and the V^+ and V^- supplies, as shown in Fig. 205.

The value of the resistor R_{ABC}, which determines the amplifier bias current, can be determined in a similar manner. The voltage drop across this resistor is equal to the voltage V_Z at the output (terminal 1) of the

bias regulator minus the voltage V_{ABC} at the bias input (terminal 6) of the 20-dB amplifier. Fig. 211(a) indicates that the bias-regulator voltage V_Z is approximately 6.8 volts for a regulator current I_2 (= 1.5 I_{ABC}) of 90 microamperes. The voltage V_{ABC}, as determined from Fig. 211(b), is approximately 0.64 volt for a current I_{ABC} of 60 microamperes. The resistance R_{ABC} can then be determined from the following calculation:

$$R_{ABC} = \frac{V_Z - V_{ABC}}{I_{ABC}}$$

$$= \frac{(6.8 - 0.64) \text{ volts}}{60 \text{ microamperes}}$$

$$= 104 \text{ kilohms.}$$

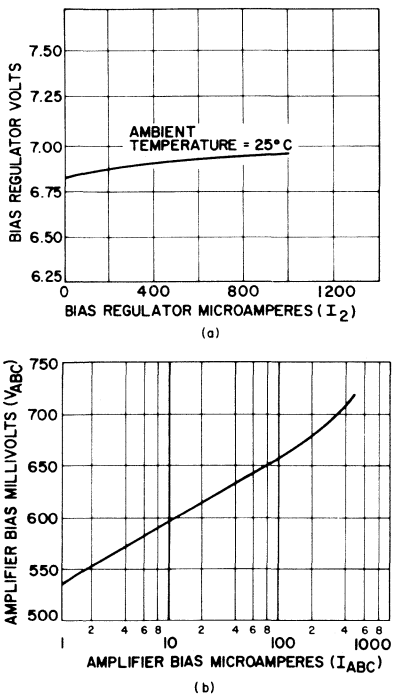


Fig. 211 — (a) Bias regulator voltage as a function of bias-regulator current and (b) amplifier bias voltage as a function of amplifier bias current.

In the actual circuit, a standard-value 100-kilohm resistor may be used.

Speed—If the three OTA's of the CA3060 are arranged in cascade, as shown in Fig. 212(a), the measured output waveforms for two I_{ABC} levels, shown in Fig. 212(b), indicate an open-loop slew rate of approximately 50 volts per microsecond for the higher bias current, and a propagation time of approximately 150 nanoseconds per OTA.

Fig. 213 shows a slew-rate test circuit and the unity-gain slew rate for three bias levels. Values as high as 8 volts per microsecond are obtained at an I_{ABC} level of 100 microamperes.

Low-Frequency Noise and Short-Term Stability—Some indication of the low-frequency noise and short-term stability of the OTA can be obtained by cascading the three OTA's of the CA3060 in a noninverting manner. The I_{ABC} levels are adjusted to produce 180 to 190 dB of open-loop voltage gain with feedback adjusted to produce a 120-dB closed-loop noninverting voltage amplifier. The pen recording of the output in Fig. 214 shows the influence of noise and drift upon the amplified 0.011-Hz 1-microvolt peak-to-peak square wave over a period of 8 minutes. Sufficient capacitance was shunted across the input of the final OTA to reduce the system rise time to 5 seconds.

Capacitance Effects—The CA3060 is designed to operate at such low power levels that high-impedance circuits must be employed. In the design of such circuits, particularly feedback amplifiers, stray circuit capacitance must always be considered because of its adverse effect on frequency response and stability. For example, a 10-kilohm load resistance and an associated stray capacitance

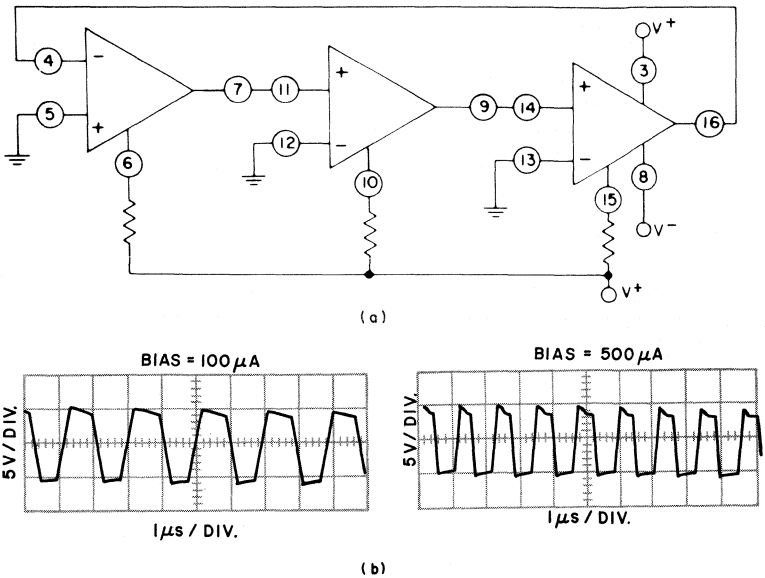
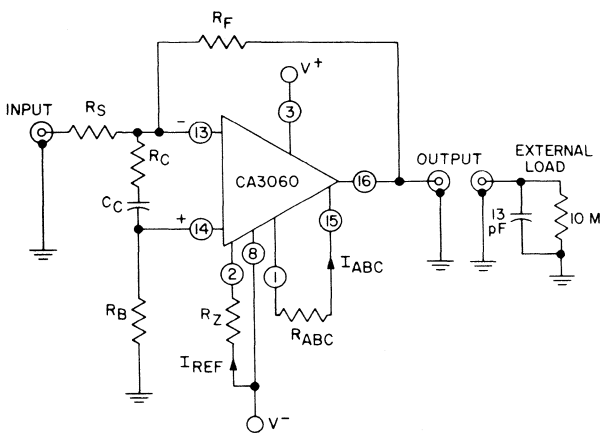


Fig. 212 — Maximum oscillating frequency of the CA3060.



TYPICAL SLEW RATE TEST CIRCUIT PARAMETERS								
I_{ABC}	SLEW RATE	R_Z	R_{ABC}	R_S	R_F	R_B	R_C	C_C
μA	V/μs	ohms						μF
100	8	56k	62k	100k	100k	51k	100	0.02
10	1	56k	620k	1M	1M	510k	1k	0.005
1	0.1	56k	6.2M	10M	10M	5.1M	∞	0

All resistance values in ohms unless otherwise specified.

Fig. 213 — Slew rate test circuit and measurements.

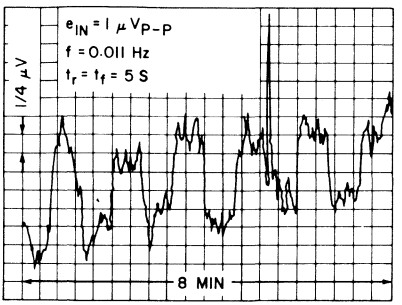


Fig. 214 — Noise and drift of the CA3060.

of 15 picofarads produce a corner in the gain-frequency response at 1 MHz [i.e., $1/(2\pi RC) = 1$ MHz]. Fig. 215 illustrates how a 10-kilohm, 15-picofarad load modifies the OTA frequency characteristic.

Capacitive loading also has an effect on slew rate. Because the peak output current is established by the amplifier bias current, I_{ABC}, the maximum slew rate is limited to the maximum rate at which the capacitance can be charged by the I_{OM}. Therefore, the slew rate SR is given by

$$SR = dV/dt = I_{OM}/C_L$$

where C_L is the total load capacitance including strays. This relationship is shown graphically in Fig. 216.

Phase Compensation—In many applications, phase compensation is not required for the amplifiers of the CA3060. When needed, compensation may easily be accomplished by a simple RC network at the input of the amplifier, as shown in Fig. 215. The values given in Fig. 215 provide stable operation for the critical unity-gain condition, provided the capacitive loading on the output is 13 picofarads or less. Input phase compensation is recommended to maintain the highest possible slew rate.

In applications such as integrators, two OTAs may be cascaded to improve current gain. Compensation is best accomplished in this case with a shunt capacitor at the output of the first amplifier. The high gain following compensation assures a high slew rate.

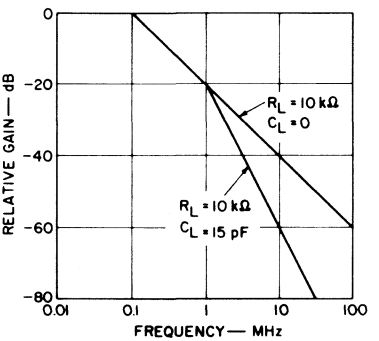


Fig. 215 — Effect of capacitive loading on frequency response.

Applications

The operational transconductance amplifiers in the CA3060 integrated-circuit array allow the circuit designer to select and control the operating level and conditions of the circuit merely by adjustment of the input to one additional terminal. The characteristics of the OTA circuits are directly dependent upon the level of the amplifier bias current I_{ABC}. For an amplifier current of only 1 microampere, the transconductance is typically 0.38 millimho, as shown in Fig. 208. If the amplifier bias current is increased to 100 microamperes, the transconductance rises to 35 millimhos. In view of the fact that the system gain of an OTA circuit is equal to the product of the transconductance and the external load resistance, complete control of the open-loop characteristic can be achieved merely by variation of the

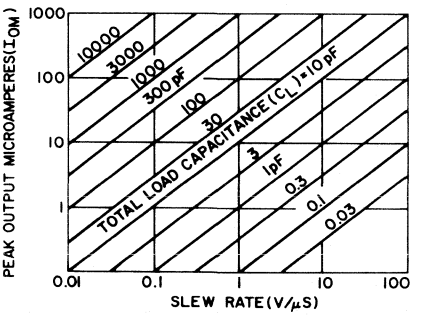
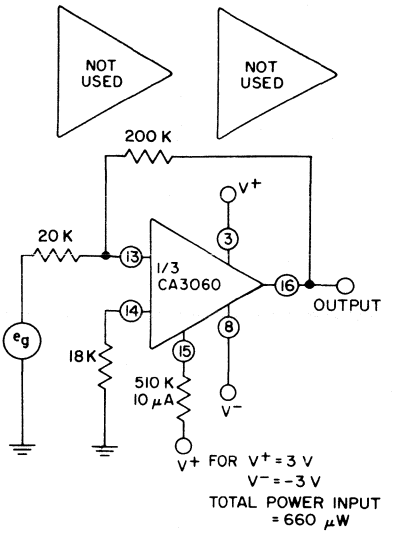


Fig. 216 — Effect of load capacitance on slew rate.

amplifier bias current. In addition, the total current to the amplifier is also directly related to the amplifier bias current so that direct control is provided over the total power input to the amplifier. These features make possible the exceptional versatility that permits use of the OTA circuit in highly diverse applications that have widely differing requirements.

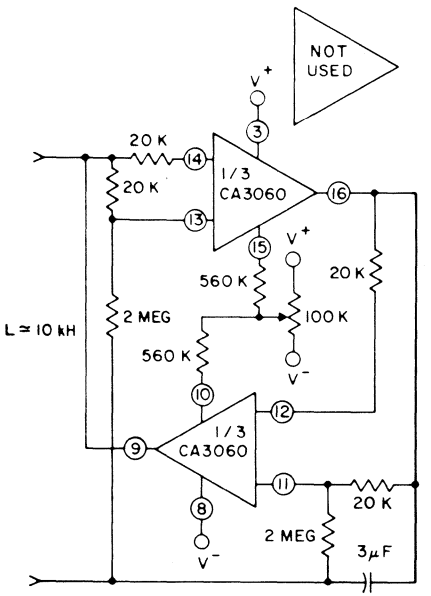
Low-Dissipation Operational Amplifier—The power dissipation of an operational transconductance amplifier is determined by I_{ABC}; it is generally below 10 milliwatts, and often below 1 milliwatt. The typical 20-dB inverting amplifier shown in Fig. 217 is operated at an ABC level of 10 microamperes. The open-loop voltage gain of the amplifier is then equal to g_m times R_L, or $4.5 \times 10^{-3} \times 0.2 \times 10^6$, or 0.9×10^3 (the feedback network and many other loads reflect directly in the open-loop voltage gain). The standard design equations for operational amplifiers may be used to calculate the amplifier closed-loop characteristics, with the load resistance on the amplifier being substituted for the output resistance in the operational-amplifier equations. The calculated closed-loop gain is 20 dB.



All resistance values in ohms unless otherwise specified.

Fig. 217 — Typical low-dissipation amplifier.

Gyrator Applications—The OTA is especially suitable for use in gyrators because the high output impedance satisfies one of the basic requirements for this application. Inductances in excess of 10 kilohenries have been realized by use of only two OTA's. Fig. 218 shows a gyrator circuit that produces such a high synthetic inductance with only a 3-microfarad capacitor. There is no reference to ground in this circuit; the "inductor" may float within the common-mode restraints of the OTA. Effectively, the inductor is isolated from the supplies by the high-impedance input and output of the amplifier. An attenuation network around the input of both amplifiers extends the differential operating range of each OTA about 100 times. In addition, this network reduces the transconductance by the same factor and thus further increases the gyration resistance. The provision for adjustable bias current



All resistance values in ohms unless otherwise specified.

Fig. 218 — Gyrator circuit using the CA3060 OTA array.

to the OTA permits direct control of transconductance and, therefore, varies gyration resistance inversely. Because phase shift restricts the Q of the inductor, operation at frequencies above the audio range is impaired.

Amplifier with Automatic Gain Control—The variable-transconductance characteristic of the OTA is useful in an agc amplifier. When the OTA operates in the open-loop condition, the transconductance, and thus the amplifier gain, can be varied directly by adjustment of the ABC level. Therefore, an excellent agc amplifier is obtained by rectifying and storing the amplifier output and applying this signal to the bias terminal. Fig. 219 shows a functional diagram of such a system. Low-frequency feedback is provided around the gain-controlled stage to balance the amplifier. As the input signal increases, the amplifier bias current decreases and reduces the transconductance and therefore the system gain.

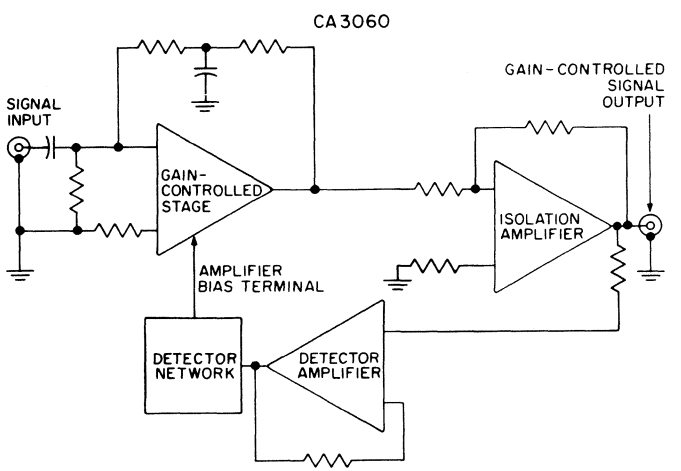
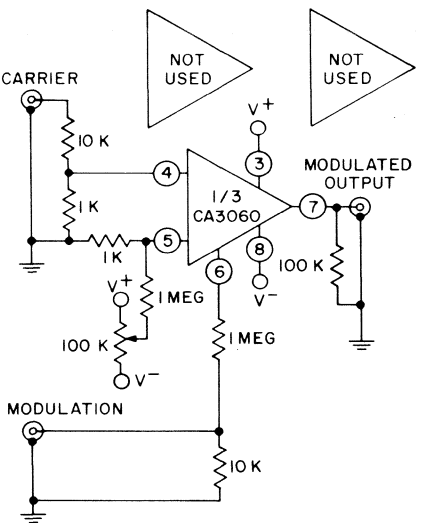


Fig. 219 — Gain-controlled amplifier.

Amplitude Modulation—The gain-control characteristic of the OTA can also be used to provide modulation from dc to the upper cutoff frequency of the system with a single OTA. In this application, a carrier signal is applied to the differential input and a modulating signal current is added to the dc level of I_{ABC}. Fig. 220 shows a modulator



All resistance values in ohms unless otherwise specified.

Fig. 220 — Modulator circuit using an OTA.

with carrier and modulating frequency capability greater than 20 kHz. Fig. 221(a) shows the waveforms obtained when the modulator operates at a carrier frequency of 10 kHz and a modulation frequency of 500 Hz. As a modulator, the circuit should also be able to handle a 500-Hz carrier and a 10-kHz modulating signal; waveforms obtained under these conditions are shown in Fig. 221(b). The function performed by an AM modulator can be expressed as follows:

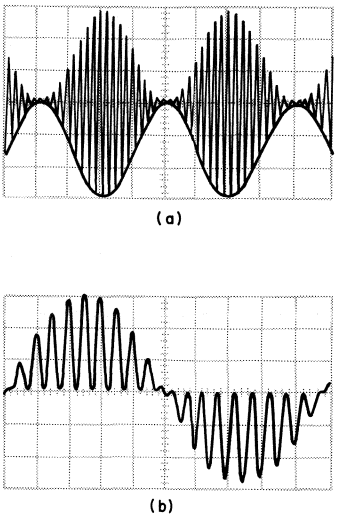


Fig. 221 — Output waveforms for modulator circuit shown in Fig. 220: (a) with a modulating signal (lower trace) of 500 Hz and a carrier of 10 kHz; (b) with modulating signal of 10 kHz and a carrier of 500 Hz.

$$e_{OUT} = KX(1 + Y)$$

Four-Quadrant Multiplier—The CA3060 is also useful as a four-quadrant multiplier. The basic configuration for such a multiplier that uses Amplifier Nos. 1, 2, and 3 is shown in Fig. 222. The multiplier consists of a single CA3060 and exhibits no level shift between input and output. In this circuit, amplifier No. 1 is connected as an inverting amplifier for the X-input signal. The output current of amplifier No. 1 is calculated as follows:

$$I_{O(1)} = [-V_X][g_{21(1)}]$$

Amplifier No. 2 is a noninverting amplifier so that the output current may be expressed by the following equation:

$$I_{O(2)} = [+V_X][g_{21(2)}]$$

Because the amplifier output impedances are high, the load current

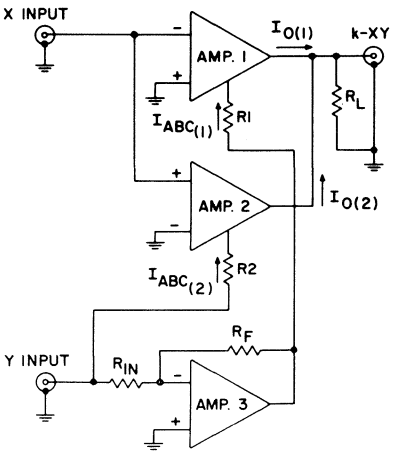


Fig. 222 — Basic configuration for a four-quadrant multiplier using the CA3060.

is the sum of the two output currents, for an output voltage defined as follows:

$$V_O = V_X R_L[g_{21(2)} - g_{21(1)}]$$

The transconductance is approximately proportional to the amplifier bias current; therefore, by varying the bias current, the transconductance g_{21} is also controlled. The bias of amplifier No. 2 is proportional to the Y-input signal and is expressed as follows:

$$I_{ABC(2)} \approx \frac{(V^-) + V_Y}{R1}$$

The transconductance of this amplifier, therefore, may be approximated by the following expression:

$$g_{21(2)} \approx k[(V^-) + V_Y]$$

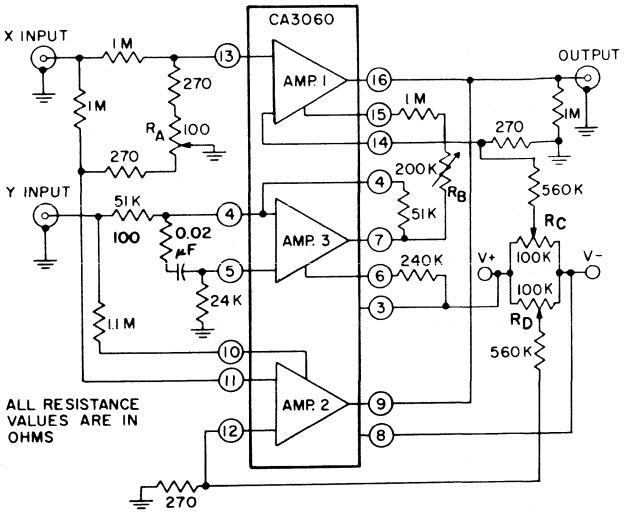
Bias for amplifier No. 1 is derived from the output of amplifier No. 3, which is connected as a unity-gain inverting amplifier. $I_{ABC(1)}$ therefore varies inversely with V_Y. The transconductance for this amplifier is given by

$$g_{21(1)} \approx k[(V^-) - V_Y]$$

If the relationships for $g_{21(1)}$ and $g_{21(2)}$ are substituted in the equation for the output voltage, the following result is obtained.

$$\begin{aligned} V_O &\approx V_X k R_L\{[(V^-) + V_Y] \\ &\quad - [(V^-) - V_Y]\} \\ &\approx 2kR_L V_X V_Y \end{aligned}$$

Fig. 223 shows the actual four-quadrant multiplier circuit, together with all the adjustments associated with differential input and an adjustment for equalizing the gains of amplifiers No. 1 and No. 2. Adjustment of the circuit is relatively simple. With both the X and Y voltages at zero, terminal 10 is connected to terminal 8. This procedure disables amplifier No. 2 and permits adjustment of the offset voltage of amplifier No. 1 to zero by means of the 100-kilohm potentiometer R_C. The short between terminals 10 and 8 is then removed, and terminal 15 is connected to terminal 8. This step disables amplifier No. 1 and permits amplifier No. 2 to be zeroed with



All resistance values in ohms unless otherwise specified.

Fig. 223 — Typical CA3060 four-quadrant multiplier circuit.

the other 100-kilohm potentiometer R_D. With ac signals applied to both the X and Y inputs, R_A and R_B are adjusted for symmetrical output signals.

Fig. 224 shows the output waveform with the multiplier adjusted. The voltage waveform in Fig. 224(a) shows suppressed carrier modulation of a 1-kHz carrier with a triangular wave. Figs. 224(b) and 224(c), respectively, show the squaring of a triangular wave and a sine wave. In both cases, the outputs are always positive and return to zero after each cycle.

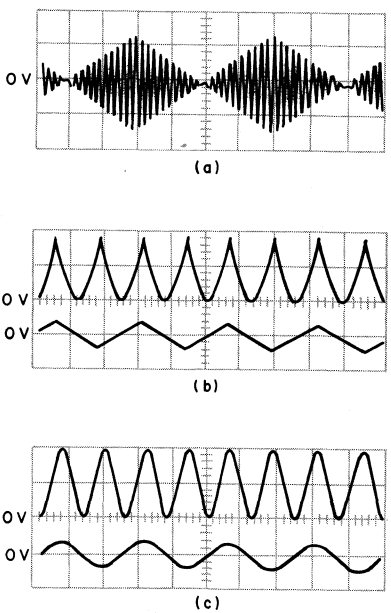
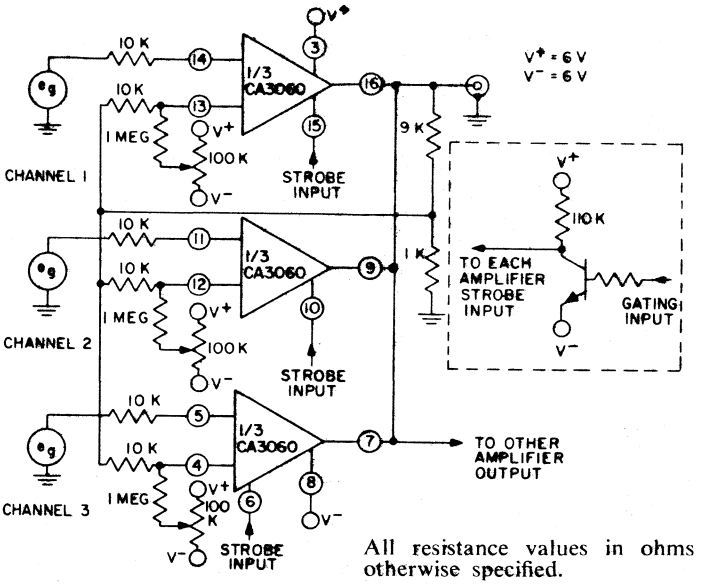


Fig. 224 — Voltage waveforms for the four-quadrant multiplier circuit shown in Fig. 223.

Multiplexing—Fig. 225 shows a three-channel gated amplifier in which each amplifier or channel may be sequentially activated to display its input with gain of about 20 dB. Because the input impedance is extremely high when the OTA is biased "off," a common feedback network may be used. Position control of each channel is accomplished with little



All resistance values in ohms unless otherwise specified.

Fig. 225 — Three-channel gated amplifier.

interaction by application of offset adjustment to the inverting input of each amplifier.

Activation of each channel is accomplished by cutting off normally saturated transistors that shunt the amplifier-bias-current terminals. Drive to the transistor switches may be applied from a ring-counter-type circuit that is either triggered by an external source or "free run" to chop the signals.

A Bistable Circuit—Fig. 226 shows an OTA circuit that is stable in either of two states. In the lower state, the total circuit dissipation is zero. A positive pulse applied to the trigger terminal "sets" the circuit to the ON state. A negative pulse applied to this terminal will reset the circuit. Alternatively, the circuit may be reset by application of a positive pulse to the inverting (RESET) terminal.

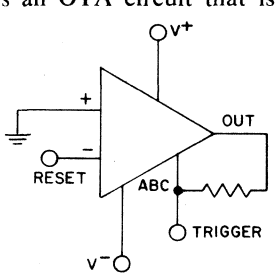


Fig. 226 — Bistable OTA circuit.

A One-Shot Circuit with Nanowatt Dissipation—The OTA circuit shown in Fig. 227 develops a single pulse whenever it is triggered (at a low duty factor only). Circuit current is drawn only during the pulse time. Signal output may be extracted from V+, V−, or the "OUT" terminal. If the V+ or V− lead is employed for pulse sampling, care must be used to observe the OTA common-mode rejection range. If the V− lead is used, other circuits of the integrated circuit may be influenced when the V− terminal and

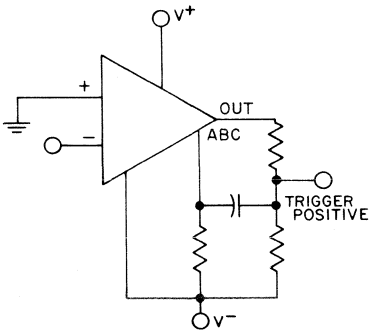


Fig. 227 — One-shot circuit.

the substrate terminal are common (as is the case for the CA3060). Loading of the output must be light. This one-shot circuit can be biased to ignore trigger pulses if the inverting input is made more positive than the noninverting input.

A Low-Dissipation Astable Circuit—Fig. 228 shows an astable OTA circuit designed for low-duty operation. Power dissipation in the nanowatt level can be achieved with this circuit. Operation is similar to that of the circuits shown in Figs. 226 and 227. The circuit of Fig. 228 may be gated "off" by the inverting input. Pulse width and duty cycle are relatively independent of V^+.

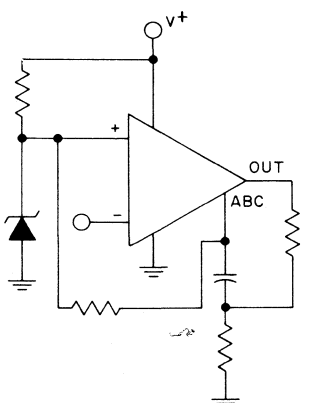


Fig. 228 — Astable circuit.

Sample-Hold-Read Application—Fig. 229 shows a functional circuit in which the storage capacitor is essentially isolated from circuit loading during the "hold" period. Because both the charging OTA and the read OTA are biased off during "hold", they contribute only leakage currents in this period. Capacitor C1 is the storage capacitor. C2 is a small capacitor used to assure stable operation.

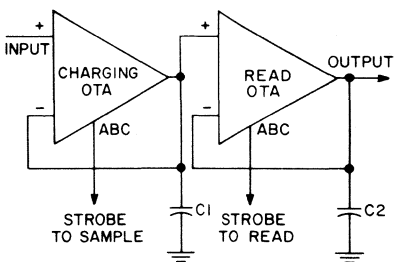


Fig. 229 — Sample-hold-read circuit.

Sample-Hold-Compare Application—The OTA circuit shown in Fig. 230 samples a voltage, holds it, and compares it to a reference voltage E. As in the circuit of Fig. 229, loading of C1 is negligible during the "hold" period.

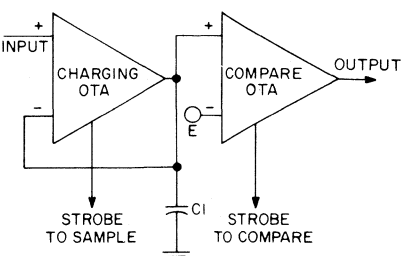


Fig. 230 — Sample-hold-compare circuit.

Multipurpose Amplifiers

The RCA line of linear integrated circuits encompasses a group of multistage amplifier circuits that can be adapted for use in a wide variety of applications as wide- or narrow-band amplifiers, video amplifiers, limiters, gain-controlled linear amplifiers, and other similar types of circuits. This group of highly versatile circuits includes three low-power video and wide-band amplifiers (CA3021, CA3022, and CA3023), an extremely broadband amplifier (CA3040) for both industrial and commercial applications, and two wide-band power amplifiers (CA3020 and CA3020A).

LOW-POWER VIDEO AND WIDE-BAND AMPLIFIERS

The RCA-CA3021, CA3022, and CA3023 integrated circuits are multipurpose high-gain amplifiers designed for use in video and AM or FM if stages in single-power-supply systems. These circuits are supplied in a 12-terminal TO-5-style package and are usable throughout the temperature range from −55°C to 125°C. They have the same circuit configuration and the same mid-band open-loop gain. However, different resistor values are used in the three circuits to provide different values of power dissipation and open-loop bandwidth. Typical power dissipation with a 6-volt supply is 3 milliwatts for the CA3021, 12 milliwatts for the CA3022, and 36 milliwatts for the CA3023. Wider bandwidths can be achieved with the CA3023, intermediate bandwidths with the CA3022, and narrower bandwidths with the CA3021.

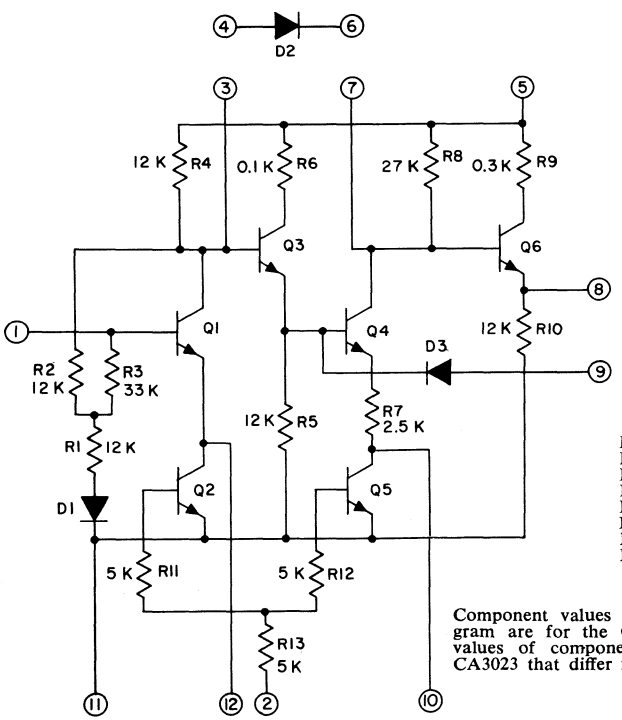
The major feature of these circuits is a flexibility that permits their use in the following applications: video amplifiers operating at frequencies through 30 MHz, AM and FM if amplifiers, and buffer amplifiers in which an isolation capability greater than 60 dB at 1 MHz is desired. The areas of circuit flexibility are as follows:

- Operation with dc supplies of 4.5 to 12 volts;
- Automatic-gain-control capability (60-dB agc range with large input-signal-handling capability);
- Limiting capability (by connection of diodes provided on the chip);
- Gain adjustment (by addition of external feedback resistor or network to obtain desired operating gain and bandwidth).

Circuit Description

The circuit diagram for the CA3021, CA3022, and CA3023 is shown in Fig. 231. Amplifier gain is obtained by use of transistors Q1, Q3, Q4, and Q6, which are connected as two dc-coupled common-emitter/common-collector amplifiers having a voltage gain of approximately 60 dB. The common-collector configuration provides the necessary impedance transformation (high-impedance input and low-impedance output) for wide bandwidth. The output transistor Q6 provides the low output impedance desired for iterative operation. The circuit must be capacitively coupled, and should have a low-impedance source.

Fig. 232 shows typical connections for the CA3021, CA3022, and CA3023 for wide-band and band-pass applications with and without agc, and for limiter applications. An external feedback resistor R_f or a tuned circuit can be added between terminals 3 and 7 for desired bandwidth and gain performance. Linear operating conditions are maintained by the bias applied between the collector and the base of Q1 by the resistor-diode network R2, R3, R1, and D1. Because the collector of Q1 is held at a fixed potential that is relatively independent of supply, device characteristics, and temperature, dc coupling to the remainder of the circuit can be used.



	CA3022	CA3023
R1	3.9 K	1.5 K
R2	3.8 K	1.5 K
R3	15 K	5.6 K
R4	3.4 K	1.8 K
R5	3.9 K	1 K
R7	0.75 K	0.15 K
R8	7.5 K	3 K
R10	3.9 K	2.2 K

Component values shown on the circuit diagram are for the CA3021. The chart shows values of components for the CA3022 and CA3023 that differ from those of the CA3021.

All resistance values in ohms unless otherwise specified.

Fig. 231 — CA3021, CA3022, or CA3023 integrated circuit.

For applications in which gain control is desired, terminals 10 and 12 are left floating and agc is applied to terminal 2, as shown in Fig. 232(b). For maximum gain, terminal 2 is operated at a positive voltage not larger than the supply voltage applied to terminal 5. In the positive-voltage condition, transistors Q2 and Q5 are saturated, and the impedance in the emitters of Q1 and Q4 is low. When the gain-control voltage becomes negative, Q2 and Q5 come out of saturation and provide high degenerative emitter resistance which reduces the gain. Because most of the increasing signals appear across the increasing degenerative resistance, the active gain transistors Q1, Q3, Q4, and Q6 handle only a small part of the large signal. As a result, signal-handling capability increases with increasing agc. Further increases of gain-control voltage reduce the current in Q1 and Q4 and thus provide the additional gain control needed to achieve maximum agc range.

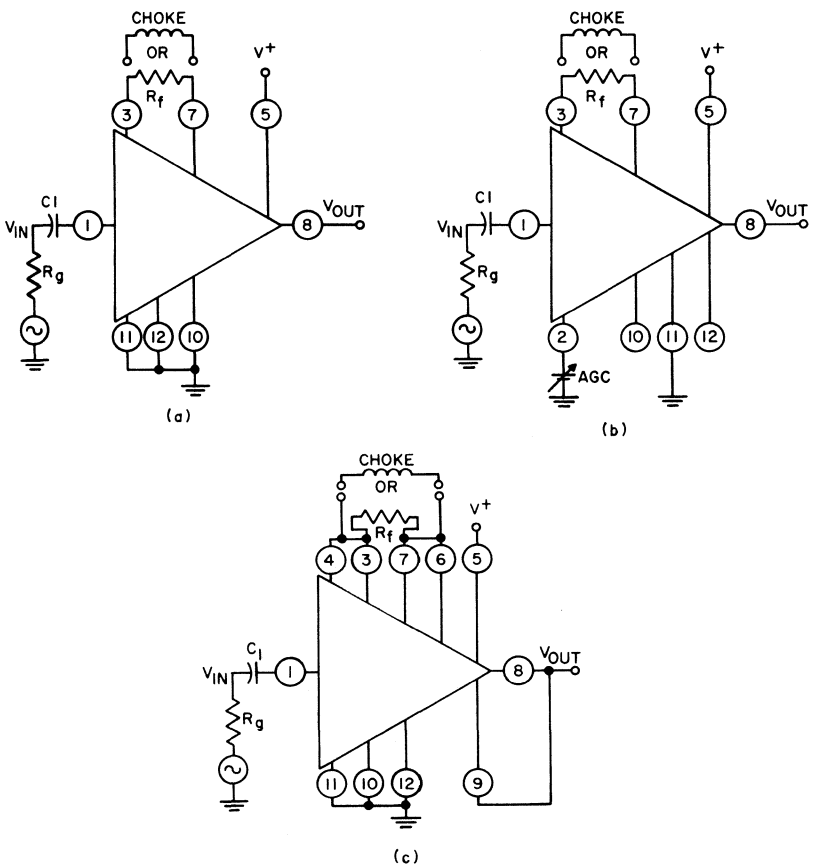


Fig. 232 — Typical connections for the CA3021, CA3022, or CA3023 for (a) wide-band and band-pass applications, (b) wide-band and band-pass applications that require agc, and (c) limiter applications.

In limiting applications, diodes D2 and D3 are connected in the feedback loops, as shown in Fig. 232(c) (terminals 4 to 3, 6 to 7, and 8 to 9). The diodes provide clamping for sufficient input-signal swing; limiting can be achieved with input-signal swings up to 2.5 volts rms.

Biasing Requirements

The most positive voltage to be applied to the CA3021, CA3022, and CA3023 integrated circuits is connected to terminal 5. The most negative voltage is connected to the substrate through terminal 11.

The circuits can be used with single power supplies of 4.5 to 12 volts. The bias technique used for transistor Q1, and thus for the remainder of the circuit, makes the collector operating voltage of Q1 and Q4 relatively independent of the supply. Consequently, the current in the circuit increases almost linearly as a function of supply voltage. Fig. 233 shows typical power dissipation for the three circuits as a function of supply voltage. Because there is little change in the collector voltage of Q4, there is little change in output operating point as a function of supply voltage.

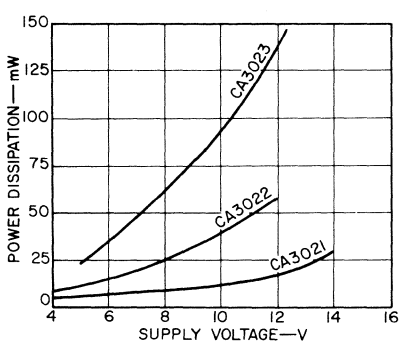


Fig. 233 — Power dissipation as a function of supply voltage for the CA3021, CA3022, and CA3023.

DC Stability with Temperature— The output operating points of the CA3021, CA3022, and CA3023 are shown in Fig. 234 as a function of temperature and feedback resistance. As a result of the resistor values used

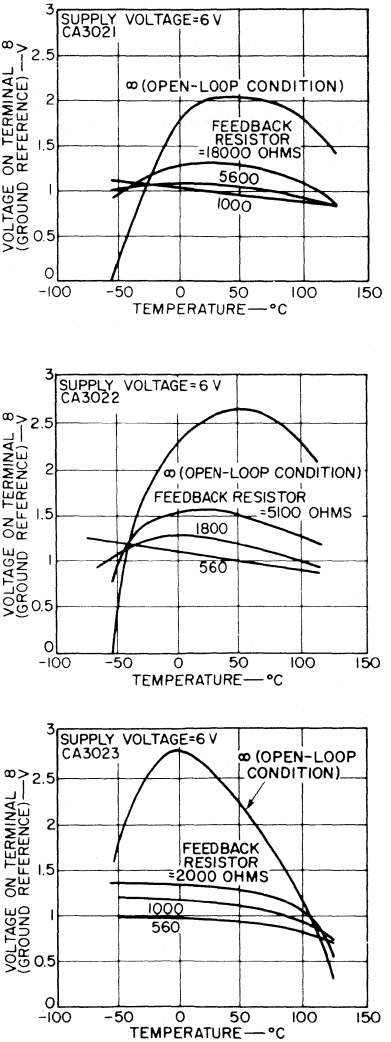


Fig. 234 — Output operating point of the CA3021, CA3022, and CA3023 as a function of temperature for various values of feedback resistance.

in each circuit, the output operating point is compensated in the temperature range between −20°C and 75°C when the circuit is operated under open-loop conditions (terminals 3 and 7 floating). Insertion of a feedback resistor between terminals 3 and 7 is recommended to minimize degradation in performance at temperatures outside this range. The maximum value of the feedback resistor R_f recommended for optimum performance of each circuit is as follows:

Circuit	*Feedback Resistance, R_f — ohms*
CA3021	18000
CA3022	5100
CA3023	3000

Use of a feedback resistor of the maximum value provides equal ac and dc feedback, but reduces the usable gain of the circuit to approximately 40 dB. When equal ac and dc feedback is not desired, as in the case of band-pass or tuned responses, a choke or tuned circuit can be included between the feedback terminals 3 and 7 to provide dc temperature stability and permit gains of 50 to 55 dB.

As a general rule, feedback should be included in all applications in which operation over an extended temperature range is required.

DC Considerations for Gain Control—When the agc transistors Q2 and Q5 are included in the circuit, the output operating point can be held constant only by addition of feedback. Variation of operating point is caused by the added collector-to-emitter voltage of Q2 and Q5 in saturation in the emitters of Q1 and Q4. The effect is more pronounced in the higher-current circuits CA3022 and CA3023. As discussed previously, full dc feedback can be used to stabilize the operating point; ac feedback can be removed by the use of tuned circuits. The maximum recommended values of R_f provide satisfactory stability when the circuit is connected for agc.

DC Considerations for Limiting—In limiter applications, diodes D2 and D3 are included in the feedback loops in the circuit [external connections are made as shown in Fig. 232(c)]. Under open-loop conditions, the dc operating point may be such that D2 and D3 (usually D3) are turned on. The gain is then reduced and the amplifier will not operate linearly at low levels. The values of R_f recommended previously also assure correct operation for limiting amplifiers.

Gain-Frequency Characteristics

Open-loop frequency responses for the CA3021, CA3022, and CA3023 are given in Fig. 235. The curves also show the response characteristics to the 3-dB point for various values of feedback resistance. Values of feedback resistance larger than those recommended for operating-point temperature stability are included to indicate gain performance at resonance when tuned circuits or chokes are used in the feedback loop. For these measurements, the circuits were operated with a 50-ohm source and a high-impedance load.

Fig. 236 shows the variation in gain with temperature for the three circuits. Each circuit was operated with sufficient feedback to provide a closed-loop gain of approximately 40 dB. The gain variation is practically independent of feedback, and is slightly greater for the CA3023 than for the other two circuits. Fig. 237 shows typical upper-3-dB frequency shifts with temperature for the three circuits for a gain of approximately 40 dB.

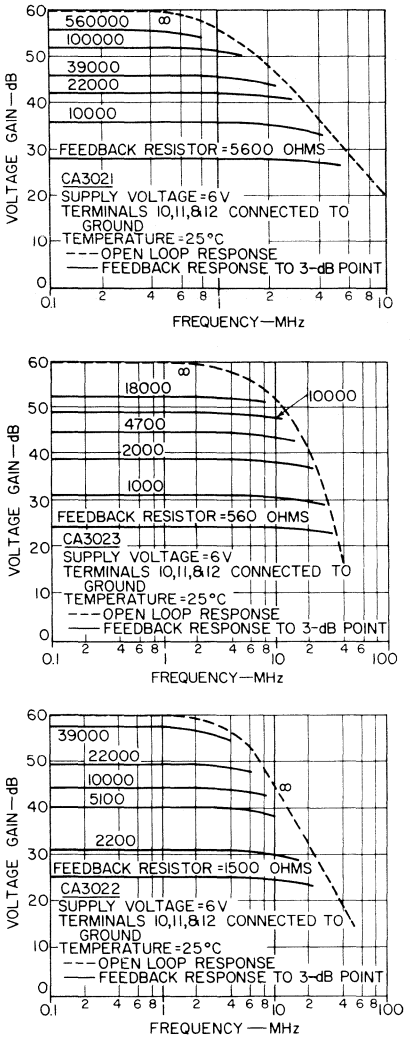


Fig. 235 — Frequency-response characteristics of the CA3021, CA3022, and CA3023.

In buffer-amplifier applications, reverse feedback or isolation capability is required. Table XXVI shows the isolation performance of the CA3021, CA3022, and CA3023 at three frequency levels with the input terminated in 50 ohms.

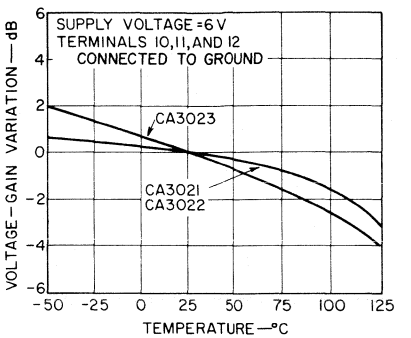


Fig. 236 — Voltage-gain variation with temperature for the CA3021, CA3022, and CA3023 (feedback adjusted to provide gain of approximately 40 dB at 25°C).

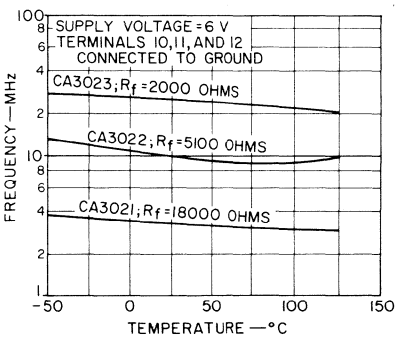


Fig. 237 — Upper 3-dB frequency shift with temperature for the CA3021, CA3022, and CA3023.

Power-Output Capability

The maximum power-output capability of the common-collector output transistor Q6 in Fig. 231 occurs for a load-resistance value higher than the output impedance. For determination of optimum load-resistor values, each circuit is operated from a 6-volt supply at a gain of approximately 40 dB with a variable resistor capacitively coupled to terminal 8. The variation of maximum linear signal output as a function of load

Table XXVI — *Isolation Performance of the Wide-Band Amplifiers*

Circuit	Feedback Resistor R_f (ohms)	Voltage Inected at Output (volts rms)	Resultant Feedthrough Input Voltage Below the Applied Output Voltage (dB) f = 1 MHz	f = 10 MHz	f = 50 MHz
CA3021	18000	2	66	66	54
CA3022	5000	2	66	66	54
CA3023	2000	2	66	66	52

resistance is shown in Fig. 238. Maximum power output is measured at a level at which output distortion is just discernible on an oscilloscope.

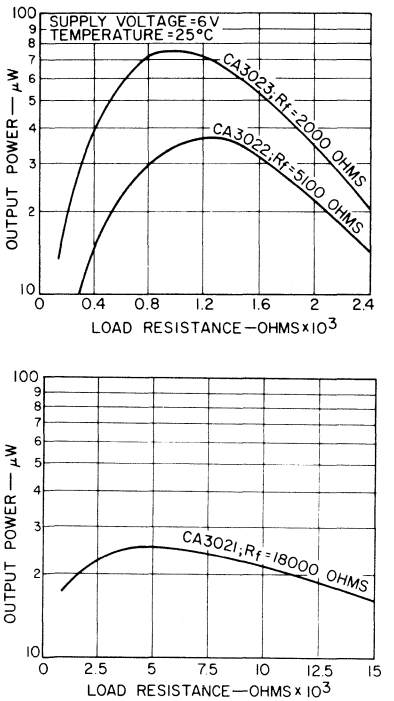


Fig. 238 — Maximum linear signal output of the CA3021, CA3022, and CA3023 as a function of load resistance.

Tuned Circuit in the Feedback Loop

When a parallel tuned circuit is included in the feedback path between terminals 3 and 7 of the CA3021, CA3022, or CA3023, the gain at resonance is a function of the equivalent resistance of the feedback loop. Gain characteristics of the three circuits as a function of feedback resistance are shown in Fig. 239. For each circuit, there is a value of feedback resistance R_f for which the gain approaches zero. This condition occurs when the small-signal transconductance g_m of the transistor Q4 is equal to the conductance of the parallel tuned circuit; signal

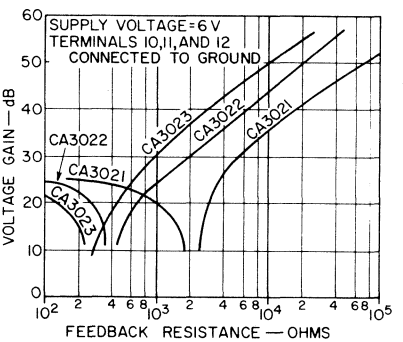


Fig. 239 — Voltage gain of the CA3021, CA3022, and CA3023 as a function of feedback resistance.

cancellation then results at terminal 7. In a tuned circuit designed with the correct feedback resistance R_f, therefore, zero gain can be obtained at the resonant frequency. The resistance values required for signal cancellation are 2000 ohms for the CA3021, 400 ohms for the CA3022, and 230 ohms for the CA3023. When the tuned-circuit impedance is made equal to these cancellation resis-

tance values at resonance, the gain increases at frequencies off resonance and a trapping effect results. For zero feedback resistance, the gain of each circuit is approximately 24 dB. For values of feedback resistance in excess of the cancellation resistance, the gain increases. When the tuned circuit has a resonant impedance higher than the cancellation resistance, the response is added to the video response characteristic, as shown in Fig. 240. Then, because no purely resistive value occurs that is equal to the cancellation resistance, no cancellation occurs.

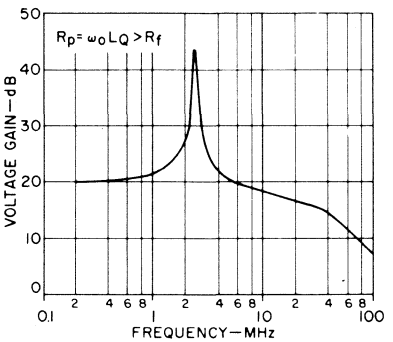


Fig. 240 — Voltage gain as a function of frequency in a band-pass amplifier when the tuned-circuit resonant impedance R_p is higher than the cancellation resistance R_{fc}.

The bandwidth of the response can be approximated by determining the total loading of R_p on the parallel tuned circuit in the feedback path, as follows:

$$R_p = \frac{R_T R_X (R4 + R8)}{(R_X + R_T)(R4 + R8) + R_X R_T}$$

$$= \omega_0 L_Q > R_{fc}$$

where R_T is the resistance at resonance of the unloaded Q, R_X is the resistance added to the tuned circuit for adjustment of gain, and (R4 + R8) is the series combination of the two common-collector load resistors. The 3-dB bandwidth for the response is given by

$$\frac{f_0}{\Delta f} = \frac{R_P}{X_L} = \frac{R_P}{X_c} = Q_L$$

Typical values for (R4 + R8) for the three circuits are 39000 ohms for the CA3021, 10900 ohms for the CA3022, and 4800 ohms for the CA3023.

Output Tuned Circuits

The curves of Fig. 238 indicate that capacitive coupling of the common-collector output transistor Q6 to a matched load severely limits the transistor output-voltage-swing capability. If the required mismatch is achieved by ac coupling of a tuned circuit directly across the output, the tuned circuit will be loaded by the low output impedance of the common-collector transistor. However, comparable output power can be obtained by use of a resistor in series with the circuit output and the tuned circuit. This arrangement provides a load for the common-collector transistor for frequencies off resonance of the tuned circuit, and prevents the possibility of reactive loads causing emitter-follower transistor instability.

Gain Control

The CA3021, CA3022, and CA3023 are connected as shown in Fig. 232(b) when gain-control application is desired. Transistors Q2 and Q5 are then included in the emitter-signal path of transistors Q1 and Q4, respectively. For maximum gain, a positive voltage is applied to terminal 2 which saturates transistors Q2 and Q5. If a voltage of 6 volts is applied to terminal 2, the typical gain-control current is 0.8 milliampere. The gain-control action is

provided by reduction of the voltage on terminal 2. The decreasing voltage causes transistors Q2 and Q5 to come out of saturation and present a high impedance in the emitter leads of transistors Q1 and Q4. It is important that good filtering and isolation be maintained at the agc terminal 2 because transistors Q2 and Q5 are in the linear active region for a portion of the agc range and can, therefore, provide gain for a signal on the agc terminal.

The minimum gain is determined by a combination of the gain of Q1 and feed-through to the collector of Q1 along a resistance path made up of R3 and R2. Because the signals are out of phase, there is a point at which cancellation of signal results. This cancellation occurs in all three circuits when terminal 2 is 0.5 volt more negative than terminal 11. It is accompanied by severe distortion of signal and AM modulation. Techniques for obtaining agc without reaching the cancellation point are discussed later.

When the maximum recommended feedback resistance for operating-point stability is used in the connection of Fig. 232(b), maximum gain is reduced because of the extra emitter resistance presented by the saturation resistance of transistors Q2 and Q5. Maximum voltage gain for each circuit is approximately 30 dB with the maximum recommended feedback resistance and a 6-volt supply. The typical agc range for each circuit is 55 dB with resistive feedback.

When a tuned circuit is used in the feedback loop, higher maximum gain can be obtained in the agc connection shown in Fig. 232(b). The maximum gain obtainable is approximately 50 dB when high feedback impedance is maintained. A self-resonant choke is a convenient element to add in the feedback loop to obtain high impedance because it provides wide bandwidth; resistance loading can be added to adjust the gain to the desired value. When a combination of self-resonant choke and added resistance is used, dc feedback is complete and the operating point is temperature-stable. Wide-bandwidth tuned circuits are suggested for all three circuits, but especially for the CA3022 and CA3023 because the bandwidth shifts with gain control, as shown in Fig. 241. For a tuned frequency of 3 MHz at full gain, for example, the resonance point of the tuned response increases slightly (about 5 per cent) for gain control of −20

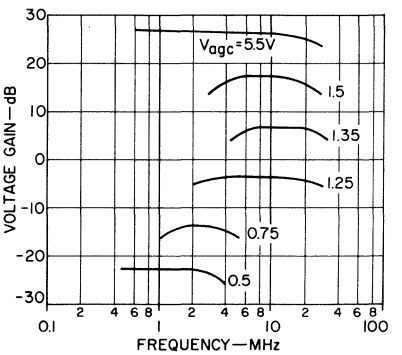


Fig. 241 — Effect of gain control on response characteristics of the CA3021, CA3022, or CA3023.

to −30 dB because of the combination of the low-frequency roll-off and the tuned response. In the region of gain control of −50 dB, the high-frequency roll-off affects the response and the resonant frequency decreases below 3 MHz (by about 10 per cent). At full agc, the tuned circuit becomes a trap in the feed-through path, minimum gain is achieved at the 3-MHz frequency, and the response is inverted, i.e., a notch occurs where a band pass had existed. When tuned circuits are included in

the feedback path of the gain-controlled amplifier, therefore, it is recommended that the bandwidth be chosen as wide as possible to minimize detuning effects. Desired bandwidth control should be obtained at the input, at the output, or in the feedback path of stages without gain control.

The use of emitter degeneration as a gain-control technique improves signal-handling capability. At full gain control, signals as high as 2 volts rms can be handled without the occurrence of serious overload distortion. Typical cross-modulation characteristics for the CA3021, CA3022, and CA3023 with only feedback resistance in the feedback loop are shown in Fig. 242. Maximum gain for each circuit is approximately 30 dB. When a tuned circuit is used in the feedback loop, more gain-control range is available as a result of the feedthrough reduction. Depending on the impedance of the tuned circuit, the gain-control range is between 60 and 80 dB. The cross-modulation characteristics when tuned circuits are used are similar to those obtained with resistive feedback except for modifications caused by different feedback characteristics of interfering signals outside the tuned-circuit pass band.

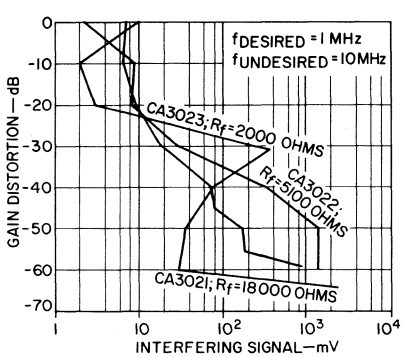


Fig. 242 — Cross-modulation distortion characteristics of the CA3021, CA3022, and CA3023.

Limiting

For applications in which signal limiting is required, the diodes of the CA3021, CA3022, and CA3023 are connected as shown in Fig. 232(c). At low signal levels, the diodes are cut off, and the gain performance is similar to that described previously except for some bandwidth reduction caused by the inherent capacitance of the diodes. For large input-signal swings in the negative direction, the collector of transistor Q1 becomes positive and the collector of transistor Q4 becomes negative, and diode D2 begins to conduct. This action clamps the collector of Q1 to the collector of Q4 and, because the diode is in the feedback path, reduces the gain. For positive swings at the input, the collector of transistor Q1 becomes negative and the output at terminal 8 becomes positive. Two effects tend to limit input signals of positive polarity: transistor Q4 going to cutoff, and diode D3 going into conduction. When the circuits are connected as shown in Fig. 232(c), limiting is symmetrical at the onset. With increased signal, however, the symmetry is not perfectly preserved because of dc shift in the circuit. Typical output-signal characteristics as a function of input level are shown in Fig. 243. The lack of symmetry at high input levels causes a decrease in power output, as shown in the waveforms.

Limiting characteristics for the CA3021, CA3022, and CA3023 are measured in the circuit configuration shown in Fig. 244. The output tuned circuit is designed to provide filtering for the desired output frequency so that rms values of output voltage

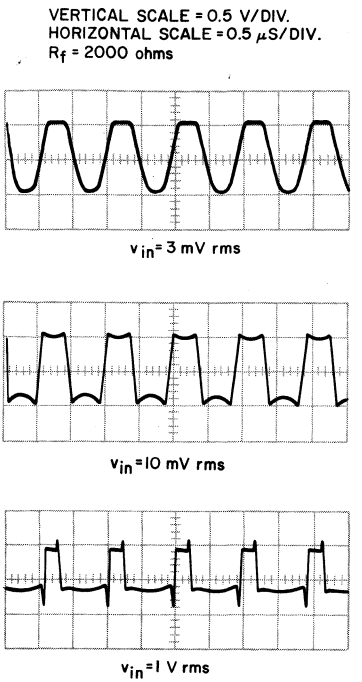


Fig. 243 — Output waveforms obtained in limiter applications using the CA3021, CA3022, or CA3023.

can be obtained. Limiting characteristics are measured for two types of feedback, resistive and tuned circuit; results are shown in Fig. 245. When a resonant circuit is used in the feedback loop, the gain of the circuits is higher, and limiting occurs at a lower input level. The effects of multistage limiting are described later.

Noise Performance

Table XXVII shows typical noise figures for the CA3021, CA3022, and CA3023 circuits for a frequency of 1 MHz, a supply voltage of 6 volts, and a source resistance of 50 ohms. The data in the first column of noise figures were measured in

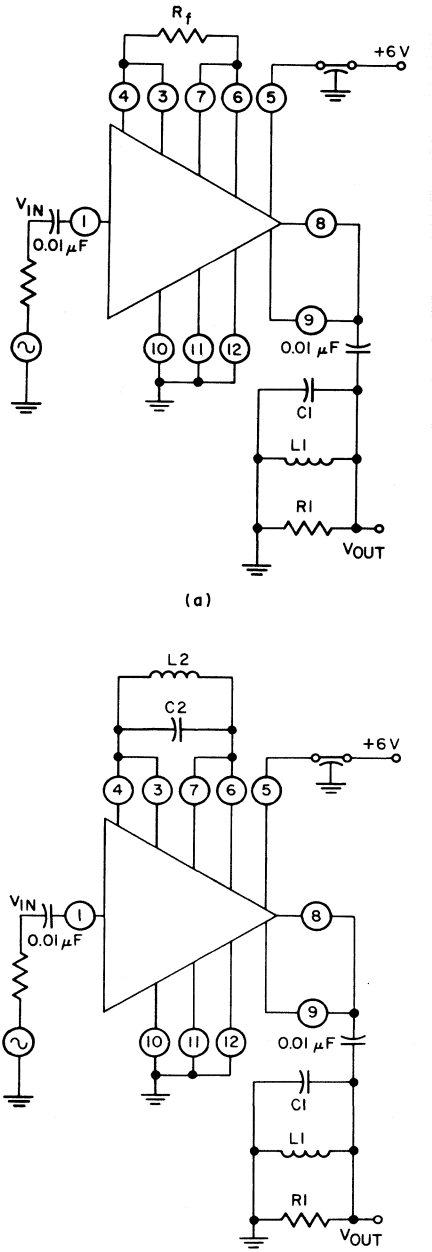


Fig. 244 — Test circuit used to evaluate limiting characteristics of the CA3021, CA3022, and CA3023.

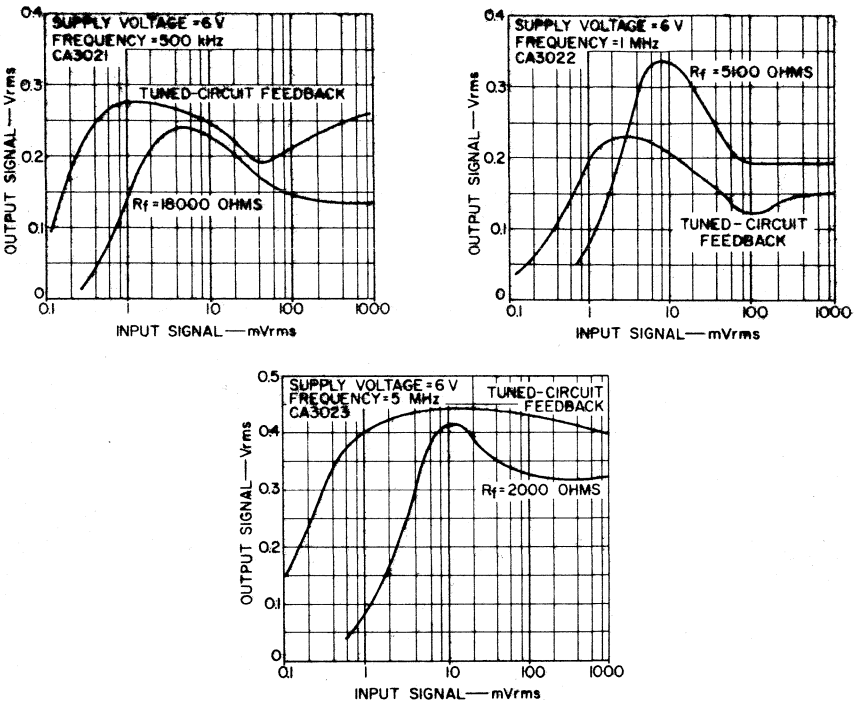


Fig. 245 — Limiting characteristics of the CA3021, CA3022, and CA3023.

Table XXVII — *Typical Noise Figures for the Integrated-Circuit Wide-Band Amplifiers*

Circuit	Noise Figure — dB Term. 10, 11, 12 connected to ground; gain = 40 dB	AGC operating, noise measured for maximum gain of 30 dB
CA3021	5.8	7.5
CA3022	7.1	8.7
CA3023	7.2	8.7

the connection shown in Fig. 232(a); the second column shows data measured in the connection shown in Fig. 232(b).

Applications

The following paragraphs describes several typical applications of the integrated-circuit wide-band amplifiers.

Video Amplifiers—The use of single CA3021, CA3022, or CA3023 integrated circuits in video applications was discussed previously. For an evaluation of iterative video performance, two CA3022 circuits were operated in cascade. Each circuit employed 0.01-microfarad coupling capacitors and feedback resistors of 2000 ohms. Performance data can be summarized as follows:

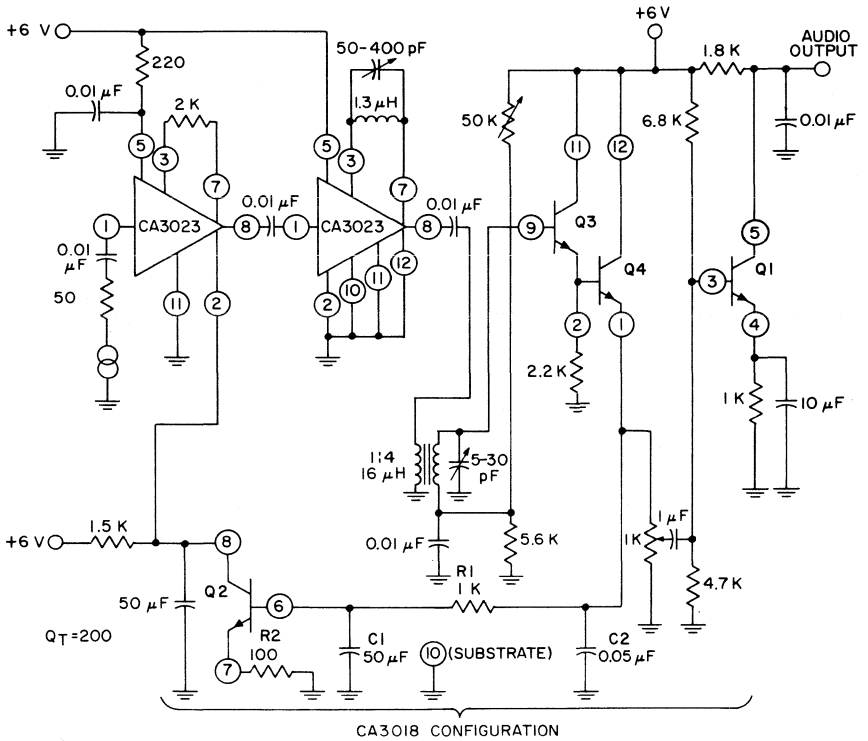
Supply voltage	6	volts
Supply current	4.5	mA
Power dissipation	27	mW
Voltage gain	61	dB
Maximum undistorted output with 510-ohm load	0.25	Vrms
Signal level for a 3-dB signal-to-noise ratio	11	μV
Dynamic range (input-output linearity)	27	dB
Bandwidth, 3-dB points:		
upper frequency	10.5	MHz
lower frequency	50	kHz

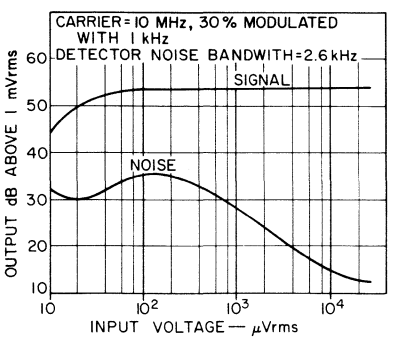
10-MHz IF Amplifier—Fig. 246 shows a 10-MHz amplifier employing two CA3023 circuits. The first stage is operated in a broadband mode with a 2000-ohm feedback resistor between terminals 3 and 7, in accordance with the design rules described previously. The second stage is a tuned if amplifier. Because the sinusoidal output capability of the CA3023 at 10-MHz is in the 200-millivolt range, it is necessary to step up the voltage to drive the envelope detector; therefore, a tuned transformer that has a 1-to-4 turns ratio is used at the second-stage output. The total effective circuit Q for this if configuration is 200, and the full rf voltage gain is 86 dB from the input of the first stage to the output of the step-up transformer.

A CA3018 integrated-circuit transistor array is used to provide detection, audio amplification, and dc amplification. (The CA3018 circuit is described in a later section.) Detection is provided by transistors Q3 and Q4 of the CA3018; the detected output is passed through a low-pass filter (C1, C2, and R1) and applied to the agc amplifier transistor Q2. Transistor Q2 goes from cutoff to saturation with increasing signal. The voltage drop across the 100-ohm degenerative resistor R2 prevents the gain-control voltage in terminal 2 of the first CA3023 amplifier from decreasing below 0.5 volt and causing signal cancellation. Transistor Q1 of the CA3018 provides audio gain and is biased in a conventional manner. Fig. 246 also shows the output-signal and noise characteristics of the circuit as functions of rf input level for an input signal that is 30-per-cent modulated by a 1-kHz sine wave. The audio-output equivalent-noise bandwidth is 2.6 kHz.

455-kHz IF Amplifier—Fig. 247 shows a 455-kHz two-stage if amplifier using the CA3021. The tuned-circuit approach discussed previously is used in the first stage. The rf feedback choke is self-resonant at 455 kHz and has a Q of 3.2 in the circuit. The second stage is a video amplifier. Input filtering would normally be provided to obtain the desired if response. For the particular choice of stage gain and agc loop gain, an interstage pad network is used to maintain stability and achieve an acceptable signal-to-noise ratio with gain control. The CA3018 output configuration is essentially the same as that used in the circuit of Fig. 246. The signal and noise characteristics of the 455-kHz amplifier are also shown in Fig. 247 for the same conditions used for the 10-MHz amplifier.

28-MHz Two-Stage Limiter Amplifier—Fig. 248 shows the circuit diagram of a 28-MHz two-stage limiter amplifier using two CA3023 integrated circuits. Terminals 3 and 7 are connected to terminals 4 and 6, respectively; terminal 8 is connected to terminal 9 to provide limiting action. A self-resonant coil in parallel with a 2000-ohm resistor is inserted in the feedback loop of each amplifier to provide gain and stability. The bandwidth of the system



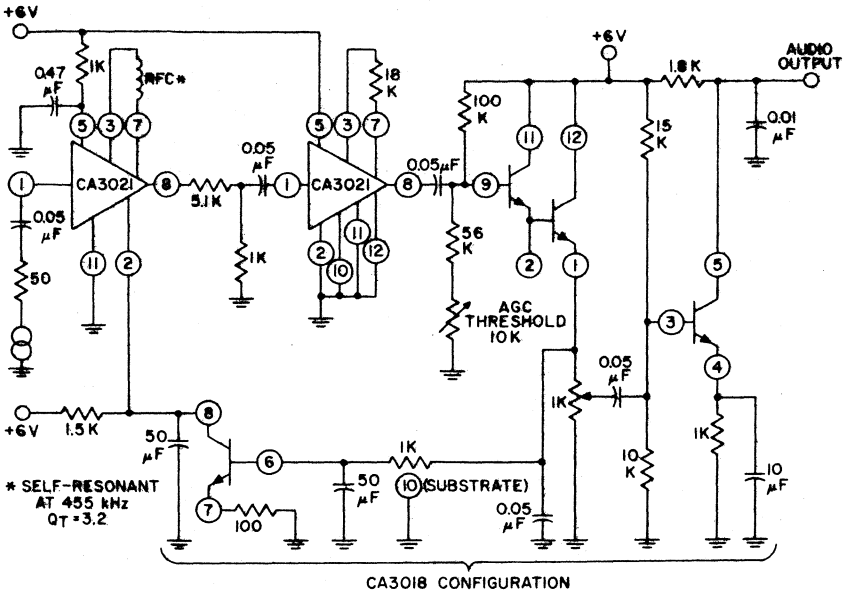


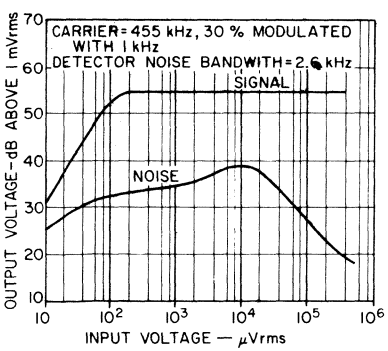
All resistance values in ohms unless otherwise specified.

Fig. 246 — Circuit diagram and performance curves for 10-MHz if amplifier using two CA3023 circuits.

before limiting is 3.8 MHz, and the effective Q is 7.35. The total gain is 61 dB (30.5 dB per stage), and the power dissipation is 66 milliwatts. Fig. 248 also shows the limiting performance of the system. Full limiting occurs at an input of 300 microvolts.

500-kHz Limiting Amplifier—Fig. 249 shows the circuit diagram of a 500-kHz limiting amplifier using two CA3021 circuits. Two 500-kHz self-resonant chokes are used in the feedback path. A tuned circuit is included in the output to obtain a sine-wave output. The limiting characteristics of this amplifier are also shown. Although limiting occurs for noise, a





All resistance values in ohms unless otherwise specified.

Fig. 247 — Circuit diagram and performance curves for 455-kHz if amplifier using two CA3021 circuits.

limited signal is apparent above the noise at an input signal of 1 microvolt. Because of the noise and early limiting, voltage gain can only be estimated; however, it is at least 100 dB. Good limiting performance is obtained for input signals up to 3 volts rms. Total power drain for the circuit with a 6-volt supply is approximately 6 milliwatts.

WIDE-BAND AMPLIFIER FOR INDUSTRIAL AND COMMERCIAL APPLICATIONS

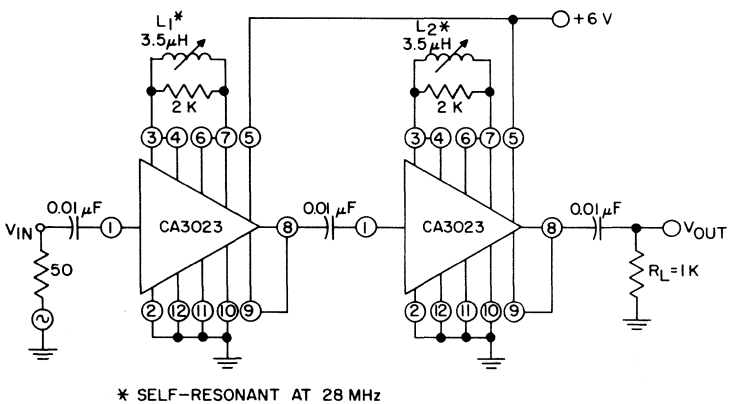
The CA3040 integrated circuit is designed for use in industrial and commercial applications that simultaneously require high gain and wide bandwidth at frequencies up to 100 MHz. This circuit, which is supplied

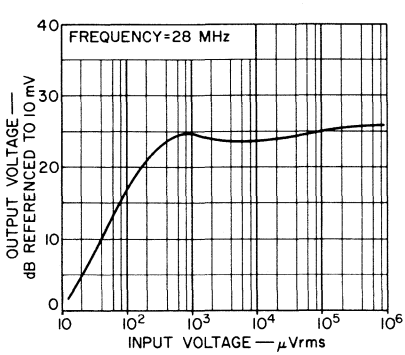
in a 12-terminal TO-5-style package, features a balanced differential voltage gain of 37 dB with less than 1 dB of imbalance and provides a typical 3-dB bandwidth of 55 MHz. Useful voltage gain is obtained well beyond the 3-dB frequency roll-off point which, in some applications, extends to frequencies up to 200 MHz. Additional features of the CA3040 include temperature compensation for gain and voltage over the −55 to 125°C temperature range, a choice of zero or 180-degree phase shift from input to output terminals, and high input and low output impedance characteristics over a broad bandwidth.

Circuit Description

Fig. 250 shows the schematic diagram for the CA3040 circuit. The heart of this circuit consists of two differentially connected cascode amplifiers that form a so-called "differential cascode" amplifier. The transistors Q3 and Q4 are common-emitter amplifiers which are connected at the emitters to form the differential transfer junction. The common-base transistors Q5 and Q6 are emitter-driven from the common-emitter transistors Q3 and Q4, respectively, to form two differential-cascode amplifier pairs.

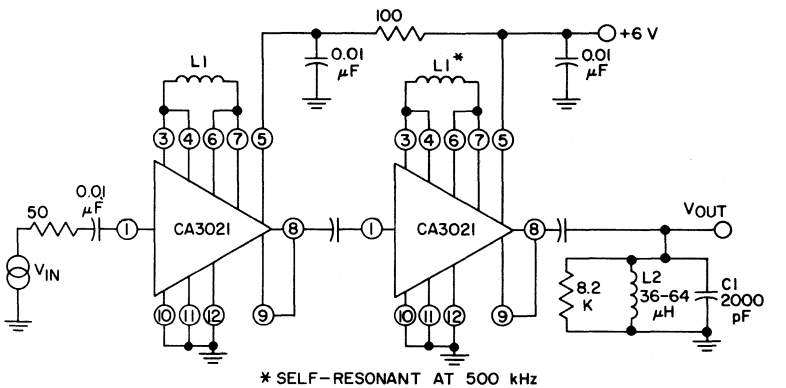
Each common-emitter amplifier is buffer-isolated from the input termi-

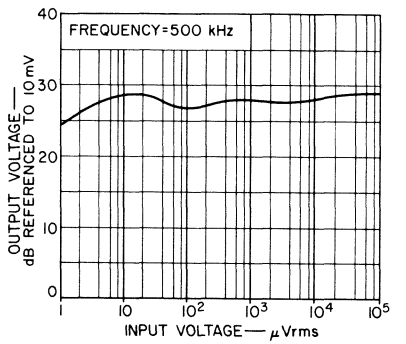




All resistance values in ohms unless otherwise specified.

Fig. 248 — Circuit diagram and limiting performance of two-stage 28-MHz limiter-amplifier using the CA3023.





All resistance values in ohms unless otherwise specified.

Fig. 249 — Circuit diagram and limiting performance of two-stage 500-kHz limiter-amplifier using the CA3021.

nals by an emitter-follower stage for high input impedance and minimum co-channel phase pulling. Each common-base amplifier of the cascode is coupled to the output terminals by use of an emitter-follower stage for low impedance at the output terminals.

When the signal flow through the device is from terminal 4 to terminal 12 and from terminal 6 to terminal 10, there is a 180-degree internal phase shift; when signal flow is from terminal 4 to terminal 10 and from terminal 6 to terminal 12, the phase shift is zero. Fig. 251 shows a signal-flow diagram for the former case. The dc feedback loop shown is a bias-selection and temperature-tracking network. The bias network consists of reference diodes D1 and D2, transistor Q9, and resistors R3, R4, R7, R8, R9, and R10. The bias network selected by proper connection of terminals 3, 7, 8, and 9 determines the "mode" of desired temperature tracking.

Bias Modes

The dc bias-point stability or ac gain stability of the CA3040 is maintained over the temperature range of −55 to +125°C by the choice of two bias modes. These bias modes are selected by proper connection of the transistor Q9 biasing network. Fig. 252 shows the bias modes for (a) constant voltage and (b) constant gain.

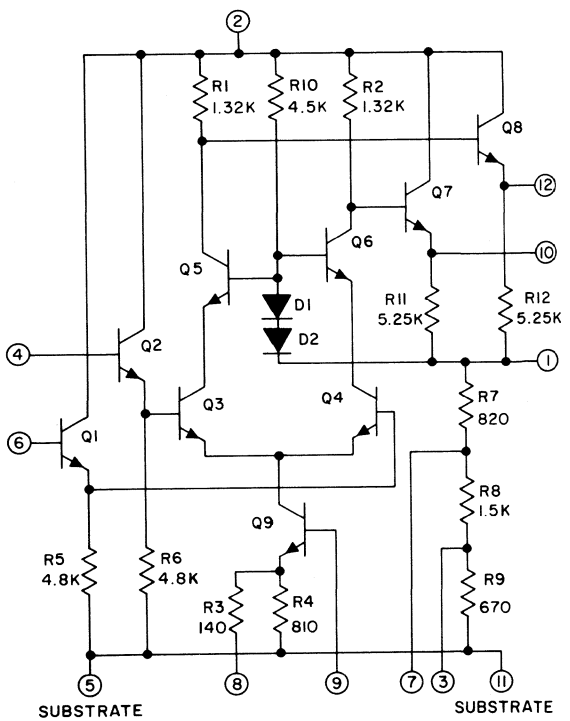
In the constant-voltage bias arrangement, terminals 3 and 8 are

open, and terminals 7 and 9 are externally connected. This circuit yields a constant-voltage output for applications that use dc coupling to succeeding stages or that require maximum dynamic range over the specified temperature. DC voltage variation in this mode is less than 0.1 volt over the entire temperature range; ac gain variations is ±2 dB.

In the constant-gain bias arrangement, terminals 3 and 9 are externally connected, terminal 7 is open, and terminal 8 is externally connected to the substrate terminals 5 and 11. In this mode, the ac gain is extremely stable (typical variation is 0 dB); the dc variation at the output terminals is ±0.8 volt.

For most applications, the constant-voltage bias mode is preferred. This mode provides typical ac-gain variation of less than 0.5 dB over the range from room temperature (25°C) to 85°C ambient. The dynamic range in this mode remains high, and the circuit exhibits less distortion and greater common-mode range for large-signal output swings. Finally, this mode requires one less terminal connection and provides a less complex layout design than that required for the constant-gain circuit.

Both modes have identical power-supply requirements, as illustrated in Figs. 252 and 253. Fig. 252 shows the use of a single 12-volt power supply, and Fig. 253 shows balanced dual positive and negative 6-volt



All resistance values in ohms unless otherwise specified.

Fig. 250 — CA3040 integrated-circuit wideband amplifier.

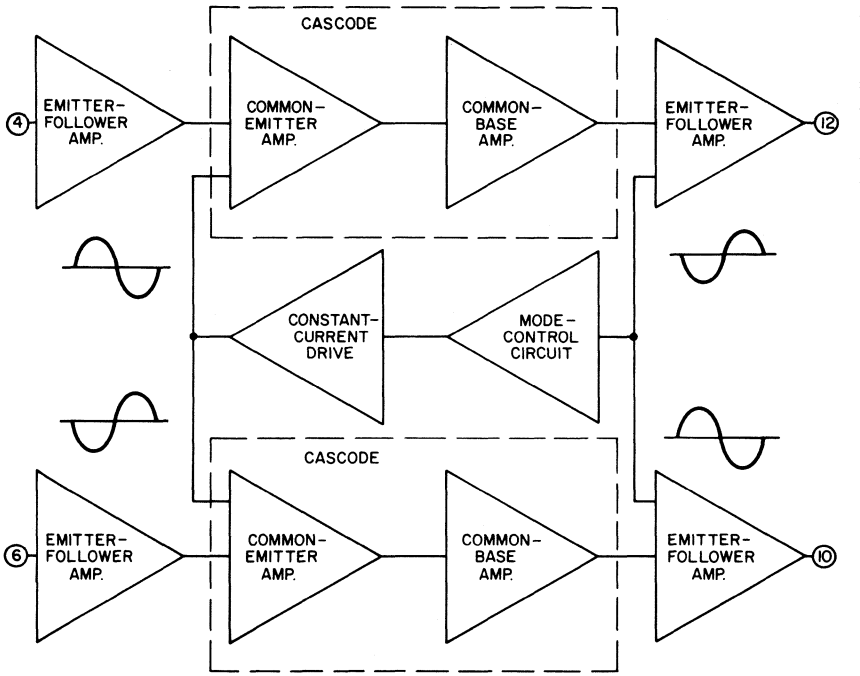
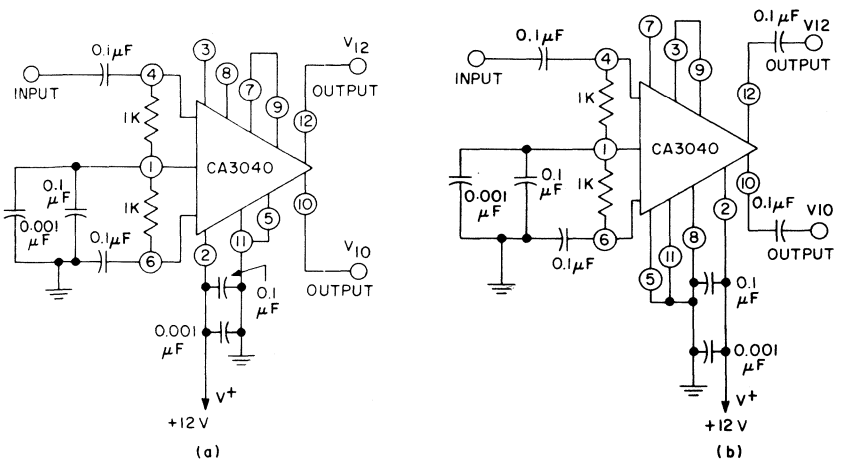


Fig. 251 — Signal-flow diagram of the CA3040.



All resistance values in ohms unless otherwise specified.

Fig. 252 — Bias configurations for the CA3040 using a single 12-volt power supply: (a) constant-voltage bias; (b) constant-gain bias.

power supplies. In Fig. 252(a) and 252(b), the inputs are bias-coupled to terminal 1, which is a reference to the center point of the power supply. Although this connection is most commonly used to maintain the common-mode range, any dc supply or "stiff" bleeder (at one-half the power-supply voltage) may be used. It should be noted that terminal 1 should not be direct-coupled to any external circuit except as a bias source; otherwise, the input transistors or the temperature-compensation characteristic will not remain within the limits.

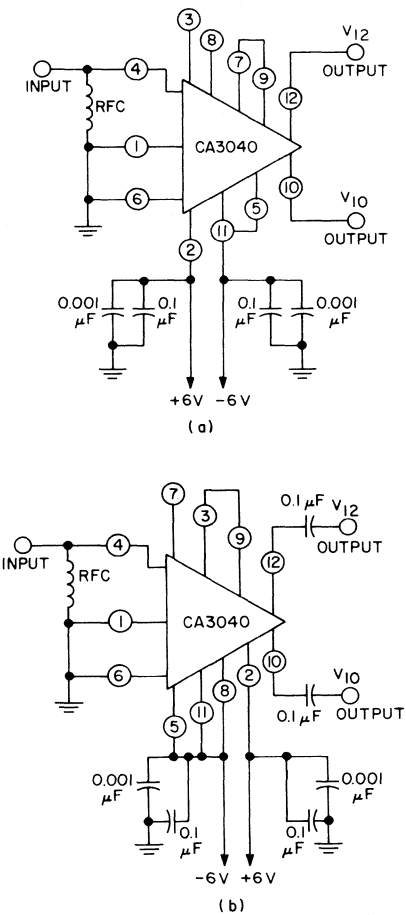


Fig. 253 — Bias configurations for the CA3040 using balanced dual (±6-volt) power supplies: (a) constant-voltage bias; (b) constant-gain bias.

Characteristics and Ratings

The high-frequency capability of the CA3040 is a characteristic of the advanced design that has been developed in the second generation of monolithic integrated-circuit devices. The following are typical performance characteristics of the CA3040.

Fig. 254 shows gain as a function of frequency for the CA3040. The 3-dB bandwidth is typically 55 MHz, and the minimum is 40 MHz at either differential output when terminal 4 is driven from a single-ended 50-ohm source. At 1 MHz, with a 63-millivolt output level, imbalance is not greater than ±1 dB. In contrast

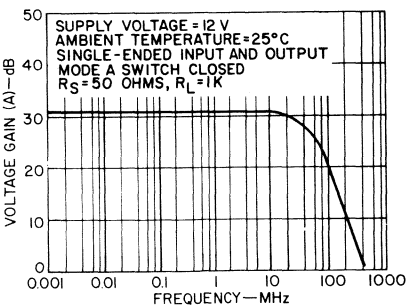


Fig. 254 — Voltage gain as a function of frequency.

to the more common specification of minimum gain at high frequency, the performance of the CA3040 is given in terms of flat bandwidth relative to the 1-MHz-gain test point.

Fig. 255 shows the input resistance and capacitance characteristics of the CA3040. (The input resistance R_{IN} is plotted as conductance G_{IN} because the resistance magnitude approaches infinity at approximately 22 MHz.) These curves were obtained with the output terminals

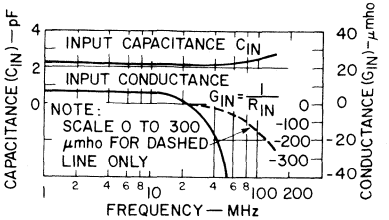


Fig. 255 — Input impedance characteristics.

shorted and by use of the constant-voltage bias configuration. Although this form of bias has a second-order effect on the input and output capacitance, the input and output capacitance and conductance values for the circuits of Figs. 252 and 253 do not change appreciably from those shown in Fig. 255. The negative value of input resistance remains high over the high-gain region and has sufficient magnitude (several thousand ohms) at 150 MHz so that the amplifier remains stable for practical values of the input matching impedance. From 1 to 10 MHz, this resistance remains approximately 150 kilohms. The input capacitance C_{IN} of the CA3040 is approximately 2.2 picofarads and remains relatively constant over the useful frequency range.

Fig. 256 shows the output resistance and output capacitance of the CA3040 amplifier as a function of frequency. The output resistance of the circuit is approximately 125

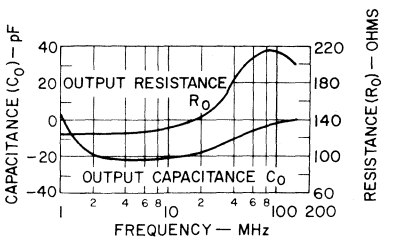


Fig. 256 — Output impedance characteristics.

ohms at low frequencies and gradually rises to 215 ohms at 100 MHz, but decreases again to 200 ohms at 150 MHz. Although a lower output impedance (50 ohms or less) is more desirable, the higher output impedance results in greater temperature-stable gain. When necessary, however, the output impedance can be reduced by addition of another emitter-follower stage. Even when this stage is directly coupled to the output, it has little effect on the dc stability for bias-current drains less than 0.1 milliampere.

Fig. 257 shows the 30-MHz noise figure as a function of source resistance. For low-noise applications, shunt-biasing resistors should be replaced by low-loss input matching

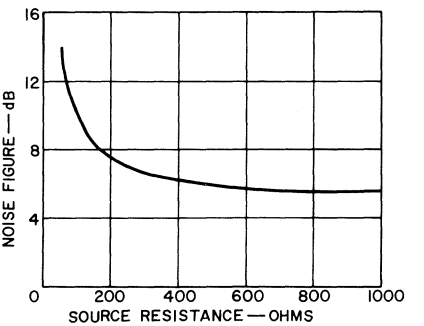


Fig. 257 — Noise figure as a function of source resistance.

circuits which can include rf chokes, a transformer, or inductive-capacitive input circuits. It is important that the dc resistances of the two stages remain equal. An unequal dc voltage drop across the bias network produces a large dc offset at the output.

Fig. 258 shows the 1/f noise characteristics of the CA3040. The curves represent different values of source resistance. The equivalent input 1/f noise is expressed in nanovolts per square root of the frequency. The limiting low-frequency

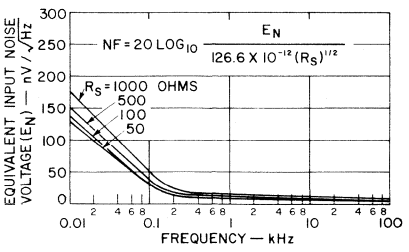


Fig. 258 — Equivalent input noise voltage as a function of frequency.

1/f noise approaches 125 nanovolts per $\sqrt{\text{Hz}}$ at 10 Hz and drops to approximately 25 nanovolts per $\sqrt{\text{Hz}}$ at 100 Hz. Above 200 Hz, the noise component is primarily shot noise.

The noise figure NF is related to the total noise voltage E_{N_T} as follows:

$$NF = 20 \log_{10} \frac{E_{N_T}}{(4KTR_S)^{1/2}}$$

$$= 20 \log_{10} \frac{E_{N_T}}{126.6 \times 10\text{-}12(R_S)^{1/2}}$$

where E_{N_T} is the noise voltage in volts per $\sqrt{\text{Hz}}$, K is Boltzmann's constant (1.38×10^{-23} joule/°K), T is the temperature in degrees Kelvin, and R_S is the external source resistance in ohms.

The CA3040 has a linear phase-shift characteristic. Fig. 259(a)

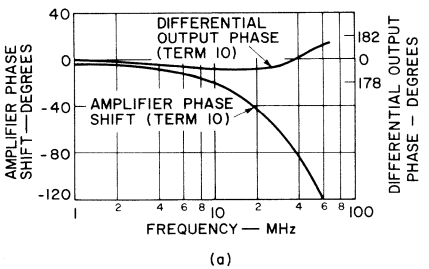
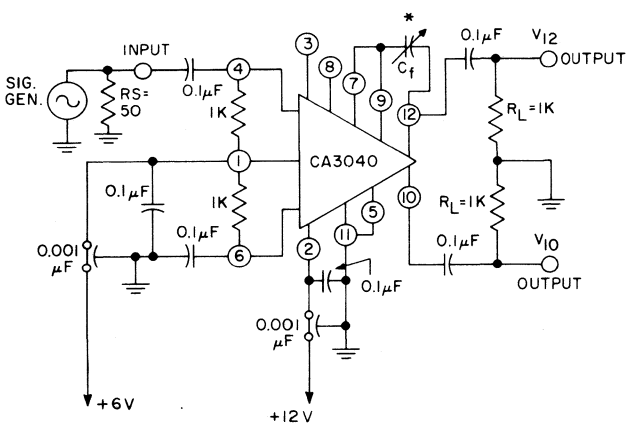


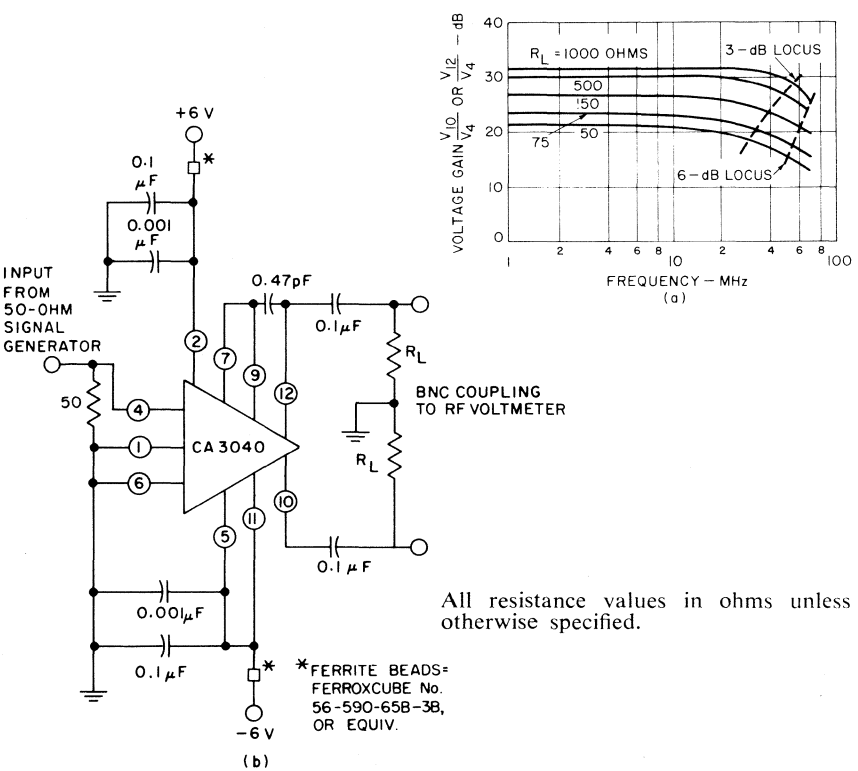
Fig. 259 — (a) Amplifier phase shift and differential output phase as a function of frequency and (b) test circuit for CA3040.

All resistance values in ohms unless otherwise specified.



* VARIABLE CAPACITANCE (0.5 – 1.0 μF) ADJUSTMENT FOR EQUAL 3-dB BANDWIDTH AT AMPLIFIER OUTPUTS, TERMINALS 10 AND 12.

shows the amplifier phase shift from input terminal 6 to output terminal 10 and the differential phase between outputs over the frequency range from 1 to 60 MHz. The test amplifier of Fig. 259(b) was used to obtain the data for these curves. The resistive portion of the output-impedance load in Fig. 259(b) consists primarily of the 1-kilohm resistors. The capacitive load consists of all essential circuitry as well as BNC connectors and phase-meter input probes that represent approximately 8.5 picofarads. Any imbalance from 180 degrees of differential phase at the output terminals remains small in comparison to the reference input-to-output phase shift and is typically less than 1 degree at frequencies up to 50 MHz. Fig. 259 shows the differential output phase with terminal 10 given as the reference phase. The imbalance exists because the feedthrough capacitance from terminal 10 to terminal 9 is greater than that from terminal 12 to terminal 9. The constant-current transistor (Q9 of Fig. 250) amplifies this unbalanced stray capacitance coupling. A fundamental correction for phase can be made by adjustment of the output-capacitance load. In Fig. 254(b), a variable capacitance C_f is used between terminals 9 and 12 for this purpose. The addition of C_f makes it possible to adjust the output signals for phase and gain



All resistance values in ohms unless otherwise specified.

Fig. 260 — (a) Frequency response curves and (b) test circuit for CA3040.

balance at the high-frequency roll-off point.

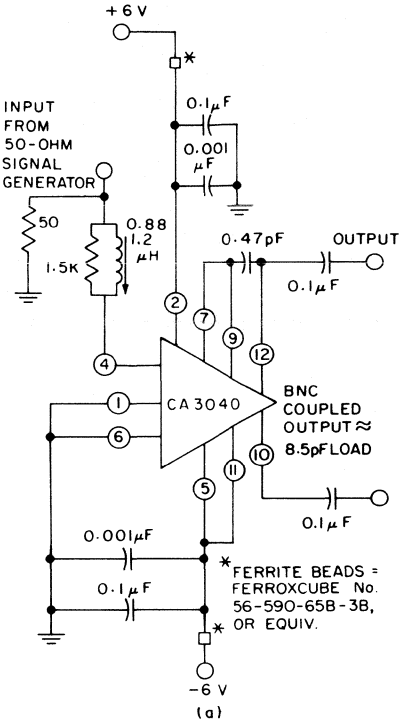
Fig. 260(a) shows the frequency response of the CA3040 for various values of load resistance. The test circuit used for these measurements is shown in Fig. 260(b). This amplifier is biased from a balanced dual power supply, but is otherwise similar to the circuit of Fig. 254(b). The curves are valid for either method of biasing.

The low-frequency portion of the curves of Fig. 260(a) shows the decrease in gain with decreased load resistance which is characteristic of the 125-ohm output resistance. The higher-frequency range shows the reduction in bandwidth as the load resistance is decreased. This output characteristic is typical of emitter-follower circuits and is caused by a reduction in transistor beta at higher frequencies.

Wide-Band Amplifiers

In basic amplifier circuits, the bandwidth of the CA3040 may be increased by use of conventional RL and RC peaking, as well as feedback correction, at the input and output stages. Fig. 261(a) shows a typical wide-band amplifier configuration using the CA3040; Fig. 261(b) shows its frequency response. The circuit has a wide-band series-peaked bandwidth greater than 90 MHz at the 3-dB point and greater than 85 MHz to within ±1 dB of gain variation. In the circuit of Fig. 261(a), care is taken to avoid "over-peaking" of the input at higher signal levels so that limiting and distortion effects are minimized.

The frequency-response curves shown in Fig. 261(b), as well as in Figs. 254(a) and 260(a), were obtained with conventional output circuits that contain BNC connectors coupled to the rf voltmeters and produce a total capacitive load of approximately 8 to 9 picofarads. The curve of Fig. 254(a) shows a roll-off characteristic of approximately 12 dB per octave in the 100-to-200-MHz range which is the result of capacitive loading of the cascode and emit-



All resistance values in ohms unless otherwise specified.

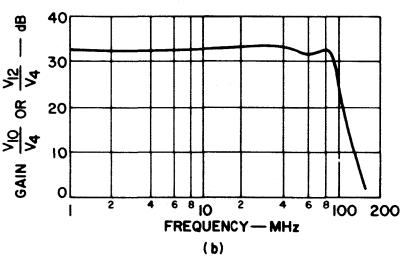


Fig. 261 — (a) Typical CA3040 wide-band-amplifier circuit with series input peaking and (b) frequency-response characteristics.

ter-follower output stages. These output stages may be peaked for partial compensation of the bandwidth loss that results from emitter-follower output loading. The remaining loss in bandwidth, however, results from internal circuit effects and is less easily corrected.

Fig. 262(a) shows a wide-band amplifier circuit that produces 50 dB ±1 dB of gain up to 53 MHz, as shown by the curve of Fig. 262(b). The curve shown is for an input-drive signal of 1.0 millivolt rms. The post amplifier has a broadband capability of approximately 85 MHz and uses adjustable rf coils (Miller Type 20A□□□RBI series, or equivalent). The adjustable capacitor at the emitter or the cascode serves to "over peak" the post amplifier and compensate for the RC roll-off of the CA3040 amplifier. With this type of peaking compensation, a flat response that deviates less than 0.2 dB up to 50 MHz is obtained. Wide-band capability of the post amplifier is also achieved through the use of high-performance silicon n-p-n transistors. The RCA-40235 has a high gain-bandwidth product f_T and a low collector-to-base feedback capacitance C_{cb} suitable for television rf applications. The 2N5187 is a high-speed switching transistor that has all the basic requirements for economical line-driver applications. The peaking circuit is of the series-shunt type at the collector of the RCA-40235 cascode. Because high idle current is needed in the amplifier output stage, the output level before limiting is set for the minimum requirement necessary for the desired level of peak-to-peak output signal. In this case, a peak-to-peak signal of 2 volts is easily obtained to drive a 50-ohm line that is matched at both ends.

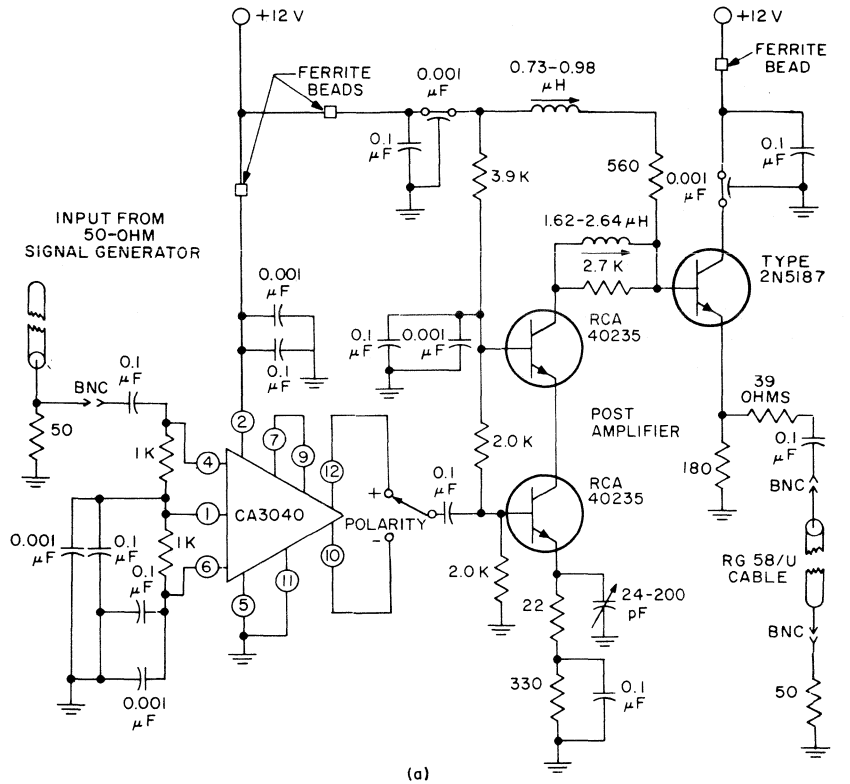
Stability

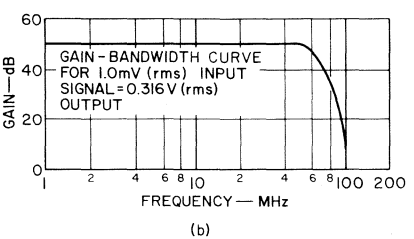
In the classical analysis, stability is evaluated as a function of the transfer impedance parameter. The number of possible operating modes and bias options, each of which is evaluated over the useful frequency range, limits the practicality of this type of analysis for the CA3040. Such an analysis would be further complicated by the fact that y-parameter data are applicable only at the discrete frequency at which they are taken. In view of these factors, the characteristics of the CA3040 are guaranteed to have a reasonable stability margin through evaluations in test circiuts and by integrity of design. Poor circuit design or improper layout, however, can reduce the stability margin so that oscillations can possibly result.

The differential-amplifier configuration of the CA3040 offers the advantage in wideband amplifier applications of neutralizing its own feedback. For this reason the circuit layout and printed-board pattern should be designed with a high degree of symmetry.

For stability purposes, terminal 9 of the CA3040 should not be bypassed because common-base oscillations may result in the constant-current transistor Q9. This effect, however, may be used to advantage in oscillator and mixing applications.

For some applications, such as wide-band if amplifiers, it is desirable to limit the high-frequency characteristics of the CA3040. In this case, series resistors in the base input leads of transistors Q1 and Q2 are recommended. Resistances of 10 to 100 ohms in series with terminals 4 and 6 not only limit the bandwidth but also act as parasitic suppressors.





All resistance values in ohms unless otherwise specified.

Fig. 262 — (a) 58-MHz wide-band amplifier including post amplifier and (b) frequency-response characteristic.

WIDE-BAND POWER AMPLIFIERS

The RCA CA3020 and CA3020A integrated circuits are multipurpose, multifunction power amplifiers designed for use as power-output amplifiers and driver stages in portable and fixed communications equipment and in ac servo control systems. The flexibility of these circiuts and the high-frequency capabilities of the circuit components make these types suitable for a wide variety of applications such as broadband amplifiers, video amplifiers, and video line drivers. Voltage gains of 60 dB or more are available with a 3-dB bandwidth of 8 MHz.

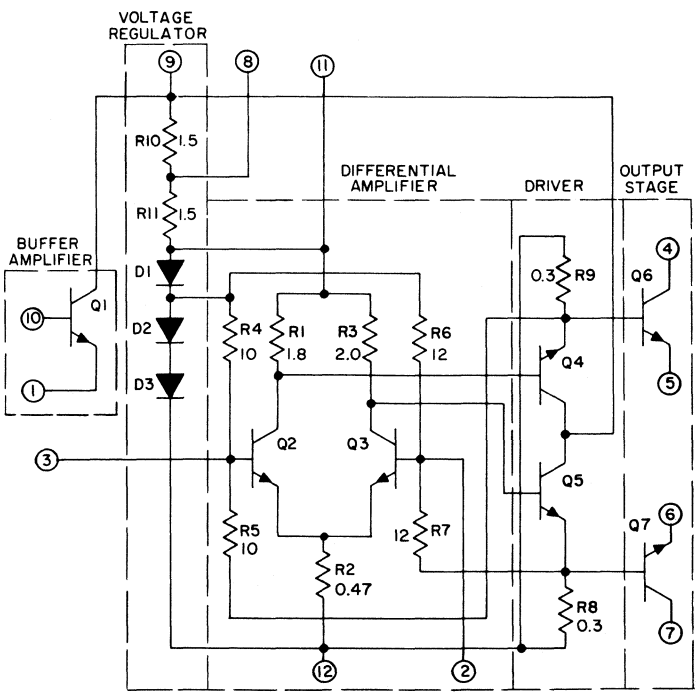
The following discussions are applicable to both integrated-circuit types. The CA3020A can operate in

all circuits shown for the CA3020. The CA3020, on the other hand, has more limited voltage- and current-handling capability and must not be used in applications which require voltage swings on the output transistors greater than 18 volts or peak currents in excess of 150 milliamperes.

The CA3020 and CA3020A are designed to operate from a single supply voltage which may be as low as +3 volts. The maximum supply voltage is dictated by the type of circuit operation. For transformer-loaded class B amplifier service, the maximum supply voltages are +9 and +12 volts for the CA3020 and the CA3020A, respectively. When operated as a class B amplifier, either circuit can deliver a typical output of 150 milliwatts from a +3-volt supply or 400 milliwatts from a +6-volt supply. At +9 volts, the idling dissipation can be as low as 190 milliwatts, and either circuit can deliver an output of 550 milliwatts. An output of slightly more than 1 watt is available from the CA3020A when a +12-volt supply is used.

Circuit Description

Fig. 263 shows the schematic diagram of the CA3020 or CA3020A, and indicates the five functional blocks into which the circuit can be divided for understanding of its operation. Fig. 264 shows the relationship of these blocks in block-diagram form.



All resistance values in ohms unless otherwise specified.

Fig. 263 — CA3020 or CA3020A integrated-circuit amplifier.

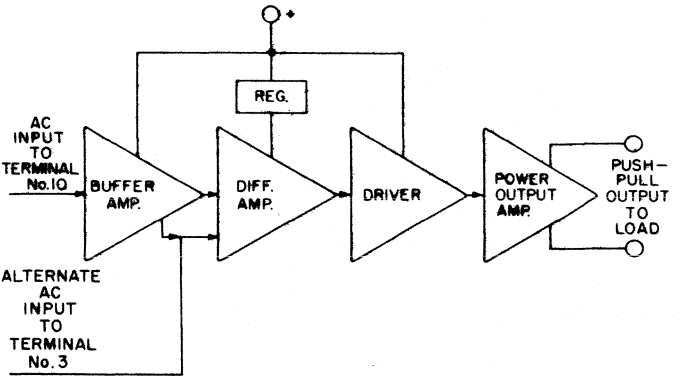


Fig. 264 — Functional block diagram of the CA3020 or CA3020A.

A key to the operation of the circuit is the voltage regulator consisting of diodes D1, D2, and D3 and resistors R10 and R11. The three diodes are designed to provide accurately controlled voltages to the differential amplifier so that the proper idling current for class B operation is established in the output stage. The characteristics of these monolithic diodes closely match those of the driver and output stages so that proper bias voltages are applied over the temperature range of −55 to +125°C. The close thermal coupling of the circuit protects it against thermal runaway within the prescribed temperature and dissipation ratings of the devices.

The differential amplifier operates in a class A mode to supply the power gain and phase inversion required for the push-pull class B driver and output stages. In normal operation, an ac signal is capacitively coupled to terminal 3, and terminal 2 is grounded through a suitable capacitor. When the signal becomes positive, transistor Q2 is turned on and its collector voltage changes in a negative direction. The same current flows out of the emitter of Q2 and tends to flow to ground through resistor R2. However, the impedance of R2 is high compared to the input impedance of the emitter of Q3, and an alternate path is available to ground through the emitter-to-base junction of transistor Q3 and then through the bypass capacitor from terminal 2 to ground. Because this path has a much lower impedance than R2, most of the current takes this alternate route. The signal current flowing into the emitter of Q3 reduces the magnitude of that current and, because the collector current is nearly equal to the emitter current, the collector current in Q3 drops and the collector voltage rises. Thus, a positive signal on terminal 3 causes a negative ac voltage on the collector of transistor Q2 and a positive ac voltage on transistor Q3, and provides the out-of-phase signals required to drive the succeeeding stages. It should be noted that the differential amplifier is not balanced; resistor R3 is ten per cent greater than R1. This unbalance is deliberately introduced to compensate for the fact that all the current in the emitter of Q2 does not flow into Q3. Use of a larger load resistor for transistor Q3 compensates for the

lower current so that the voltage swings on the two collectors have nearly the same magnitude.

The driver stages (transistors Q4 and Q5) are emitter-follower amplifiers which shift the voltage level between the collectors of the differential-amplifier transistors and the bases of the output transistors and provide the drive current required by the output transistors.

The power transistors (Q6 and Q7) are large, high-current devices capable of delivering peak currents greater than 0.25 ampere. The emitters are made available to facilitate various modes of operation or to permit the inclusion of emitter resistors for more complete stabilization of the idling current of the amplifier. Inclusion of such resistors also reduces distortion by introducing negative feedback, but reduces the power-output capability by limiting the available drive.

Inclusion of emitter resistors between terminals 5 and 6 and ground also enhances the effectiveness of the internal dc feedback supplied to the bases of transistors Q2 and Q3 through resistors R5 and R7. Any increase in the idling current in either output transistor is reflected as an increased voltage at its base. This change is coupled to the input through the appropriate resistor to correct for the increased current.

Operating Characteristics

The operating requirements and characteristics of the CA3020 and CA3020A are explained in the following paragraphs.

Supply Voltages and Derating— The CA3020 operates with any supply voltage between +3 and +9 volts. The CA3020A can also be operated with supply voltages up to +12 volts with inductive loads or +25 volts with resistive loads. Fig. 265 shows

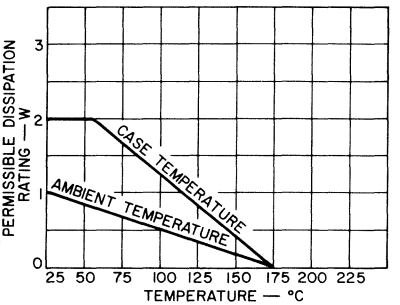


Fig. 265 — Dissipation rating of the CA3020 or CA3020A as a function of case and ambient temperatures.

the permissible dissipation rating of the CA3020 and CA3020A as a function of case and ambient temperatures. At supply voltages from +6 to +12 volts, a heat sink may be required for maximum power-output capability. The worst-case dissipation $P_{d_{max}}$ as a function of power output can be calculated as follows:

$$P_{dmax} = (V^+_1 I_{CC1} + V^+_2 I_{CC2}) + (V^+_2 / R_{CC})$$

where V^+_1 and V^+_2 are the supply voltages to the differential-amplifier and output-amplifier stages, respectively; I_{CC_1} and I_{CC_2} are the corresponding idling currents; and R_{CC} is the collector-to-collector load resistance of the output transformer. This equation is preferred to the conventional formula for the dissipation of a class B output transistor (i.e., 0.84 times the maximum power output) because the $P_{d_{max}}$ equation accounts for the device standby power and device variability.

Input-Resistance Options—The input signal may be applied to the CA3020 or CA3020A in either of two ways, as shown in Fig. 266. Typical input resistance is 700 ohms

for the configuration in Fig. 266(a), and 50,000 ohms for the configuration shown in Fig. 266(b).

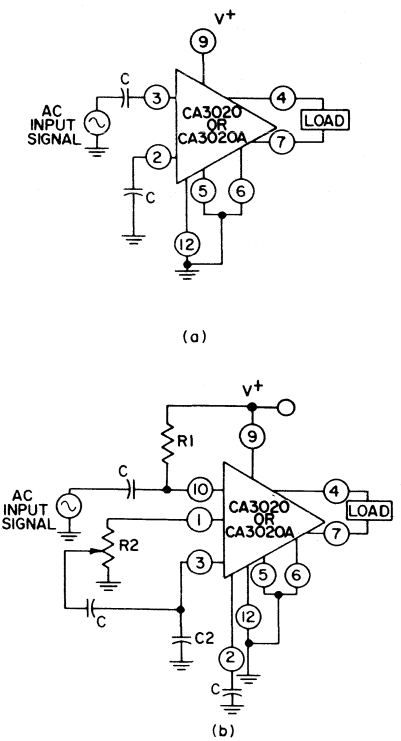


Fig. 266 — Input-impedance options for the CA3020 or CA3020A.

Squelch—The CA3020 and CA-3020A have an extremely flexible squelch capability. Two methods of squelch application are shown in Fig. 267. In method A, when the squelch voltage E_s is at zero, transistor Q_s is off. When E_s switches to a value of 1 volt or more (threshold is at a V_{BE} of about 0.7 volt), Q_s turns on, terminal 11 is clamped to 0.3 volt, and the differential amplifier is turned off. Method B operates in the same manner as method A except that the center-tap of R10 and R11 (terminal 8) is connected

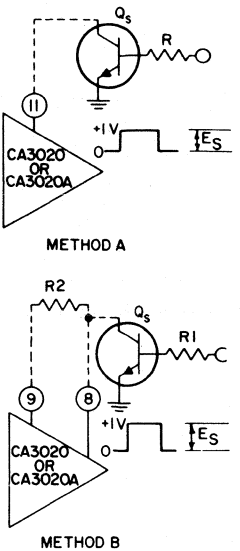


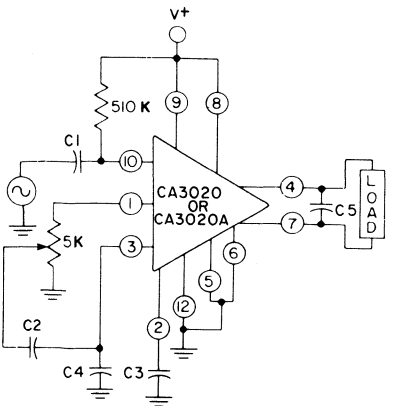
Fig. 267 — Methods of applying squelch to the CA3020 or CA3020A.

to the collector of Q_s. The resistor R2 is not necessary for squelching, but can be used to set the desired operating mode (idling current).

Frequency Shaping

In communication systems it is often necessary to restrict the bandwidth of the audio amplifier to minimize the effects of noise (particularly low-frequency noise) and other interfering signals outside the pass band. The CA3020 and CA3020A are wide-band amplifiers that have a relatively flat frequency response to approximately 6 MHz. Various methods can be used to roll off the high- and low-frequency response by means of the coupling capacitors and bypass capacitors shown in the feedback loop in Fig. 268.

Capacitors C1, C2, and C3 may be used for rolling off the low-frequency response. The low-frequency cutoff is determined by the time constants C1R10 and C2R3, where R10



All resistance values in ohms unless otherwise specified.

Fig. 268 — Methods of restricting the bandwidth of the CA3020 or CA3020A.

is the input resistance at terminal 10 (about 50,000 ohms) and R3 is the input resistance at terminal 3 (about 700 ohms).

Capacitors C4 and C5 are used for establishing the upper-frequency cutoff. The high-frequency roll-off is determined by the time constants C4R3 and $C5R_L$ where R_L is the load resistance.

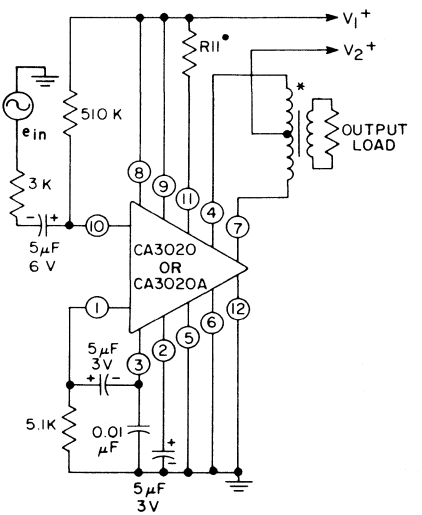
For a restricted bandwidth of 300 Hz to 3 kHz, the following capacitance values are recommended:

C1	0.02 μF
C2	1 μF
C3	2 μF
C4	0.1 μF
C5	0.2 μF

Audio Amplifiers

The CA3020 and the CA3020A integrated-circuits are well suited for use in audio-amplifier applications. These circuits may be used without transformers to drive a high-impedance speaker directly, or they may be used with power transformers to deliver power to a low-impedance speaker. They may also be used as transformer-coupled drivers for one or more power transistors to develop up to 10 watts of audio output power.

Basic Class B Amplifier—Fig. 269 shows a typical audio-amplifier circuit in which the CA3020 or



All resistance values in ohms unless otherwise specified.

Fig. 269 — Basic class B audio amplifier circuit using the CA3020 or CA3020A.

CA3020A can provide a power output of 0.5 or 1 watt, respectively. Table XXVIII shows performance data for both types in this amplifier. The circuit can be used at all voltage and power-output levels applicable to the CA3020 and CA3020A.

The emitter-follower stage at the input of the amplifier in Fig. 269 is used as a buffer amplifier to provide a high input impedance. Although many variations of biasing may be applied to this stage, the method shown is efficient and economical. The output of the buffer stage is ap-

Table XXVIII — *Typical Performance of CA3020 and CA3020A in Circuit of Fig. 269**

Characteristic	CA3020	CA3020A	
Power Supply — V^-_1	9	9	V
V^+_2	9	12	V
Zero-Signal Idling Current — I_{CC_1}	15	15	mA
I_{CC_2}	24	24	mA
Maximum-Signal Current — I_{CC_1}	16	16.6	mA
I_{CC_2}	125	140	mA
Maximum Power Output at 10% THD	550	1000	mW
Sensitivity	35	45	mV
Power Gain	75	75	dB
Input Resistance	55	55	kΩ
Efficiency	45	55	%
Signal-to-Noise Ratio	70	66	dB
% Total Harmonic Distortion at 150 mW	3.1	3.3	%
Test Signal	1000 Hz/600Ω generator		
Equivalent Collector-to-Collector Load	130	200	Ω
Idling-Current Adjust Resistor (R11)	1000	1000	Ω

* Integrated circuit mounted on a heat sink, Wakefield 209 Alum. or equiv.

plied to terminal 3 of the differential amplifier for proper balance of the push-pull drive to the output stages. Terminals 2 and 3 must be bypassed for approximately 1000 ohms at the desired low-frequency roll-off point.

At low power levels, the cross-over distortion of the class B amplifier can be high if the idling current is low. For low cross-over distortion, the idling current should be approximately 12 to 24 milliamperes, depending on the efficiency, idling dissipation, and distortion requirements of the particular application. The idling current may be increased by connection of a jumper between terminals 8 and 9. If higher levels of operating idling current are desired, a resistor (R11) may be used to increase the regulated voltage at terminal 11 by a slight amount with additional current injection from the power supply V^+_1.

In some applications, it may be desirable to use the input transistor Q1 of the CA3020 or CA3020A for other purposes than the basic buffer amplifier shown in Fig. 269. In such cases, the input ac signal can be applied directly to terminal 3.

The extended frequency range of the CA3020 and CA3020A requires that a high-frequency ac bypass capacitor be used at the input terminal 3. Otherwise, oscillation could occur at the stray resonant frequencies of the external components, particularly those of the transformers. Lead inductance may be sufficient to cause oscillation if long power-supply leads are not properly ac bypassed at the CA3020 or CA3020A common ground point. Even the bypassing shown may be insufficient unless good high-frequency construction practices are followed.

Fig. 270 shows typical power output of the CA3020A at supply voltages of +3, +6, +9, and +12 volts, and of the CA3020 at +6 and +9 volts, as measured in the basic class B amplifier circuit of Fig. 269. The CA3020A has higher power output for all voltage-supply conditions because of its higher peak-output-current capability.

Fig 271 shows total harmonic distortion (THD) as a function of

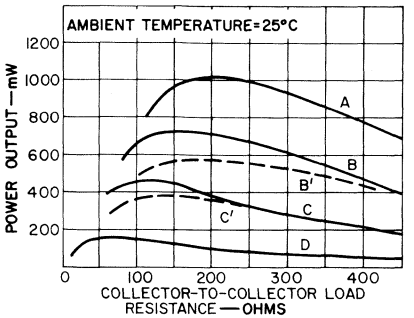


Fig. 270 — Power output of the CA3020 or CA3020A as a function of collector-to-collector load resistance R_{CC}.

power output for each of the voltage conditions shown in Fig. 270. The values of the collector-to-collector load resistance (R_{CC}) and the idling-current adjust resistor (R11) shown in the figure are given merely as a fixed reference; they are not necessarily optimum values. Higher idling-current drain may be desired for low cross-over distortion, or a higher value of R_{CC} may be used for better sensitivity with less power-output capability. Because the maximum power output occurs at the same conditions of peak-current limitations, the sensitivities at maximum power output for the curves of Figs. 270 and 271 are approximately the same.

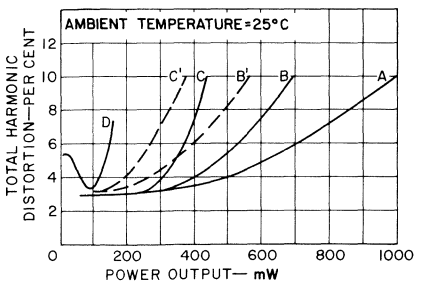


Fig. 271 — Total harmonic distortion of the CA3020 or CA3020A as a function of power output.

Increasing the idling-current drain by reducing the value of resistor R11 also improves the sensitivity.

Fig. 272 illustrates the improvement in cross-over distortion at low power levels. Distortion at 100 milliwatts is shown as a function of idling current I_{CC_2} (output stages only). There is a small improvement in total harmonic distortion for a large increase in idling current as the current level exceeds 15 milliamperes.

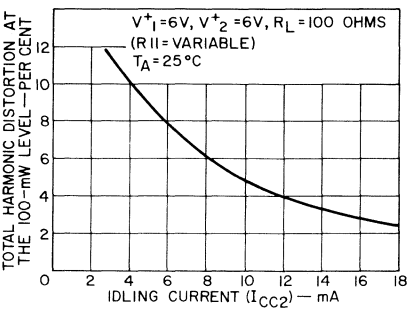
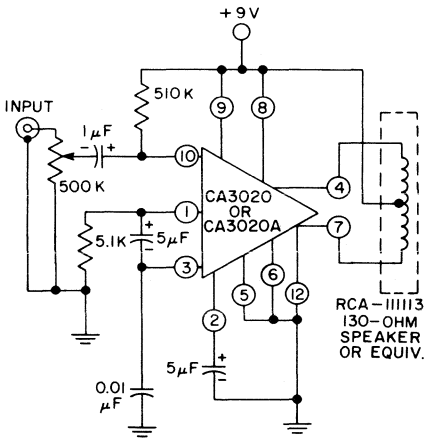


Fig. 272 — Total harmonic distortion as a function of idling current for a supply voltage of 6 volts and an output of 100 milliwatts.

Transformerless Audio Amplifier —The circuit shown in Fig. 269 may be used as a highly efficient class B audio power-output circuit in such applications as communications systems, AM or FM radios, tape recorders, phonographs, intercom sets, and linear mixers. Fig. 273 shows a modification of this circuit which may be used as a transformerless audio amplifier in any of these applications or in other portable instruments. The features of this circuit are a power-output capability of 310 milliwatts for an input of 45 millivolts and a high input impedance of 50,000 ohms. The idling-current drain of the circuit is 24 milliamperes. The curves of Fig. 270 may be used to determine the value of the center-tapped resistive load required for a



All resistance values in ohms unless otherwise specified.

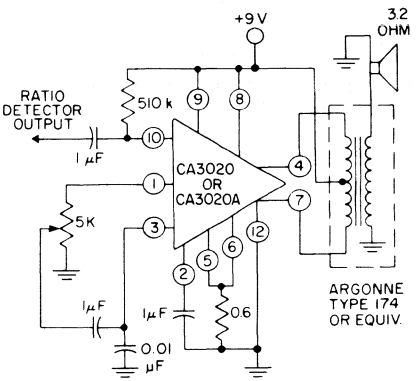
Fig. 273 — 310-milliwatt audio amplifier without transformers.

specified power-output level (the indicated load resistance is divided by two).

The CA3020 or CA3020A provides several advantages when used as a sound output stage or as a preamplifier-driver in communications equipment because each type is a compact and low-power drain circuit. The squelching requirement in such applications is simple and economical.

545-Milliwatt Amplifier Driving a Low-Impedance Speaker—Fig. 274 shows a circuit configuration that has the required characteristics for driving a conventional low-impedance speaker. The circuit shown uses a transformer capable of driving a 3.2-ohm speaker; other transformers may be used to drive 8-ohm and 16-ohm speakers. This circuit has the following characteristics:

Input voltage for full power output .....45 mV
Maximum power output .....545 mV
Idling current .....22 mA
Input resistance .....50,000 ohms
Total harmonic distortion at P_{out} = 135 mW3.3%
Signal-to-noise ratio (input voltage reference of 20 mV) .....77 dB

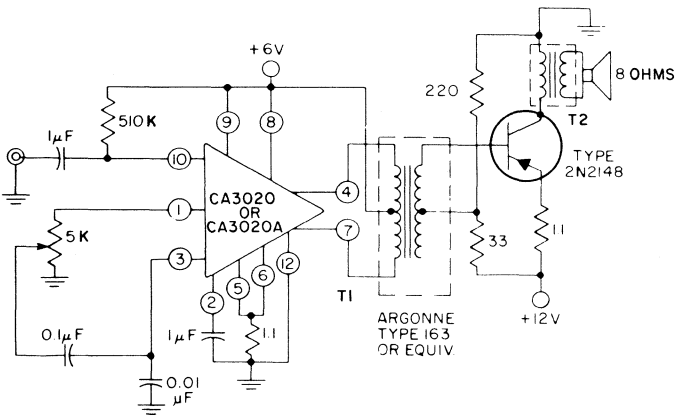


All resistance values in ohms unless otherwise specified.

Fig. 274 — 545-milliwatt amplifier driving a low-impedance speaker.

4-Watt Class A Audio Amplifier—Fig. 275 shows a class A audio amplifier in which the CA3020 or CA3020A is used with a driver transformer, a 2N2148 power transistor, and an output transformer. This circuit can deliver a power output of 4 watts to an 8-ohm speaker for an input voltage of 18 millivolts, or 0.45 watt for an input of 5.5 millivolts.

7-Watt Single-Ended Class B Audio Amplifier—Fig. 276 shows a class B audio amplifier in which the CA3020 or CA3020A is used with a driver transformer and two 2N2869 power transistors in a single-ended output stage. With an input voltage of 14.2 millivolts, this circuit has an idling current of 350 milliamperes and can deliver an output of 7 watts to the 2.5-ohm speaker.

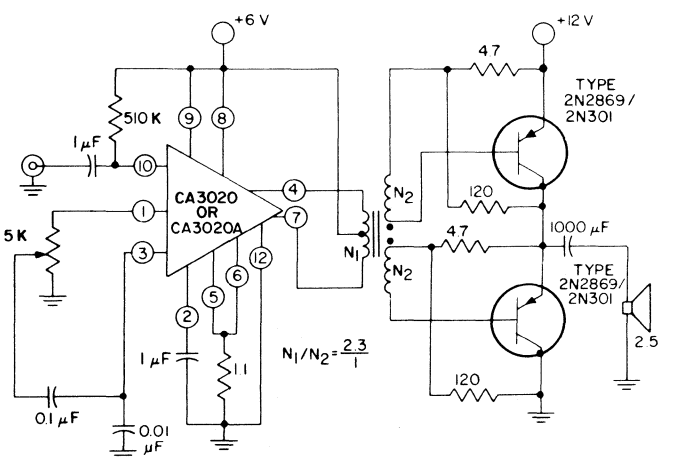


All resistance values in ohms unless otherwise specified.

Fig. 275 — 4-watt audio amplifier.

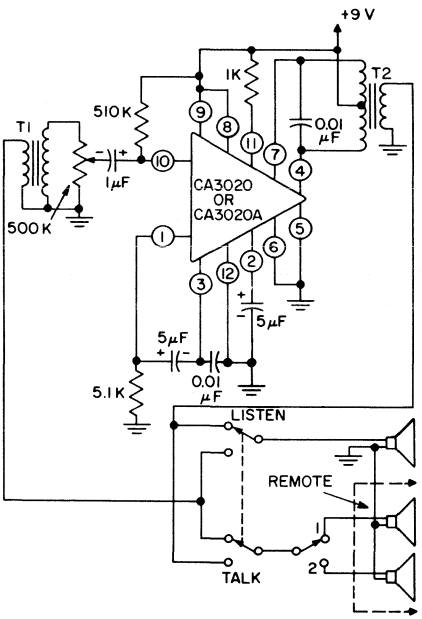
Intercom—Fig. 277 illustrates the use of the audio amplifier shown in Fig. 269 in an intercom in which a listen-talk position switch controls two or more remote positions. Only the speakers, the switch, and the input transformer are added to the basic audio amplifier circuit. A suitable power supply for the intercom could be a 9-volt battery used intermittently rather than continuously.

Driver Amplifiers—The high power-gain and power-output capabilities of the CA3020 and the CA3020A make these integrated circuits highly suitable for use as drivers for higher-power stages. In most ap-



All resistance values in ohms unless otherwise specified.

Fig. 276 — 7-watt class B single-ended audio amplifier.



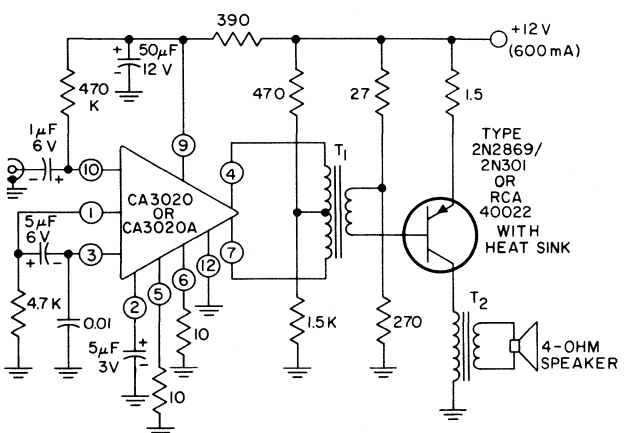
All resistance values in ohms unless otherwise specified.

Fig. 277 — Intercom using CA3020 or CA3020A.

plications, the full power-output capability of the circuit is not required, and large emitter resistors may be used in the output stage to reduce distortion. The CA3020 and CA3020A can drive any transformer-coupled load within their respective ratings. Several examples of typical applications are given below.

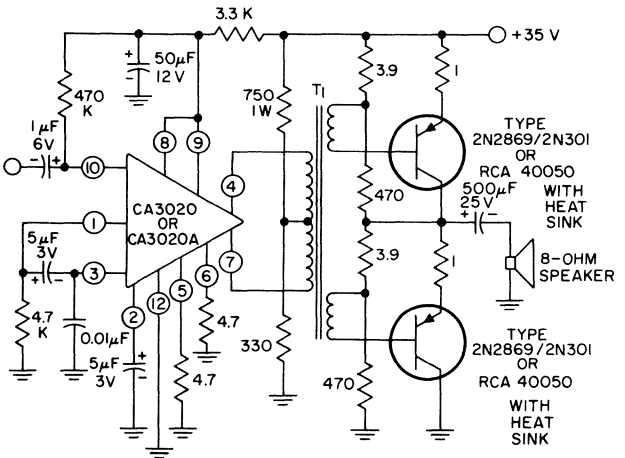
Fig. 278 illustrates the use of the CA3020 or CA3020A to drive a germanium power-output transistor to a 2.5-watt level. Because the integrated circuit is required to deliver a maximum power output of less than 50 milliwatts, an unbypassed emitter resistor can be used in the output stage to reduce distortion. Sensitivity for an output of 2.5 watts is 3 millivolts; this figure can be improved at a slight increase in distortion by reduction of the 10-ohm resistors between terminals 5 and 6 and ground.

Because so little of the power-output capability of the CA3020 or CA3020A is used, higher-power class B stages can easily be accommodated by selection of suitable output transistors and appropriate transformers.



All resistance values in ohms unless otherwise specified.

Fig. 278 — 2.5-watt class A audio amplifier using the CA3020 or CA3020A as a driver amplifier.



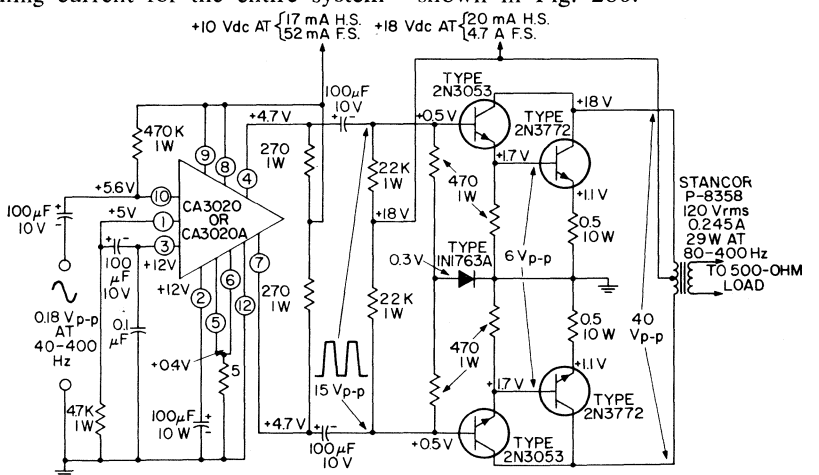
T1 = Thordarson Type TR-454 or equiv.

All resistance values in ohms unless otherwise specified.

Fig. 279 — 10-watt single-ended class B audio amplifier using the CA3020 or CA3020A as a driver amplifier.

Fig. 279 shows a medium-power class B audio amplifier in which the CA3020 or CA3020A is used as a driver. The output stage uses a pair of TO-3-style germanium output transistors which must be mounted on a heat sink for reliable operation. Idling current for the entire system is 70 milliamperes from the 35-volt supply. Sensitivity is 10 millivolts for an output of 10 watts.

Motor Controller and Servo Amplifier—The CA3020 or CA3020A may be used as a 40-to-400-Hz motor controller and servo amplifier, as shown in Fig. 280.



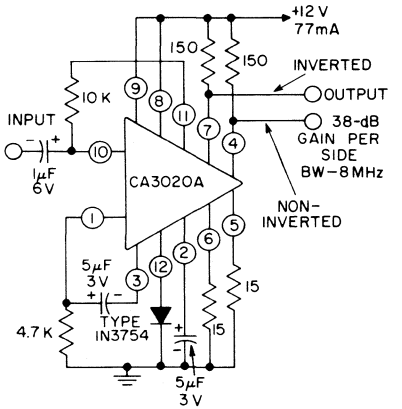
All resistance values in ohms unless otherwise specified.

Fig. 280 — Motor controller and servo amplifier using CA3020 or CA3020A.

Wide-Band Amplifiers

A major general-purpose application of the CA3020 and CA3020A is to provide high gain and wide-band amplification. The CA3020 and CA3020A have typically flat gain-bandwidth response to 8 MHz. Although the circuits are normally biased for class B operation, only the output stages operate in this mode. If proper dc bias conditions are applied, the output stages may be operated as linear class A amplifiers.

Fig. 281 shows the recommended method for achieving an economical and stable class A bias. The differential amplifier portion of the CA3020A is placed at a potential

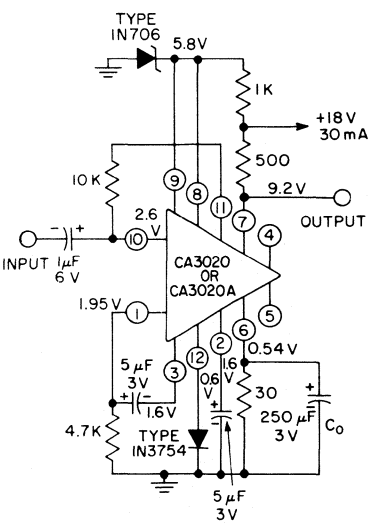


All resistance values in ohms unless otherwise specified.

Fig. 281 — Wide-band video amplifier illustrating economical and stable class A bias of CA3020A.

above ground equal to the base-to-emitter voltage V_{BE} of the integrated-circuit transistors (0.5 to 0.7 volt). In this condition, the output stages have an emitter-current bias approximately equal to the base-to-emitter voltage divided by the emitter-to-ground resistance. The circuit in Fig. 281 is a wide-band video amplifier that provides a gain of 38 dB at each of the push-pull outputs, or 44 dB in a balanced-output connection. The 3-dB bandwidth of the circuit is 30 Hz to 8 MHz. Higher gain-bandwidth performance can be achieved if the diode-to-ground voltage drop at terminal 12 is reduced. The lower voltage drop permits the use of a higher ratio of output-stage collector-to-emitter resistors without departure from the desired portion of the class A load line. It is important to note that the temperature coefficient of the terminal-12-to-ground reference element should be sufficiently low to prevent a large change in the current of the output stages.

The same method for achieving class A bias is used in the large-signal-swing output amplifier shown in Fig. 282. Either the CA3020 or the CA3020A may be used in this circuit with power supplies below +18 volts; the CA3020A can also be used with



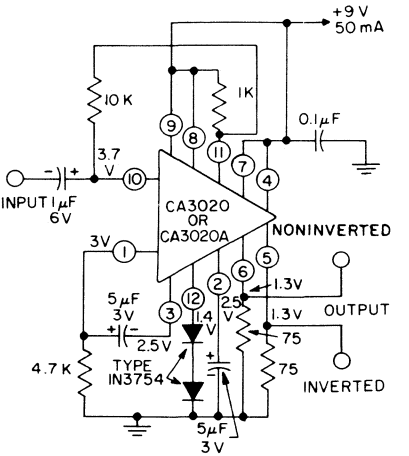
All resistance values in ohms unless otherwise specified.

Fig. 282 — Large-signal-swing output amplifier using CA3020 or CA3020A.

supply voltages up to 25 volts with noninductive loads. The circuit of Fig. 282 provides a gain of 60 dB and a bandwidth of 3.2 MHz if the output transistor Q7 has a bypassed emitter resistor. With an unbypassed output emitter resistor, the gain is 40 dB and the bandwidth is 8 MHz. The output stage can deliver a 5-volt-rms signal when a supply of +18 volts is used. For better performance in this type of circuit, the input signal is coupled from the buffer amplifier Q1 to the input terminal 3 of the differential amplifier. This arrangement provides higher gain because the collector resistor of the differential-amplifier transistor Q3 is larger than that of Q2. (This difference results from a requirement of differential drive balance that is not used in this circuit.) In addition, the terminals of the unused output transistor Q6 help to form an isolating shield between the input at terminal 3 and the output at terminal 7. This cascade of amplifiers has a single phase inversion at the output for much better stability than could be achieved if terminal 4 were used as the output and terminal 3 as the input.

Fig. 283 illustrates the use of the CA3020 or CA3020A as a class A linear amplifier. This circuit features a very low output impedance and may be used as a line-driver amplifier for wide-band applications up to 8 MHz. The circuit requires a 0.12-volt peak-to-peak input for a single-ended output of 1 volt or a balanced peak-to-peak output of 2 volts from a 3-ohm output impedance at each emitter. The input impedance is specified as 7800 ohms, but is primarily a function of the external 10,000-ohm resistor that provides bias to Q1 from the regulating terminal 11.

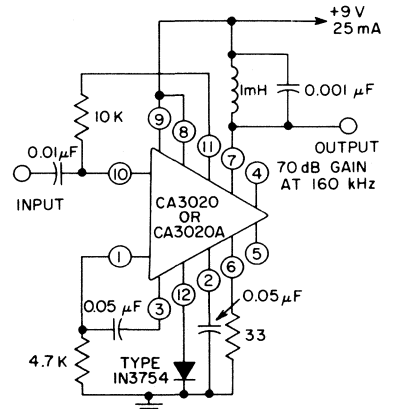
Fig. 284 illustrates the practical use of the CA3020 or CA3020A as



All resistance values in ohms unless otherwise specified.

Fig. 283 — Class A linear amplifier using CA3020 or CA3020A.

a tuned amplifier. This circuit uses dc biasing similar to that shown previously, and has a gain of 70 dB at a frequency of 160 kHz. The CA3020 or CA3020A can be used as a tuned rf amplifier or oscillator at frequencies well beyond the 8-MHz bandwidth of the basic circuit.



All resistance values in ohms unless otherwise specified.

Fig. 284 — 160-kHz tuned amplifier using the CA3020 or CA3020A.

Special-Purpose Circuits

The RCA integrated-circuit product line includes a number of types that are essentially subsystems designed to replace several discrete-component stages in specific types of applications. Such circuits are designed to provide multiple functions in specialized applications. Some typical uses of the special-purpose subsystem circuits are as follows:

- Television and FM if amplifiers
- Automatic-fine-tuning systems
- Audio amplifiers
- Voltage regulators
- Photodetector-and-power-amplifier circuit
- Power-control circuits

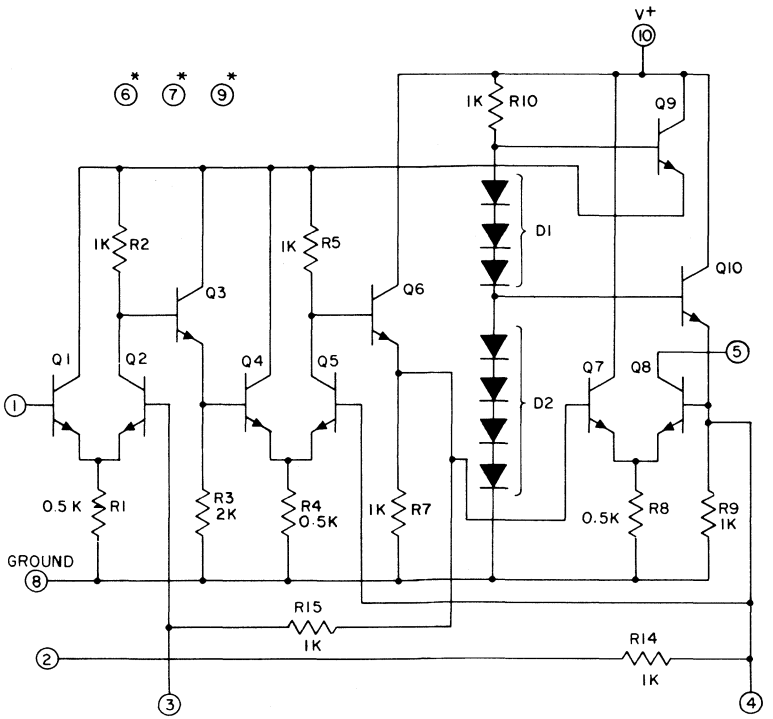
FM IF AMPLIFIERS

The RCA CA3011, CA3012, and CA3043 integrated circuits are designed especially for use in the if section of FM broadcast and communications receivers. The CA3011 and CA3012 are basically wide-band amplifier-limiter circuits intended for use with external FM detectors. The CA3043, however, can provide high-gain if amplification, noise limiting, FM detection, and low-level audio amplification in FM receivers without the use of external components other than tuned coupling networks and bypass elements.

Wide-Band Amplifier-Limiters

The CA3011 and CA3012 integrated-circuit wide-band amplifier-limiters are supplied in 10-terminal TO-5-style packages and operate over the temperature range of −55°C to +125°C. The two circuits have identical circuit configurations, but the CA3012 is capable of operation at higher supply voltages.

Circuit Description—Fig. 285 shows the schematic diagram of the CA3011 and CA3012 circuits. Each circuit consists of three direct-coupled cascaded differential-amplifier stages and a built-in regulated power supply. Each of the cascaded stages consists of an emitter-coupled amplifier and an emitter follower. The operating conditions are selected so that the dc voltage at the output of each stage is identical to that at the input to the stage. This condition is achieved by operation of the bases of the emitter-coupled differential pair of transistors at one-half the supply voltage and selection of the value of the common-emitter load resistor to be one-half that of the



* INTERNAL CONNECTION - DO NOT USE

All resistance values in ohms unless otherwise specified.

Fig. 285 — CA3011 or CA3012 integrated-circuit wide-band amplifier.

collector load resistor. As a result, the voltage drops across the emitter and collector load resistors are equal, and the collector of the emitter-coupled stage operates at a voltage equal to one V_{BE} plus the common-base potential. The potential at the output of the emitter follower, therefore, is the same as the common-base potential.

Operating Characteristics—The CA3011 is designed to operate at various levels of dc supply voltage up to 7.5 volts. The CA3012, which has higher supply-voltage and dissipation ratings, may be operated at dc supply voltages up to 10 volts. For each circuit, the external dc voltage is applied to terminals 10 and 5; dc voltages required at other terminals are derived from the internal power supply. When the circuits are operated at the same dc levels, the characteristics of their amplifier-limiter stages are identical. For operation at 7.5 volts with an ac resistive load impedance of 3000 ohms from terminal 5 to ground, the output voltage at terminal 5 with respect to ground is typically 3 volts peak-to-peak. Figs. 286 through 290 show the significant characteristics of the FM-if amplifier integrated circuits.

The performance of the CA3011 and CA3012 integrated circuits in

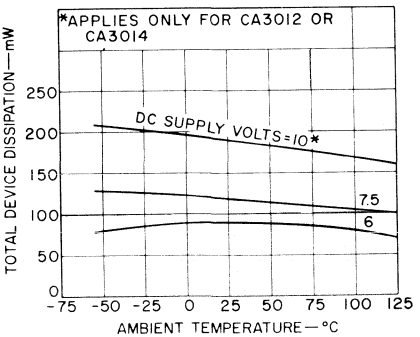


Fig. 286 — Total dissipation as a function of temperature.

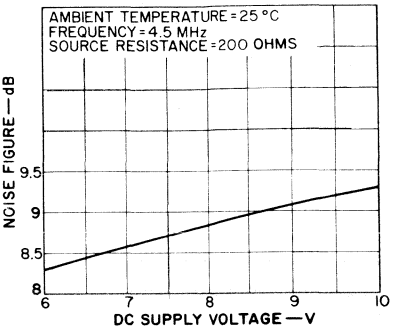
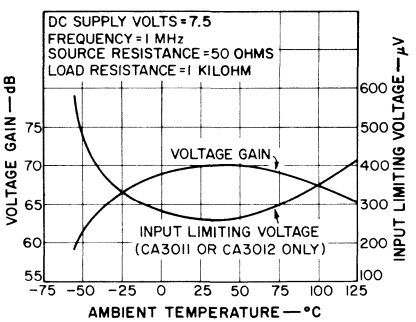


Fig. 287 — Noise figure as a function of dc supply voltage.



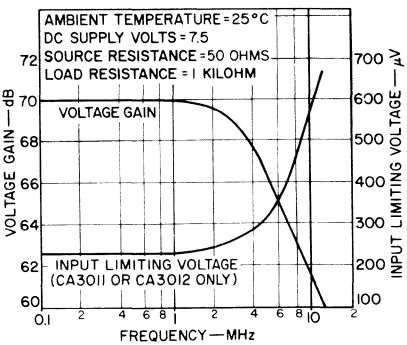
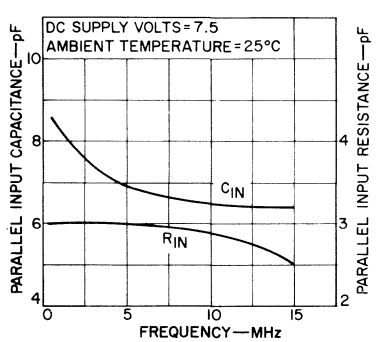


Fig. 288 — Voltage gain and input limiting voltage as a function of temperature and of frequency.



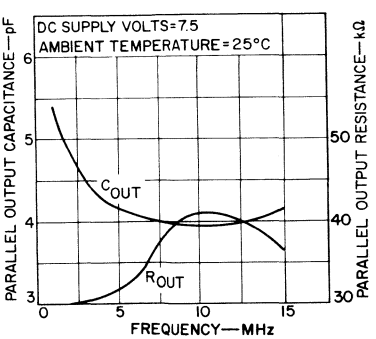


Fig. 289 — Input and output impedance as a function of frequency.

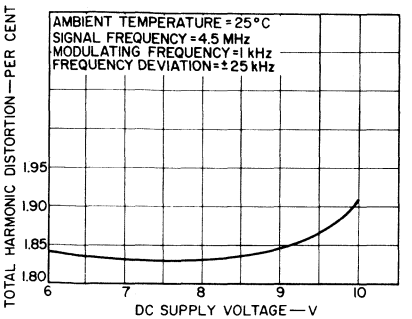


Fig. 290 — Total harmonic distortion as a function of dc supply voltage.

the if amplifier-limiter section of FM radio receivers is at least equal to that of conventional circuits in every characteristic, and is superior in many of them. In particular, the AM rejection ratio (more than 50 dB) of the integrated circuits is so large that it cannot be measured with commercial FM-AM signal generators because of incidental phase modulation of the generators. Fig. 291 shows the use of the CA3011 or CA3012 wide-band amplifier in the 10.7-MHz if-amplifier channel of an FM broadcast receiver.

CA3012 FM IF Strip—Fig. 292 shows the use of two CA3012 units in a 10.7-MHz if-amplifier strip. At an operating point 3 dB down from the knee of the transfer curve, the CA3012 requires an input between 400 and 600 microvolts, depending on the ratio-detector design. A double-tuned filter that has a voltage insertion loss of 8 dB is located between the two CA3012 units to provide a filter input of approximately 1000 microvolts (at terminal 5 of the first CA3012). For an if-strip sensitivity of 4 microvolts, a gain of 48 dB is required. However, if the CA3012 has a load impedance of 1200 ohms, the available gain is 65 dB, or approximately 17 dB more than required. The extra gain is not wasted, but drives the second CA-3012 harder, causing it to limit so that its gain is reduced by approximately 17 dB.

Fig. 293 shows the selectivity of the double-tuned interstage filter. The 3-dB bandwidth is 200 kHz at an input of 10 microvolts and 240 kHz at inputs from 500 microvolts to 0.5 volt. The coefficient of critical

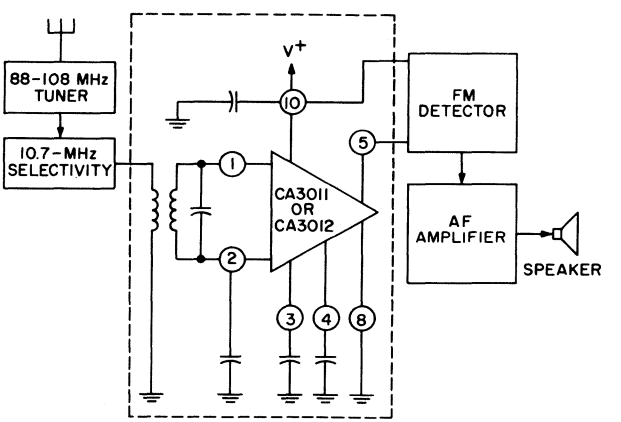
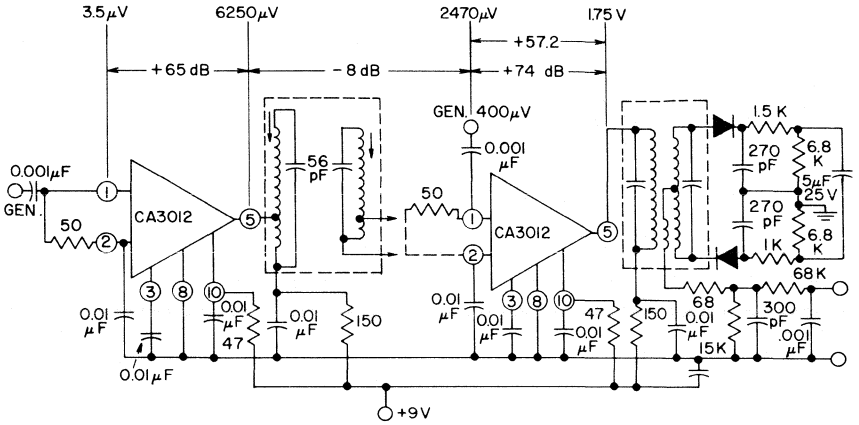


Fig. 291 — Block diagram of typical FM receiver using CA3011 or CA3012 integrated-circuit wide-band amplifier.



All resistance values in ohms unless otherwise specified.

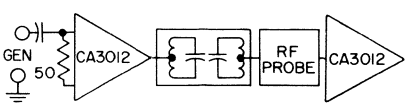
Fig. 292 — 10.7-MHz if-amplifier strip using CA3012 integrated circuit.

coupling is approximately 0.5 at 10 microvolts and increases to 1.0 but still maintains good phase response. The double-tuned filter should be coupled capacitance-aiding to avoid a nearly in-phase over-all relationship. Otherwise, bypassing of terminal 10 and the ratio-detector primary becomes critical, and over-all stability is impaired.

The connection of the FM front end to the integrated-circuit if strip must provide good selectivity and good phase response. A double-tuned filter is not suitable from the standpoint of selectivity. An actual IHFM* receiver selectivity between 35 and 40 dB is practical and does not impose too much burden on alignment. Because IHFM selectivity includes other factors than pass band, a combined filter design that provides second-channel attenuation between 52 and 60 dB becomes imperative.

Investigation of various types of inductance-capacitance filters indicates the use of a triple-tuned type to form the major lumped selectivity of the FM receiver. Fig. 294 shows the response curve and two configurations for such a filter. Economy and ease of alignment are the major features in this approach.

The triple-tuned filter, which is located between the mixer and the



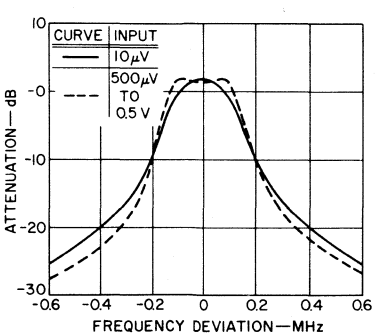
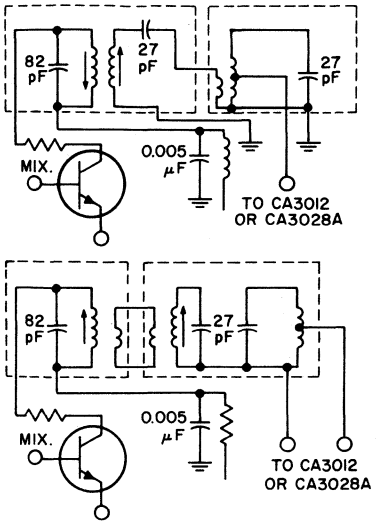


Fig. 293 — Selectivity curve for double-tuned interstage filter used in the if-amplifier strip shown in Fig. 292.

* Institute of High-Fidelity Manufacturers



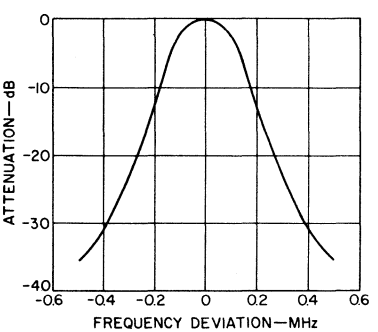


Fig. 294 — Configurations and response curve for triple-tuned interstage filter.

first integrated circuit, may have a voltage insertion loss of 33 dB, depending on the desired gain distribution. The power insertion loss of the filter, which is between 12 and 17 dB, is the loss that contributes to if noise. If the primary impedance is reduced to provide a lower voltage insertion loss, the front-end gain is decreased by a corresponding amount. Stability criteria must be the deciding factor in impedance and gain distribution.

Most FM front ends come equipped with a double-tuned 10.7-MHz if transformer in which a secondary high-impedance winding is brought out capacitively unterminated and nonpolarized with respect to ground. This configuration does not lend itself readily to optimum skirt selectivity (form factor) when connected with an additional single-tuned transformer to form a triple-tuned filter. Most effective use of the existing front-end filter is accomplished by the addition of another double-tuned filter, such as those shown in Fig. 295. Either bottom inductance or capacitance coupling can be used. Voltage insertion

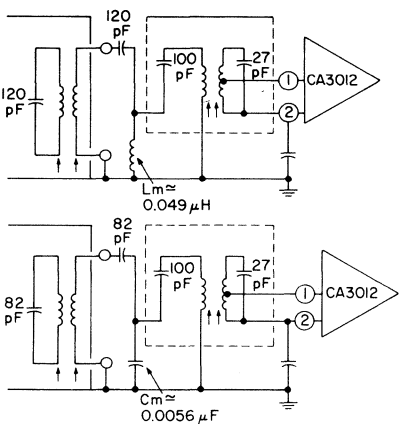
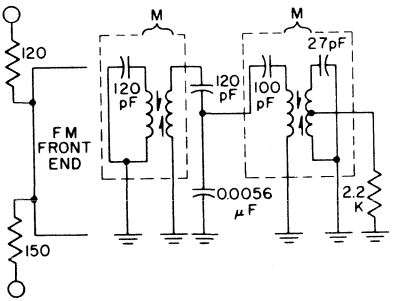


Fig. 295 — Configurations of two quadruple-tuned interstage filters.

losses from 18 dB to 26 dB can be expected. Fig. 296 shows the response curve obtained with a quadruple-tuned interstage filter. The per-cent coupling between filters and the coupling mode must be determined on the basis of over-all stability and performance.

It may be appropriate to consider briefly the noise associated with high-insertion-loss filters. Over-all re-



All resistance values in ohms unless otherwise specified.

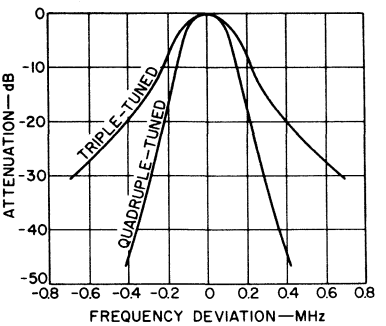


Fig. 296 — Response curve obtained with quadruple-tuned filter.

ceiver noise figure F is calculated as follows:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2}$$

where F_1, F_2, and F_3 are the noise figures of the first (rf), second (mixer), and third (if) stages, respectively; and G_1 and G_2 are the power gains of the first and second stages. If a value of 27 dB is assumed for the if noise figure F_3 (filter plus integrated circuit), 10 dB for the mixer noise figure, and 30 dB for mixer power gain, the effect of if noise on mixer noise is determined as follows:

$$F_2' = F_2 + \frac{F_3 - 1}{G_2}$$

$$= 10 + \frac{27 - 1}{1000} = 10.026 \text{ dB}$$

If the rf stage is assumed to have a power gain of 15 dB and a noise figure of 5 dB, total receiver noise is then determined as follows:

$$F = F_1 + \frac{F_2' - 1}{G_1}$$

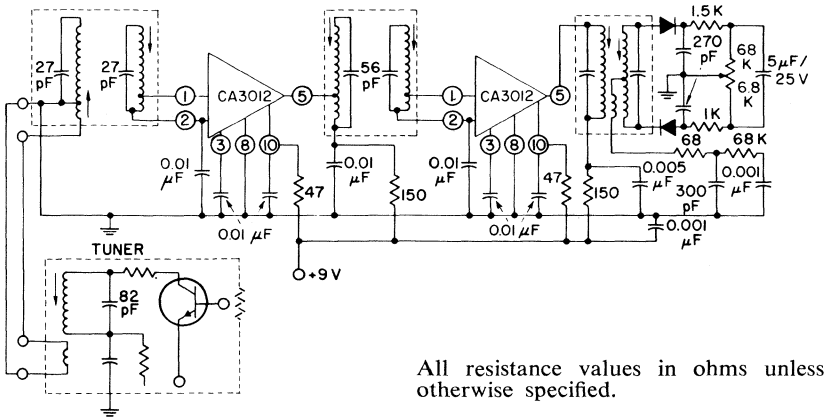
$$= 5 + \frac{10.87 - 1}{31.7} = 5.285 \text{ dB}$$

These calculations show that the power gain of the rf-amplifier stage overrides both if noise and mixer noise. A minimum power gain of 10 dB is advisable.

The use of a tuning capacitance of 82 picofarads in the collector circuit of the mixer stage provides a loaded primary impedance of approximately 10,000 ohms and eliminates the need for a tap. The 27-picofarad tuning capacitances that comprise the other poles of this filter could be reduced to obtain more favorable loaded-to-unloaded-Q ratios without use of additional resistor loading. The choice of 27 picofarads is based primarily on circuit stability considerations.

Fig. 297 shows one type of complete integrated-circuit if strip, and Fig. 298 shows the accompanying voltage gains and impedances. Values are given for two levels of mixer output impedance. All other impedance levels shown have exhibited good stability. Over-all performance of the circuit is illustrated in Fig. 299.

Capture ratio, which was measured at various levels, varies from 5 dB at 2 microvolts to 1.2 dB above 500 microvolts. With careful adjustment, values as low as 0.8 dB can be obtained. The selectivity curve for the integrated-circuit if strip is shown in



All resistance values in ohms unless otherwise specified.

Fig. 297 — Complete 10.7-MHz if-amplifier strip using two CA3012 integrated circuits.

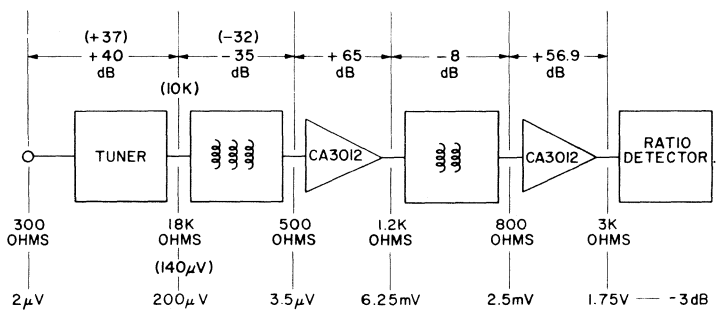


Fig. 298 — Voltage gain and impedance values for if-amplifier strip shown in Fig. 297.

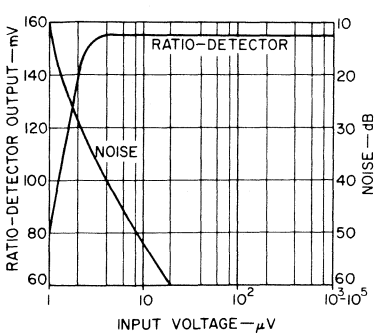


Fig. 299 — Performance curves for if-amplifier strip shown in Fig. 297.

Fig. 300. Over-all selectivity for a given ratio detector and the if strip is shown in Fig. 301. Some distributed-selectivity receivers have very little second-channel selectivity at an antenna input of 2000 microvolts. The points marked in Fig. 301 show such selectivity for several antenna input levels.

Fig. 302 shows an if strip that combines high gain per package and the single-stage-per-package approach. CA3012 and CA3028 integrated circuits are used in a differential-mode connection. An if

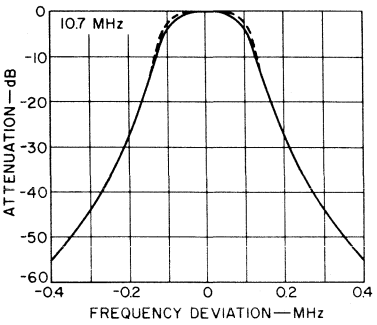


Fig. 300 — Selectivity curve for if-amplifier strip shown in Fig. 297.

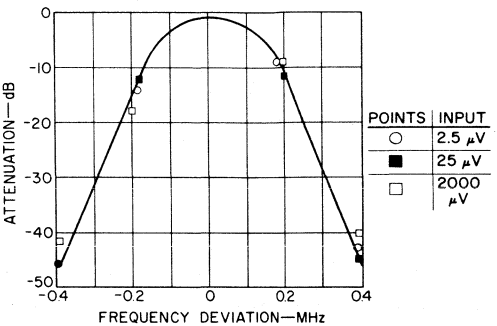
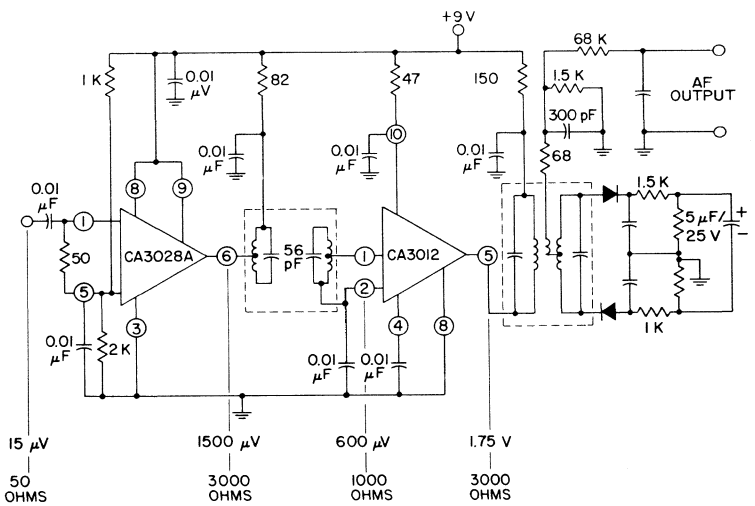


Fig. 301 — Measured over-all selectivity curve for if-amplifier strip shown in Fig. 297.



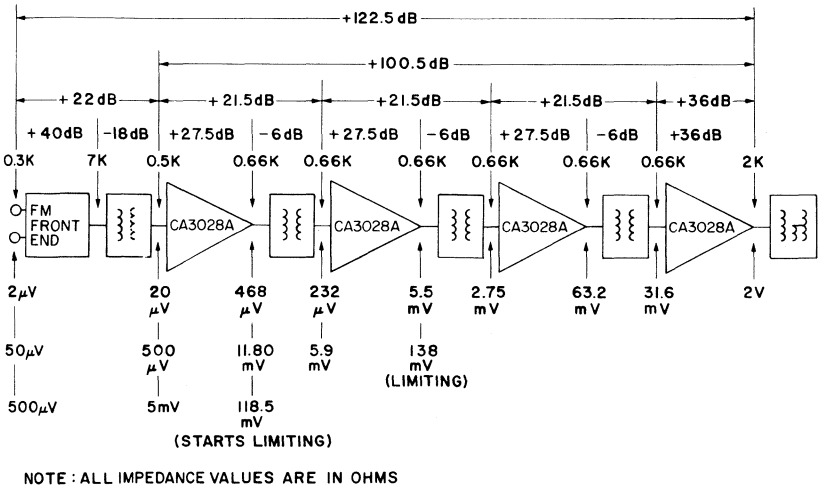
All resistance values in ohms unless otherwise specified.

Fig. 302 — IF-amplifier strip using CA3028A and CA3012 integrated circuits.

sensitivity of 15 microvolts can be obtained with this if strip.

If discrete circuits are directly replaced by single differential integrated-circuit amplifiers, a minimum of if-transformer and printed-circuit-board redesign is required. Values of voltage gain and impedance are indicated on the block diagram in Fig. 303. All three double-tuned transformers are made symmetrical with respect to primary and secondary windings and taps.

Because the single- or double-tuned circuit used between the mixer and the if strip has inherently less insertion loss than a triple-tuned input filter, the required input to this if strip is 20 microvolts, instead of 3.5 microvolts as required for the if strip shown in Fig. 297. All three double-tuned if transformers have an



NOTE : ALL IMPEDANCE VALUES ARE IN OHMS

Fig. 303 — Voltage gain and impedance values for if-amplifier strip shown in Fig. 302.

insertion loss of 6 dB and a 3-dB bandwidth of 280 to 300 kHz. The ratio-detector primary impedance dictates the stage gain of 36 dB for the last integrated circuit. Each of the remaining three stages has a gain of 21.5 dB, for the total required gain of 100 dB. The impedance required for the desired stage gain was calculated to be 660 ohms for both the primary and secondary windings of the if transformers.

With inputs from 20 to 200 microvolts, second-channel selectivity as high as 52 to 59 dB can be attained for three double-tuned and four double-tuned filters, respectively, for a 3-dB bandwidth of 196 kHz. For higher inputs, the same deterioration of selectivity occurs as that experienced with discrete circuits, as shown in Fig. 304.

Several receivers incorporating the if strips shown have been field-tested in areas of 200-kHz station separation, where a weak station was sandwiched between two strong stations. The weak station was received with-

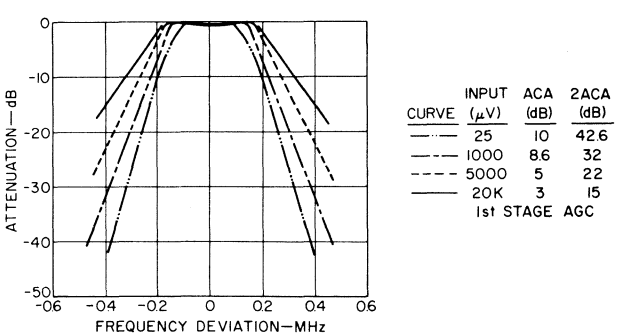


Fig. 304 — Selectivity curves for discrete-component if-amplifier strip using six double-tuned filters.

out interference, as compared to the performance of other high-quality FM receivers fabricated with discrete-component if circuits, in which lack of selectivity marred reception.

Amplifier-Limiter-Detector Circuit for FM Receivers

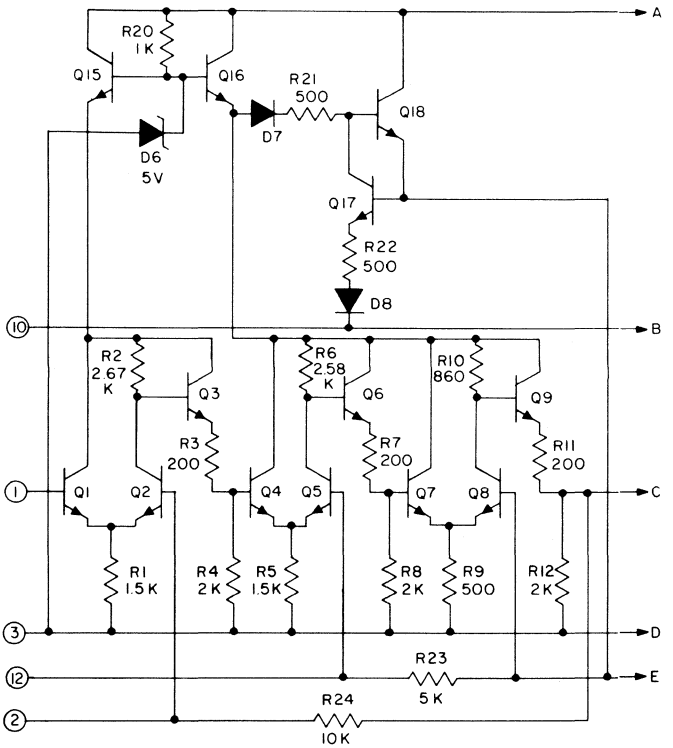
The CA3043 integrated circuit includes a high-gain if amplifier-limiter, an FM detector, an audio preamplifier-driver, and a zener-diode-regulated power supply on a single monolithic chip. This circuit is designed for use as a major subsystem for the if sections of communications and high-fidelity FM receivers. The CA3043 is supplied in a 12-terminal TO-5-style package and operates over a temperature range of −55°C to +125°C. Provision for independent use of the amplifier-limiter, FM detector, and audio preamplifier-driver sections makes possible exceptional versatility in circuit design.

Circuit Description—Fig. 305 shows the schematic diagram for the CA3043 subsystem. The four-stage emitter-coupled if amplifier-limiter section provides a voltage gain of 80 dB at 10.7 MHz. The output stage of this section provides exceptional limiting characteristics, which can be attributed to its use of a transistor constant-current source. The FM detector section is distinguished by circuitry which provides forward bias to the detector diodes, D2 and D3, and also provides a reference voltage for automatic frequency control (afc). The audio preamplifier-driver provides a low-impedance drive for subsequent audio amplifiers. The power-supply section provides zener-diode-regulated decoupled voltages for the if amplifier, detector, and audio-amplifier sections.

The CA3043 is designed to operate from a dc supply voltage of +30 volts applied to terminal 11 through a 750-ohm resistance. Terminal 11 may be connected to any positive voltage source through a suitable resistor provided the maximum dissipation limit or any of the maximum voltage or current limits for the circuit are not exceeded. Fig. 306 shows the limiting characteristics of the CA3043.

Experimental Receiver—An experimental receiver that uses only a commercial FM tuner, an LC filter, and an RCA CA3043 with a discriminator transformer is shown in Fig. 307. The 1½-by-⅞-by-⅝-inch LC filter was designed to operate with source and load impedances of 500 ohms. The output of the filter was terminated in a 470-ohm resistor connected between terminals 1 and 12 of the CA3043. Terminal 12 was bypassed to ground; and, because the output of the filter is dc-isolated, it was connected directly to terminal 1. At the tuner end, matching was accomplished by use of a capacitive tap on the transformer secondary winding to reduce the impedance to the 500-ohm level.

Performance data for the experimental receiver are given in Table XXIX. AM rejection is not included, but has been measured as approximately 58 dB. The 20-dB quieting sensitivity was measured at 2 microvolts at the antenna; 30-dB quieting sensitivity was measured at 3 microvolts. The 3-dB limiting sensitivity was reached at 7 microvolts. The selectivity curve for the receiver shows that the 60-dB rejection points are reached at 304 kHz from the desired frequency; the 3-dB bandwidth at small-signal levels is better than 220 kHz.



All resistance values in ohms unless otherwise specified.

Fig. 305 — CA3043 integrated-circuit high-gain amplifier-limiter FM detector, and audio preamplifier-driver for FM receivers.
(Continued on page 247)

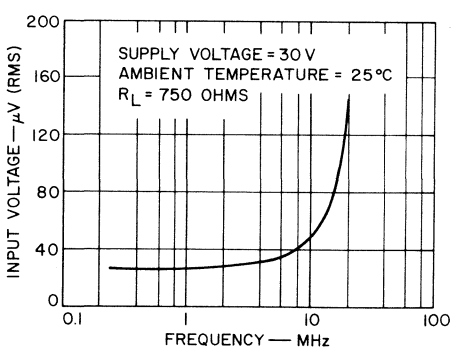


Fig. 306— Input limiting voltage (knee) at —3-dB point as a function of frequency.

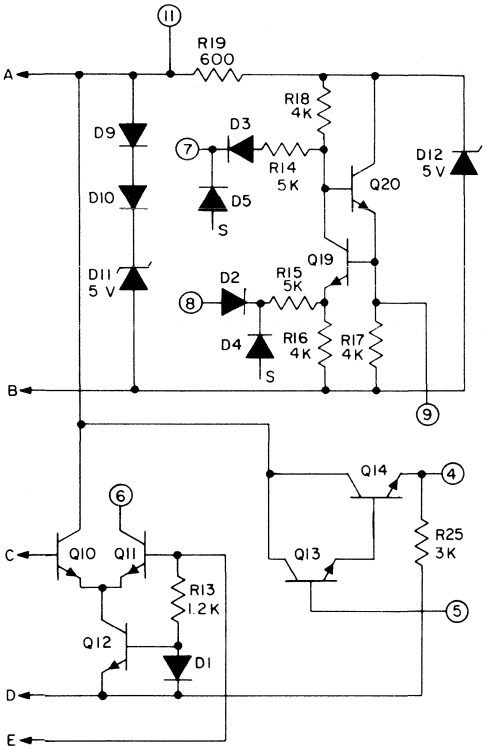
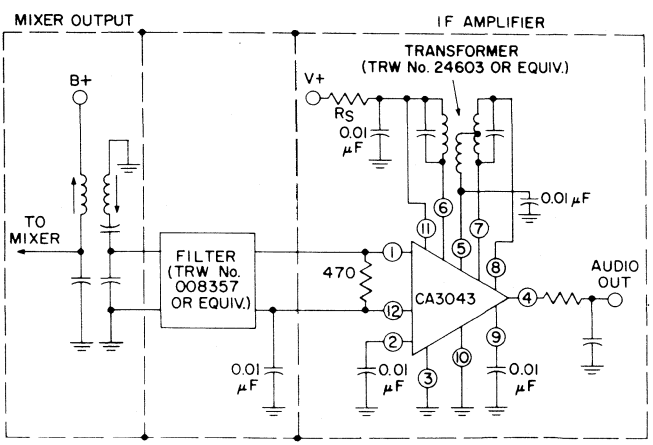


Fig. 305 — CA3043 integrated-circuit high-gain amplifier-limiter, FM detector, and audio preamplifier-driver for FM receivers.
(Continued from page 246)



All resistance values in ohms unless otherwise specified.

Fig. 307 — Experimental FM receiver using a commercial FM tuner, an LC filter, and a CA3043 with a discriminator transformer.

Table XXIX — *Performance Data for experimental Receiver shown in Fig. 307.*

Performance Data

20-dB quieting sensitivity = 2 μV
30-dB quieting sensitivity = 3 μV
3-dB limiting sensitivity = 7 μV
total harmonic distortion
225-μV input = 0.35%
10-μV input = 1.3%

Selectivity (tuner + filter)

3-dB bandwidth = 223 kHz
6-dB bandwidth = 305 kHz
20-dB bandwidth = 399 kHz
40-dB bandwidth = 486 kHz
60-dB bandwidth = 608 kHz

The high-gain integrated-circuit if amplifiers used in the experimental receiver are designed to operate without external feedback. Negative feedback can be used as a gain-control mechanism; however, positive feedback must be avoided if the amplifier is to remain free of spurious oscillations. The concentration of a high dynamic gain across a small input-output separation magnifies the problem of isolating the high-level output signals from the low-level input. In addition, direct coupling of several cascaded stages on the integrated circuit chip requires the use of a large amount of internal negative dc feedback. Careful bypassing of the feedback point must be provided externally to eliminate the effects of this feedback at the intermediate frequency. Accordingly, the design of if amplifiers using high-gain integrated circuits consists mainly of optimizing the printed-circuit-board layout and component connections to reduce external feedback, determining the source and load terminations for stability, and assuring effective bypassing of the internal negative feedback. For the CA3043, the load-source conductance product to assure stability is given as follows:

$$g_S g_L(\min) = 0.6 \times 10^{-6} \text{ (mhos)}^2$$

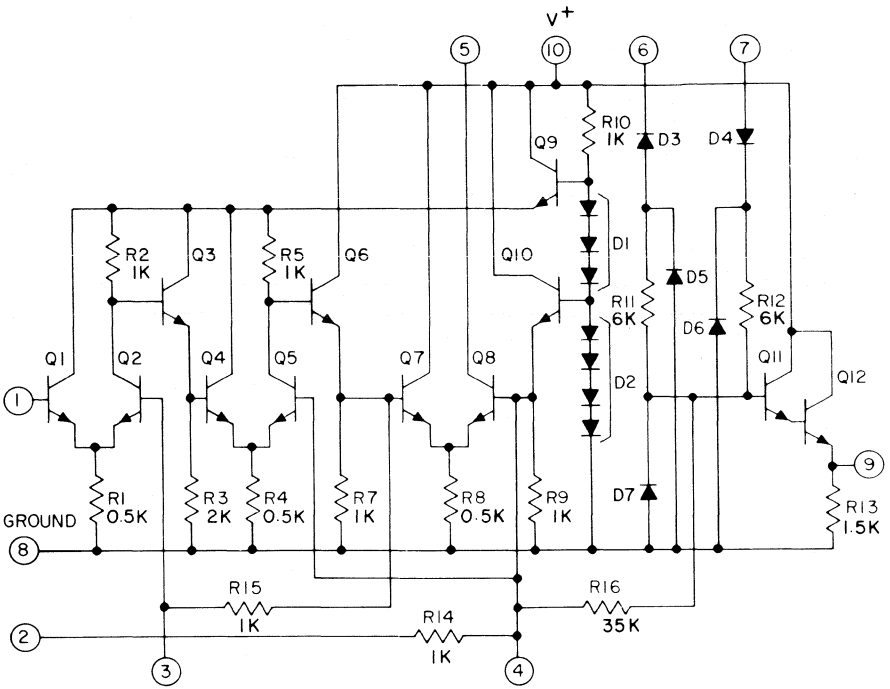
TELEVISION SOUND-SYSTEM CIRCUITS

RCA offers several multistage integrated circuits that provide essentially all the circuit functions required for the complete sound section of an intercarrier television receiver. The following paragraphs describe the basic features of these circuits and explain their application in the sound section of a television receiver.

CA3013 and CA3014 Integrated Circuits

The CA3013 and CA3014 integrated circuits can provide if amplification, noise limiting, FM detection, and low-level audio amplification in an FM receiver or the sound-if section of a television receiver without the use of external components other than tuned coupling networks and bypass elements. These circuits are supplied in a 10-terminal TO-5-style package and operate over the temperature range from −55°C to +125°C. The CA3013 and CA3014 are identical, except that the CA3014 has a higher dc voltage rating.

Circuit Description—Fig. 308 shows the schematic for the CA3013 or CA3014 amplifier-discriminator. Each amplifier-discriminator includes a three-stage, direct-coupled, amplifier-limiter cascade and regulated power supply identical to those in the CA3011 and CA3012 wideband amplifiers, together with an FM detector and a Darlington-pair low-level audio output stage, on the same silicon chip. The operation of the amplifier-limiter stages and the regulated power supply is identical to that of



All resistance values in ohms unless otherwise specified.

Fig. 308 — CA3013 or CA3014 integrated-circuit amplifier-discriminator.

the CA3011 or CA3012 wide-band amplifier-limiters.

The FM detector includes all the components required for FM demodulation except the tuned phase-shift transformer. In the design of the integrated detector, the large non-integrable diode load capacitors conventionally used to obtain peak rectification in balanced phase-shift discriminators and in ratio detectors are eliminated, and average detection is employed with a substantially resistive load. Filtering of the signal frequency and its harmonics is provided by the distributed capacitance of the load resistors; additional filtering is provided by the capacitance of the small reverse-biased diode junctions D5, D6, and D7. The parallel input resistance at the discriminator terminals 6 and 7 is typically 12,000 ohms; the parallel input capacitance at these terminals is typically 7 picofarads.

Operating Characteristics—The CA3013 is designed to operate at various levels of dc supply voltage up to 7.5 volts. The CA3014 may be operated at dc supply voltages up to 10 volts. For each circuit, the external dc voltage is applied to terminals 10 and 5; dc voltages required at other terminals are derived from the internal power supply. When the circuits are operated at the same dc levels, the characteristics of the amplifier-limiter stages of the CA3013 and CA3014 are identical to those of the CA3011 and CA3012 amplifier-limiters. The characteristics

data for the CA3011 and CA3012 FM-if amplifier integrated circuits shown in Figs. 286 through 290, therefore, are equally applicable to the amplifier-limiter stages of the CA3013 and CA3014. Fig. 309 shows the input limiting voltage (knee) and recovered audio-frequency voltage for operation of the CA3013 or CA3014 at 1.75, 4.5, and 10.7 MHz.

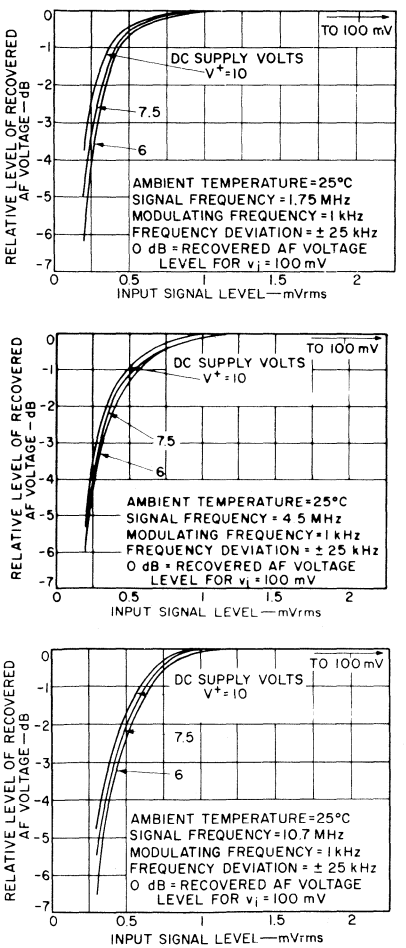


Fig. 309 — Input limiting voltage (knee) and recovered audio-frequency voltage for operation of amplifier-discriminator at 1.75, 4.5, and 10.7 MHz.

The block diagram in Fig. 310 shows the use of the CA3013 or CA3014 amplifier-discriminator in the sound channel of an intercarrier television receiver. (Details of the discriminator transformer shown in Fig. 310 are given in Fig. 311.)

CA3041 and CA3042 Integrated Circuits

The CA3041 and CA3042 comprise, on a single monolithic chip, a major subsystem for the sound section of television receivers. These integrated circuits are supplied in 14-terminal dual-in-line plastic packages and operate over the temperature range from 0°C to +85°C.

Circuit Descriptions—Figs. 312 and 313 show the schematic diagrams for the CA3041 and CA3042 integrated-circuit subsystems. Each type contains a wide-band three-stage if amplifier-limiter section, an FM detector stage, a zener-diode-regulated power supply, and an audio preamplifier-driver section. The audio preamplifier-driver section of the CA3041 is specifically designed to drive directly a 6AQ5 beam-power tube or other audio-output tube that has similar characteristics. The audio preamplifier-driver section of the CA3042 is designed to drive directly an n-p-n audio-output transistor or a high-gain audio-output pentode tube. With the exception of the audio-amplifier sections, the CA3041 and CA3042 integrated circuits are identical. Exceptional versatility of these circuits is made possible by the fact that the if amplifier-limiter section, the FM detector section, and the audio preamplifier-driver section can be wired, and used, independently.

Functionally, the CA3041 and CA3042 integrated circuits are very similar to the CA3013 and CA3014 integrated circuits. The power supply

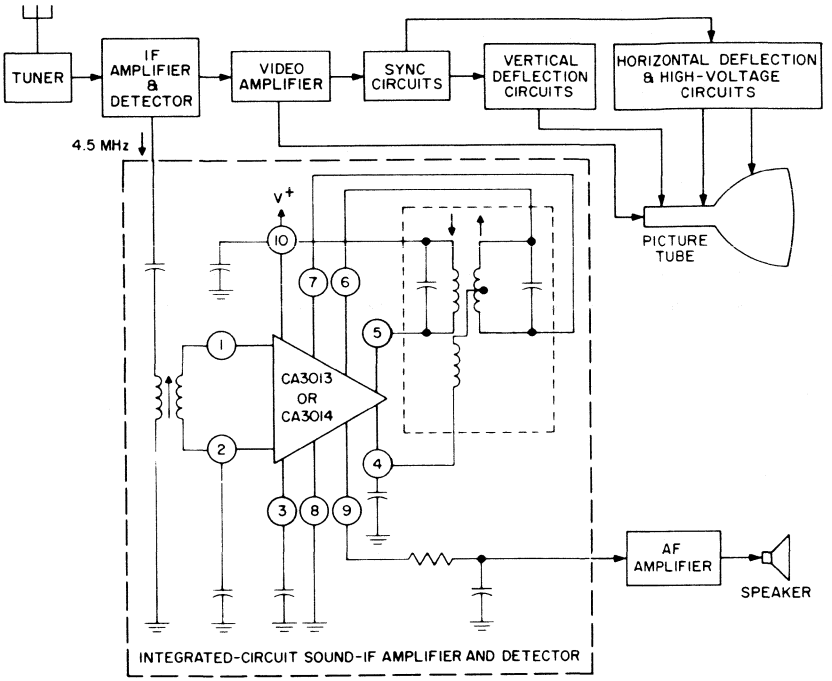


Fig. 310 — Block diagram of typical television receiver using a CA3013 or CA3014 integrated-circuit sound if amplifier and detector section.

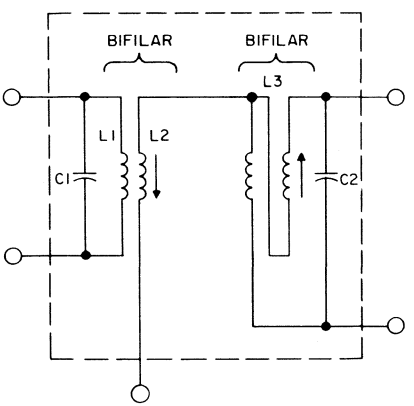
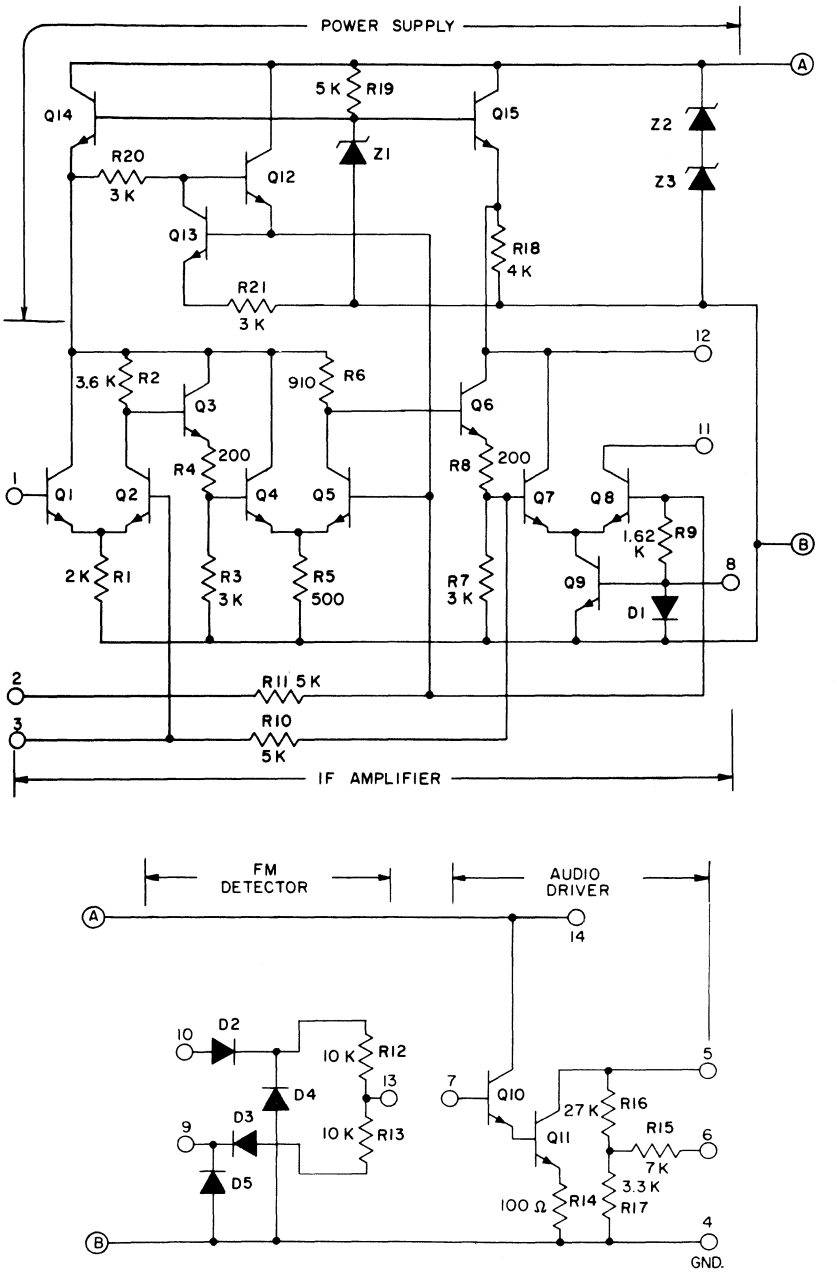
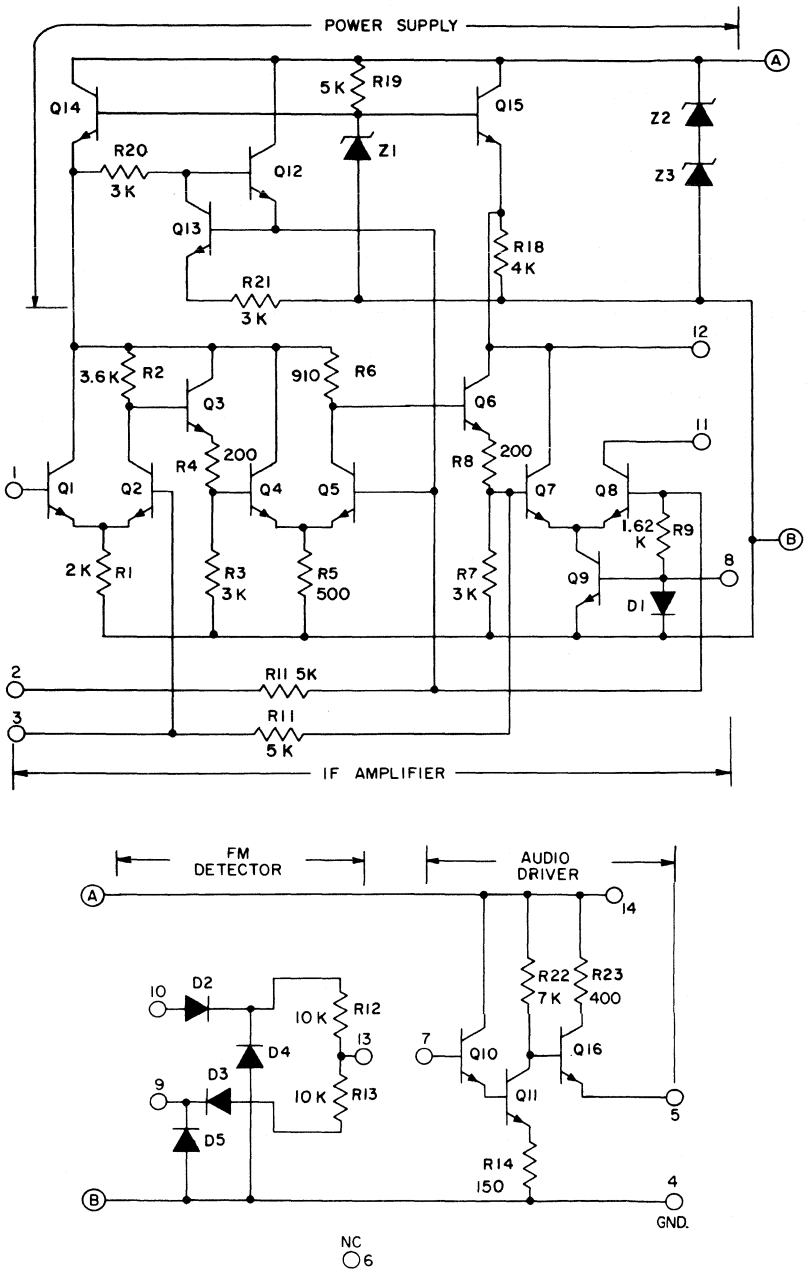


Fig. 311 — Details of the discriminator transformer shown in Fig. 310.



All resistance values in ohms unless otherwise specified.

Fig. 312 — CA3041 integrated-circuit if amplifier-limiter, FM detector, and audio amplifier.



All resistance values in ohms unless otherwise specified.

Fig. 313 — CA3042 integrated-circuit if amplifier-limiter, FM detector, and audio amplifier.

of the CA3041 and CA3042, however, provides zener-diode-regulated decoupled voltages for the if-amplifier, detector, and audio-amplifier sections. In addition, the use of a transistor constant-current source in the final if amplifier results in improved limiting characteristics for the CA3041 and CA3042.

Operating Characteristics—The CA3041 and CA3042 are designed to operate from a dc supply of +140 volts applied through a resistance of 6200 ohms to terminal 14. Other combinations of dc supply voltage and series resistance that will not cause the maximum dissipation limit or any of the maximum voltage or current limits for the CA3041 or CA3042 to be exceeded may also be used.

Fig. 314 shows typical dissipation characteristics for the CA3041 and CA3042. Figs. 315 and 316 show limiting and AM rejection characteristics of the two circuits. Figs. 317 and 318 show audio-amplifier characteristics for the CA3041 and CA3042, respectively.

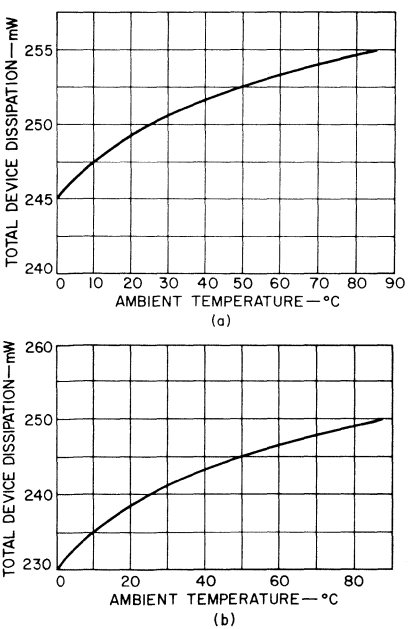


Fig. 314 — Typical dissipation characteristics for (a) the CA3041 and (b) the CA3042.

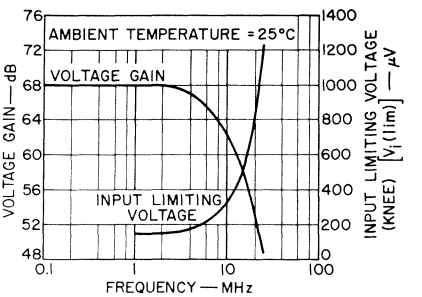


Fig. 315 — Typical IF-amplifier voltage-gain and input-limiting-voltage (knee) characteristics.

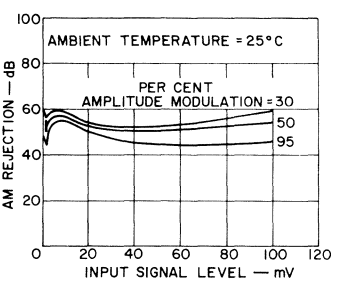


Fig. 316 — Typical AM rejection characteristics for CA3041.

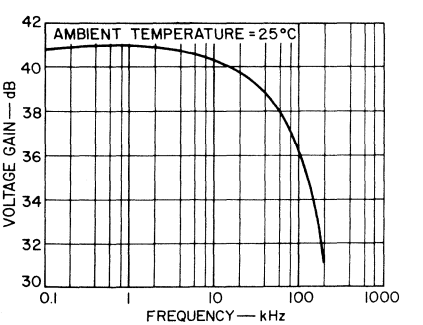


Fig. 317 — Typical af-driver voltage-gain characteristics for the CA3041.

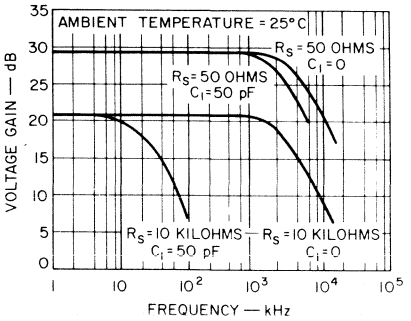


Fig. 318 — Typical af-amplifier voltage-gain characteristics for the CA3042.

Determination of Series Dropping Resistance—The shunt regulation provided by zener diodes Z2 and Z3 stabilizes circuit voltages, but may also cause wide variations in the dissipation on the integrated-circuit chip, depending upon power-supply and device variations. The external power supply for CA3041 and CA3042 integrated circuits, therefore, must be carefully designed to assure that the maximum dissipation rating of the integrated circuit is not exceeded, even under worst-case conditions, and that adequate voltage regulation is provided under all conditions.

The main variables to be considered in determination of the external series dropping resistors are as follows: (1) power-supply voltage and tolerance, (2) maximum allowable integrated-circuit dissipation at the maximum ambient temperature, and (3) variations in integrated-circuit characteristics.

When the CA3041 or CA3042 is operated at high power-supply voltages, the integrated-circuit dissipation does not vary widely; operation of the circuit at higher temperatures is then permitted. Under such conditions, however, total system dissipation is increased and a higher power rating is required for the series dropping resistor R_S. When low-voltage supplies are used, the power rating of the series resistor may be reduced, but a decrease in the temperature range of the integrated circuit also results.

The maximum value of the series dropping resistor R_S is the value for which a zener current of 1 milliampere is allowed to flow under worst-case conditions, i.e., under conditions of low line voltage, high zener voltage, and high integrated-circuit current drain. The minimum value of the resistor R_S is the value for which the worst-case dissipation is limited to that defined by the maximum ambient temperature and the circuit derating curve shown in Fig. 319.

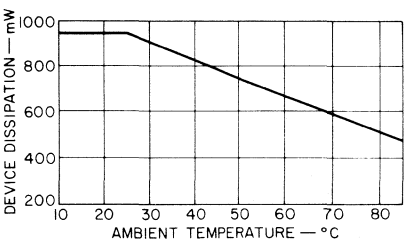


Fig. 319 — Maximum-device-dissipation derating curve for the CA3041 and CA3042 integrated circuits.

The procedure used to define the resistor R_S differs slightly for the two types of integrated circuits. A few additional steps are required for the CA3041 because the dissipation of this circuit is a function of the load resistor of the audio-amplifier stage (this resistor is not used in the CA3042). Tables XXX and XXXI outline the procedure used to determine the resistor R_S for the CA3042 and CA3041, respectively. The voltage-current curves for the CA3041 and CA3042 also differ because of the difference in the audio-amplifier stage of these circuits.

Table XXX — *Procedure for Finding the Series Dropping Resistor R_S for the CA3042*

(Points referred to in the procedure are shown on Fig. 321)

		Example
1.	Define nominal supply voltage and tolerance, minimum and maximum supply voltage, and maximum ambient temperature	$V_S = 40\ V \pm 10\%$ $V_S(min) = 36\ V.$ $V_S(max) = 44\ V.$ $T_A(max) = 75°C$
2.	Compute maximum value of R_S using voltage and current at point X $R_S(max) = \frac{V_S(min) - V_X}{I_X}$	$R_S(max) = \frac{36 - 11.55}{21} = 1.16\ K\Omega$
3.	Assume resistor tolerance, and compute nominal value or R_S $R_S(nom) = R_S(max)(1 - \%\ Tolerance)$ FIND NEXT LOWER STANDARD VALUE	Tolerance = 10% $R_S(nom) = 1.16 \times 0.9 = 1.05\ K\Omega$ $1\ K\Omega$
4.	Construct the worst-case load line using the minimum value of R_S and the maximum value of V_S. Two points are required. Because the voltage scale is incomplete, find the current at 10 volts and 13 volts. $I_{10} = \frac{V_S(max) - 10}{R_S(min)}$ $I_{13} = \frac{V_S(max) - 13}{R_S(min)}$ Connect Points 10, I_{10} (F) and 13, I_{13} (G)	$I_{10} = \frac{44 - 10}{0.9\ K\Omega} = 36.8\ mA$ $I_{13} = \frac{44 - 13}{0.9\ K\Omega} = 34.5\ mA$
5.	Compute the worst-case dissipation. This condition occurs at the point at which the load line F-G intersects either curve A or curve D. Multiply the voltage and current at each intersection, and use the higher value.	$P_1 = 36 \times 11.1 = 400\ mW$ $P_2 = 34.8 \times 12.4 = 432\ mW$ $P_{MAX} = 432\ mW$
6.	Find the maximum allowable temperature permitted for P_{MAX} on Fig. 319.	From Fig. 319, $T_A(max) > 85°C$
7.	If $T_A(max)$ is greater than the maximum value required, the design is satisfactory.	
8.	If $T_A(max)$ is less than the maximum value required, go back to step 2 and recompute for a tighter tolerance on R_S, or go back and choose a higher supply voltage.	
9.	Compute the required dissipation rating for R_S. Use $V_S(max)$, $R_S(min)$ and the lower of the two values of power calculated in step 5. $P = \frac{V_S(max)^2}{R_S(min)} - P\ (from\ 5)$	$P = \frac{44^2}{900} - 0.400 = 1.75\ watts$ R_S is a 1 KΩ resistor with a ±10% tolerance

Figs. 320 and 321 show the limiting power-supply condition, together with the test circuit used to determine this condition, for the CA3041 and CA3042 circuits, respectively. For supply-voltage values (at terminal 14) below 10 volts, the zener diodes Z2 and Z3 do not conduct, and the current drain is that of the connected portions of the integrated circuit. The vertical distances between the curves in Figs. 320 and 321 represent the limits of current drawn by the operating portions of the circuit. The current drawn by the zener diodes adds to the circuit current at supply voltages (at terminal 14) above 10 volts. The voltage difference

Table XXXI — *Procedure for Finding the Series Dropping Resistor R_S for CA3041*

(Points referred to in the procedure are shown on Fig. 320)

		Example
1. to 5.	Follow steps 1 through 5 from CA3042 procedure except note that the dissipation does not include the power dissipated in the audio amplifier.	
6.	Select power-supply voltage and nominal operating point for audio amplifier. Note from published data for CA3041 that the ac voltage swing is limited to the range of +1 to +29 volts by saturation effects and breakdown voltage.	Use same supply as before $V_S(nom) = 40$ $V_S(max) = 44$ $V_C(nom) = 15$ volts (Point N)
7.	Find the audio load resistor R_L $R_L = \frac{V_S(nom) - V_C(nom)}{I_C(nom)}$	$R_L = \frac{40 - 15}{4\text{ mA}} = 6.25$ K use nearest 10% resistor, 6.8 K
8.	Find worst-case load line using $V_S(max)$ and $R_L(min)$ $R_L(min) = R_L(1 - \%\text{ Tolerance})$ Load line intersects V = 0 at $I = \frac{V_S(max)}{R_L(min)}$ Load line intersects V = 30 V at $I = \frac{V_S(max) - 30}{R_L(min)}$	$R_L(min) = 6.8\text{ K} \times .9 = 6.1$ K $I = \frac{44}{6.1} = 7.2$ mA (Point P) $I = \frac{14}{6.1} = 2.3$ (Point Q)
9.	Compute P_{audio} at point $P_{audio} = I_R \times V_R$	$P_{audio} = 4.7 \times 16 = 75$ mW
10. to 14.	Add P_{audio} to P_{Max} from Step 5, and proceed with steps 6 through 9 of the CA3042 procedure.	

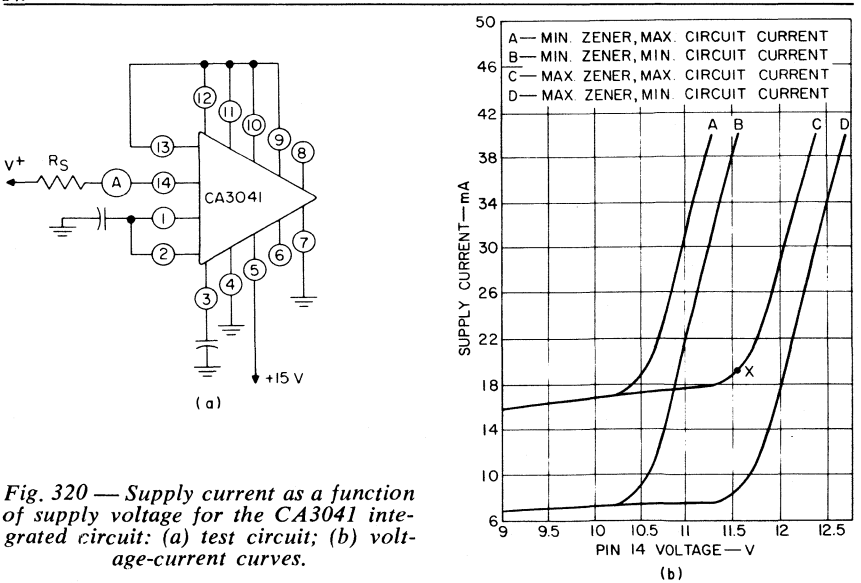
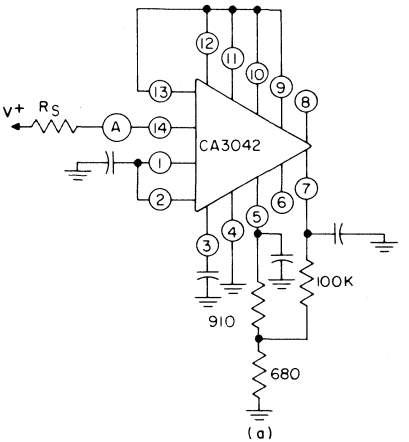
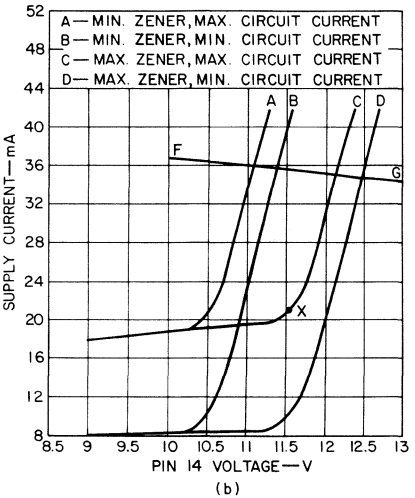


Fig. 320 — Supply current as a function of supply voltage for the CA3041 integrated circuit: (a) test circuit; (b) voltage-current curves.



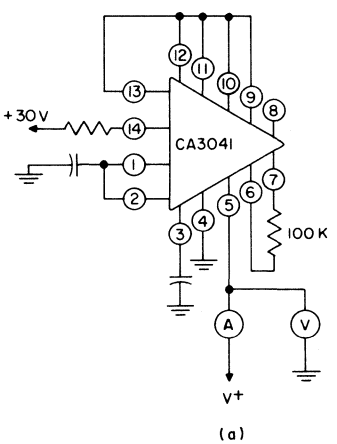


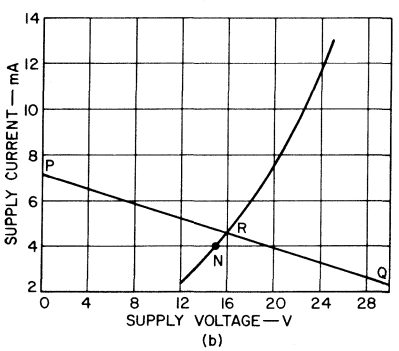
All resistance values in ohms unless otherwise specified.

Fig. 321 — Supply current as a function of the supply voltage for the CA3042 integrated circuit: (a) test circuit; (b) voltage-current curves.

between curves A and C at a total drain of 25 milliamperes indicates a tolerance of less than ±5 per cent on the zener voltage.

The voltage-current curves for the CA3041 and CA3042 differ because the current for the final amplifier stage is drawn from the main dropping resistor in the CA3042 and through an external resistor in the CA3041. Fig. 322 shows the dc voltage-current relationship for the audio-amplifier stage in the CA3041 circuit. The audio-amplifier stage is self-biased by the 100-kilohm resistor between terminal 6 and terminal 7 so that a unique curve is formed.





All resistance values in ohms unless otherwise specified.

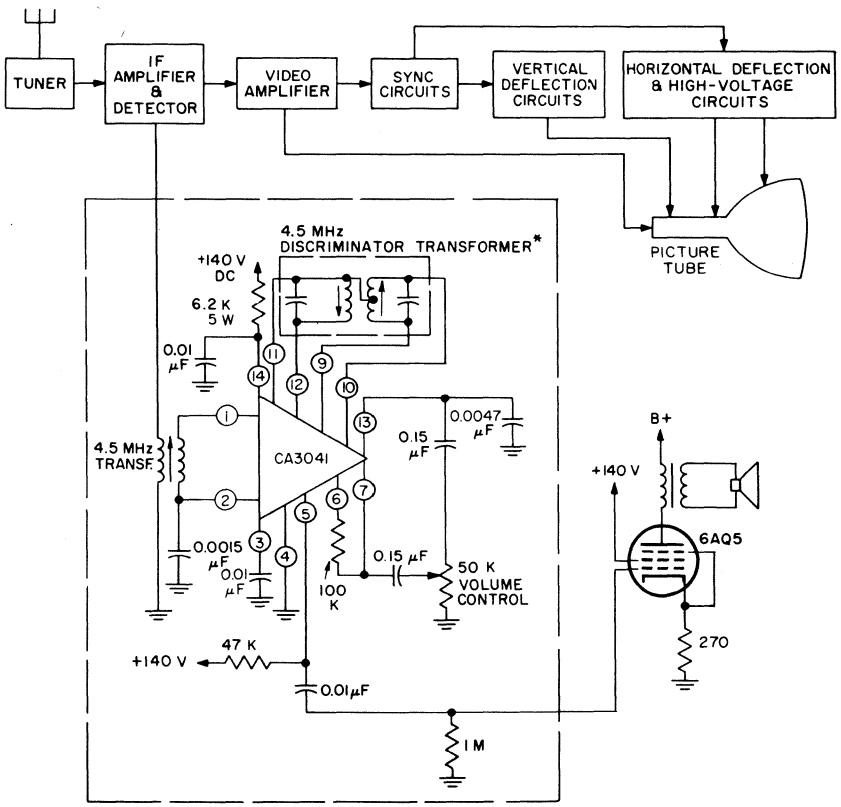
Fig. 322 — Collector characteristic of the audio-amplifier stage of the CA3041 integrated circuit: (a) test circuit; (b) voltage-current curves.

Applications—The block diagrams shown in Figs. 323, 324, and 325 illustrate use of the CA3041 and CA3042 circuits in the sound channel of an intercarrier television receiver.

In addition to application of the CA3041 and CA3042 for sound-channel processing in television receivers, these circuits may also be used for FM if amplification in high-fidelity FM receivers. The applications information pertaining to the CA3011 and CA3012 may also be applied to the CA3041 and CA3042. Terminal loading conditions, however, must be considered in order to assure that stable operation is maintained. Stable operation of the CA3041 and CA3042 requires that the product of the load and source conductances be given, as follows:

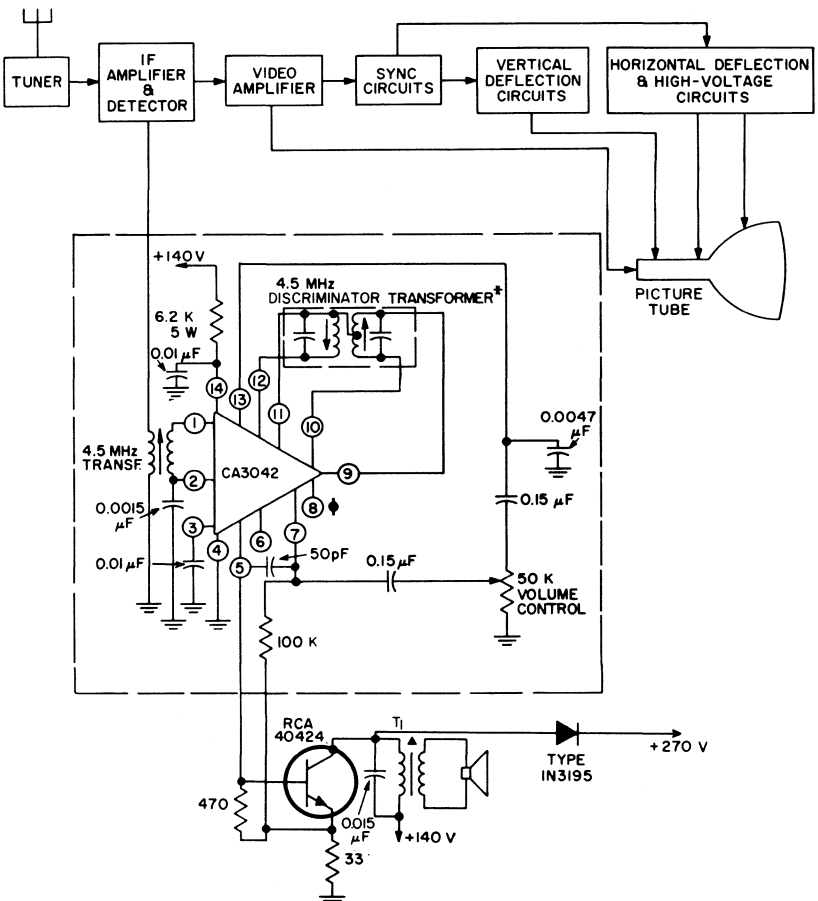
$$g_S g_L(\text{min}) = 1.6 \times 10^{-6}\ (\text{mhos})^2$$

In television sets using the CA3041 or CA3042 integrated circuits, the volume control is often located remote from the amplifier.



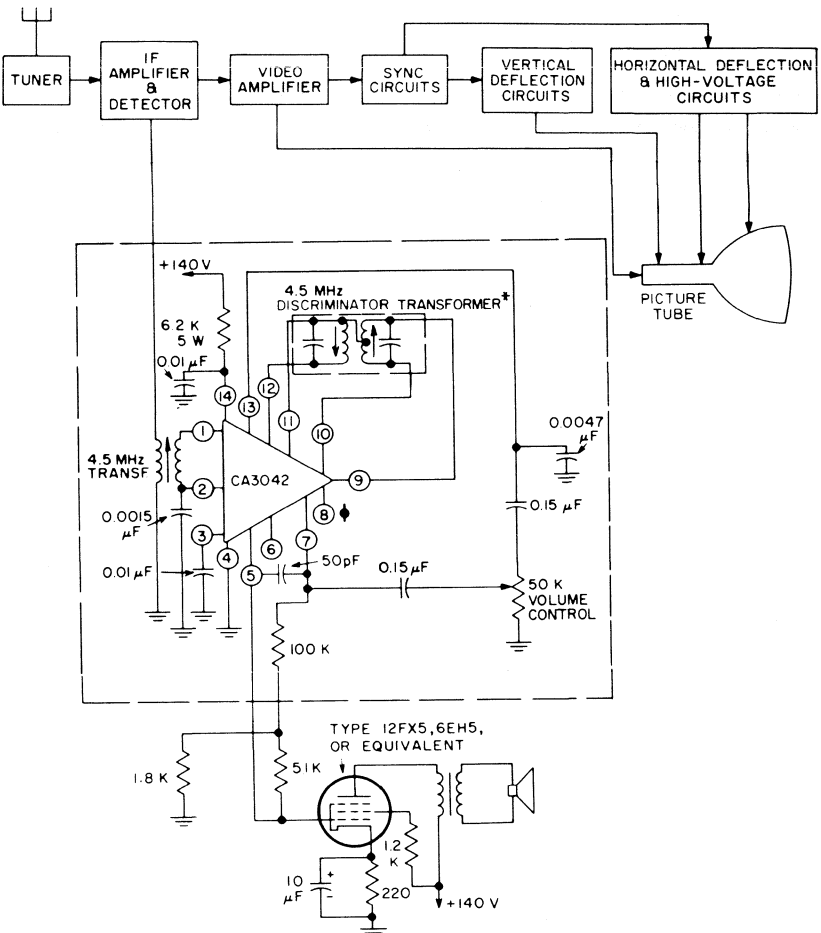
All resistance values in ohms unless otherwise specified.

Fig. 323 — Block diagram of typical television receiver using the CA3041.



All resistance values in ohms unless otherwise specified.

Fig. 324 — Block diagram of typical television receiver using the CA3042 and an RCA-40424 transistor audio output stage.



All resistance values in ohms unless otherwise specified.

Fig. 325 — Block diagram of typical television receiver using the CA3042 and a 12FX5, 6EH5, or equivalent.

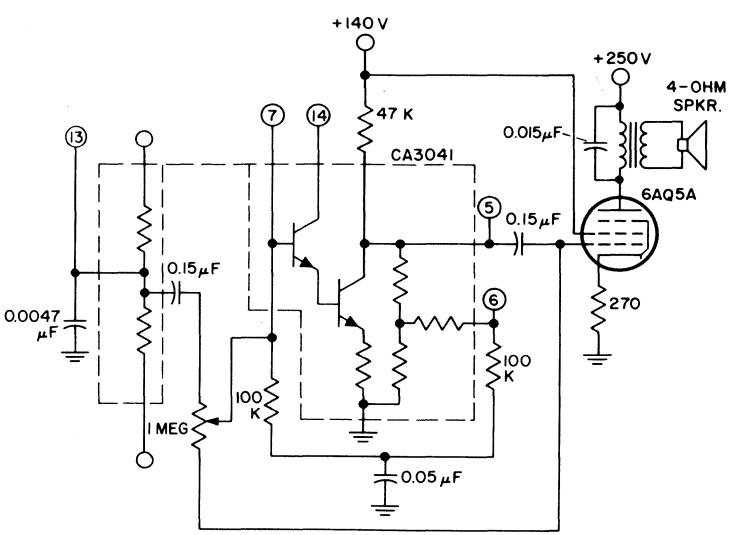
The long leads required in such a configuration sometimes pick up undesirable signals that, in turn, cause the system to exhibit hum and noise at low volume levels. The feedback-type volume control reduces hum and noise pick-up by reducing the gain of the system rather than the signal level, and thus eliminates the cost of shielding the leads.

Figs. 326 through 330 show conventional and feedback types of volume-control circuits for the CA3041 and CA3042.

CA3065 Integrated Circuit

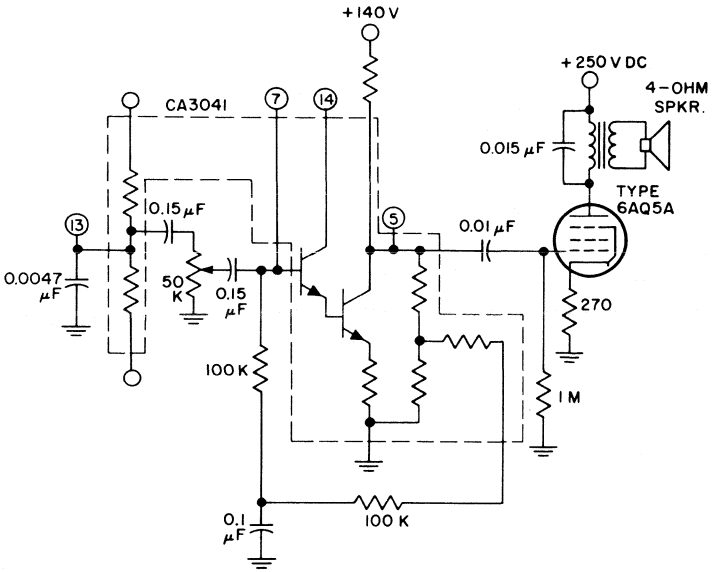
The RCA CA3065 television sound system is a monolithic integrated circuit which combines a multistage if amplifier-limiter, an FM detector, an electronic attenuator, a zener-diode-regulated power supply, and an audio amplifier-driver that is designed to drive directly an n-p-n power transistor or a high-transconductance tube. Because the circuit is so inclusive, a minimum number of external components is required. This circuit is supplied in a 14-terminal dual-in-line plastic package. It operates over a temperature range of −40°C to +85°C.

The CA3065 with its advanced circuit design provides a high-performance multistage subsystem for the sound system of a television receiver. A particular feature of the CA3065 is the electronic attenuator which performs the conventional volume-control function. Volume control is accomplished when the bias levels in the attenuator are changed by means of a variable resistor connected between terminal 6 and ground (attenuation in excess of 60 dB is attained). Because no audio signal is present in this control, hum or noise pickup can be bypassed. In most cases, only a single unshielded wire is required between the if board and the variable resistor (volume control).



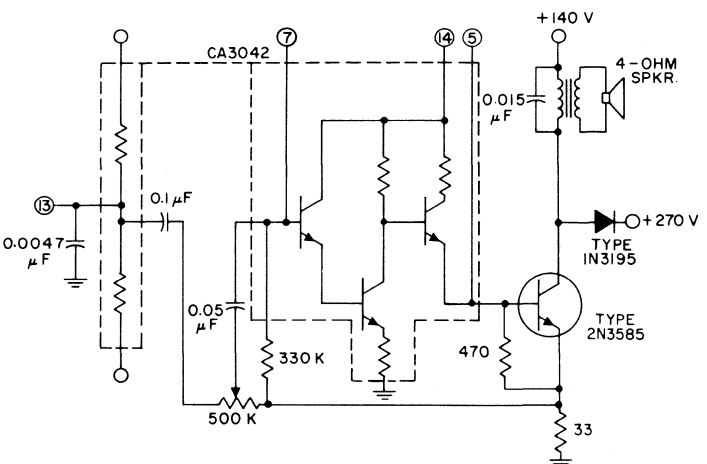
All resistance values in ohms unless otherwise specified.

Fig. 326 — A feedback volume-control circuit for the CA3041.



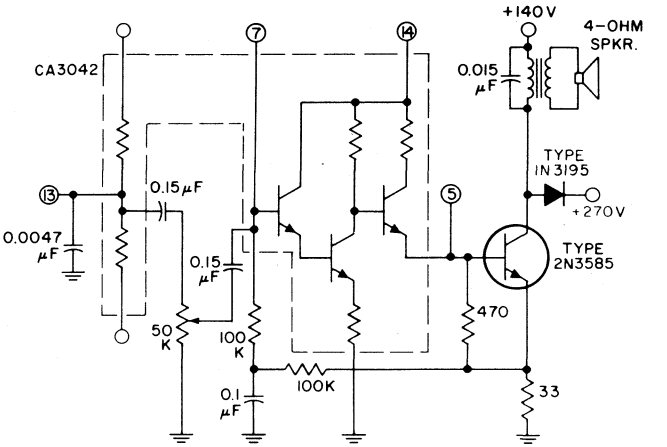
All resistance values in ohms unless otherwise specified.

Fig. 327 — A conventional volume-control circuit for the CA3041.



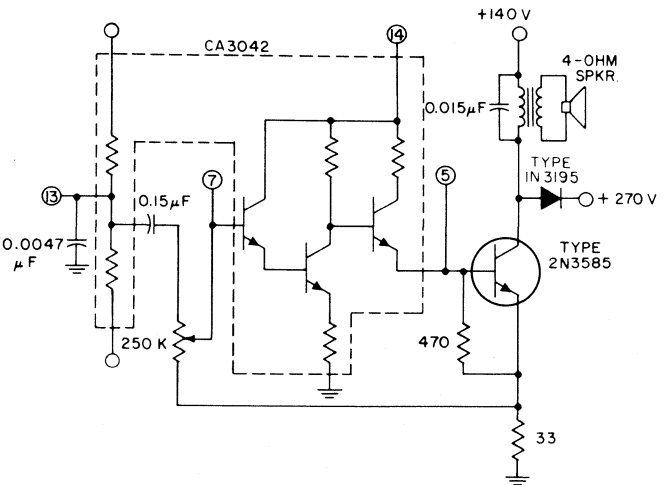
All resistance values in ohms unless otherwise specified.

Fig. 328 — A feedback volume-control circuit for the CA3042.



All resistance values in ohms unless otherwise specified.

Fig. 329 — A conventional volume-control circuit for the CA3042.



All resistance values in ohms unless otherwise specified.

Fig. 330 — A low-cost feedback volume-control circuit for the CA3042.

Fig. 331 shows the schematic diagram of the CA3065. Fig. 332 illustrates the use of this circuit in a typical application. The differential peak detector circuitry requires the use of only one single-tuned coil. The if-amplifier section has a limiting (knee) sensitivity of 200 microvolts at 4.5 MHz, and provides typical AM rejection of 50 dB. Fig. 333 shows the gain-reduction characteristics of the attenuator section of the circuit.

AUTOMATIC-FINE-TUNING (AFT) SYSTEMS

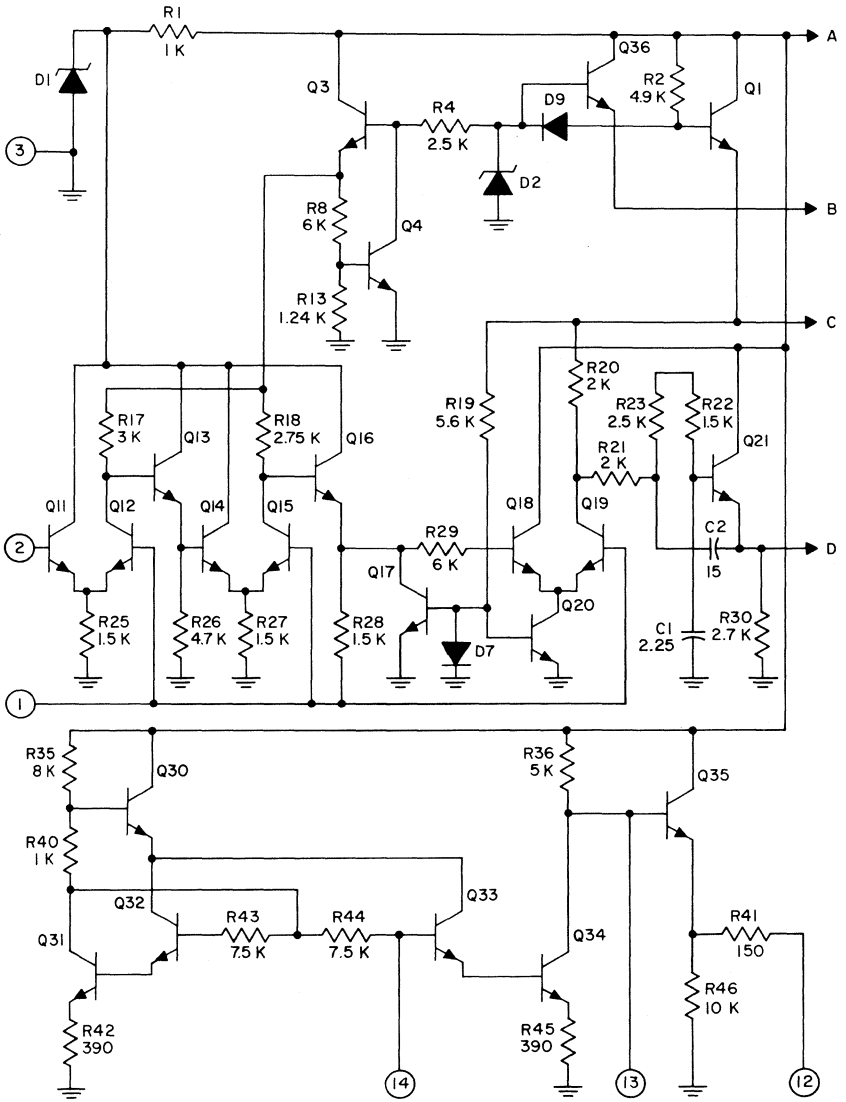
The RCA-CA3044 and CA3064 monolithic integrated circuits are designed specifically for use in automatic-frequency-control applications. The CA3044 is intended primarily for operation with three-tube video if strips, in which the signal level in the last if stage is relatively high. The input amplifier of the AFT circuit is connected to the last if stage; the sensitivity requirements of the circuit, therefore, are relatively low. The CA3064, on the other hand, is intended primarily for use with transistor or two-tube video if strips, in which the video signal in the last stage is at a comparatively low level and there is a need for greater sensitivity in the input amplifier of this AFT circuit. In addition, in the design of the CA3064 input amplifier, the need for an external input choke is eliminated. These circuits are supplied in 10-terminal TO-5-style packages and operate over a temperature range of −55°C to +125°C.

Circuit Description

The schematic diagrams of the CA3044 and CA3064 are shown in Figs. 334 and 335. The use of these circuits in a typical automatic-fine-tuning (AFT) system for a color television receiver is shown in Fig. 336. In such a system, the CA3044 and CA3064 provide all of the signal-processing components needed (with the exception of the tuned phase-detector transformer) to derive the AFT correction signals from the output of the video-if amplifier. The other components of the system provide signal coupling and power-supply decoupling as required for proper signal processing in the video intermediate-frequency range.

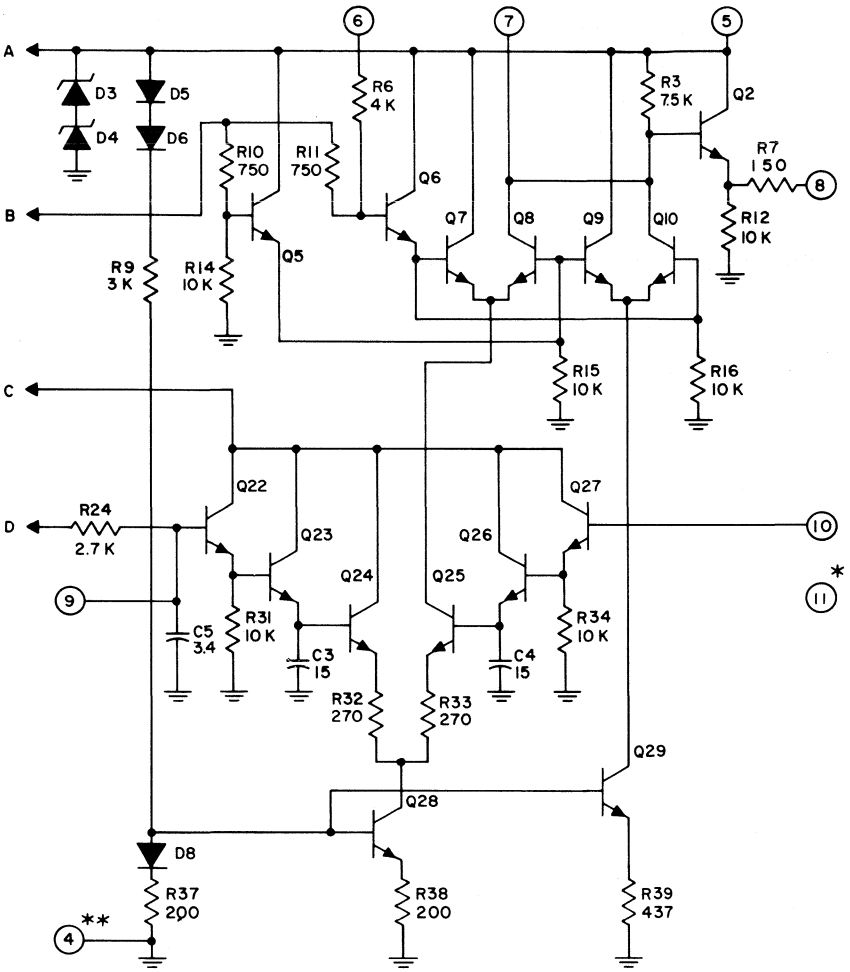
The CA3044 integrated circuit can be considered as the combination of four functional blocks: a limiter-amplifier, a balanced detector, a differential amplifier, and a regulator. The CA3064 is comprised of the same four functional blocks as the CA3044, plus an agc amplifier block. In each circuit, the 45-MHz limiter-amplifier is basically a differential amplifier that supplies a peak-to-peak output current of approximately 4 milliamperes for input levels above the limiting threshold. The use of a load impedance which does not exceed 2000 ohms guarantees an excellent limiting characteristic and eliminates detuning effects caused by saturation of the amplifier under worst-case conditions. In the system shown in Fig. 336, the load impedance at the center frequency is about 1800 ohms.

For the CA3044, the diode matrix composed of D1, D2, D3, and D4 constitutes a balanced detector that converts the output of the phase transformer to a filtered dc signal. Diodes D1 through D4 perform the detection function. Diodes D7 and D8 are always reverse-biased and serve as capacitors; they filter the output of the detector in conjunction with resistors R9 through R12. Diodes D5 and D6 are included to balance the parasitic diodes that exist



All resistance values in ohms unless otherwise specified.

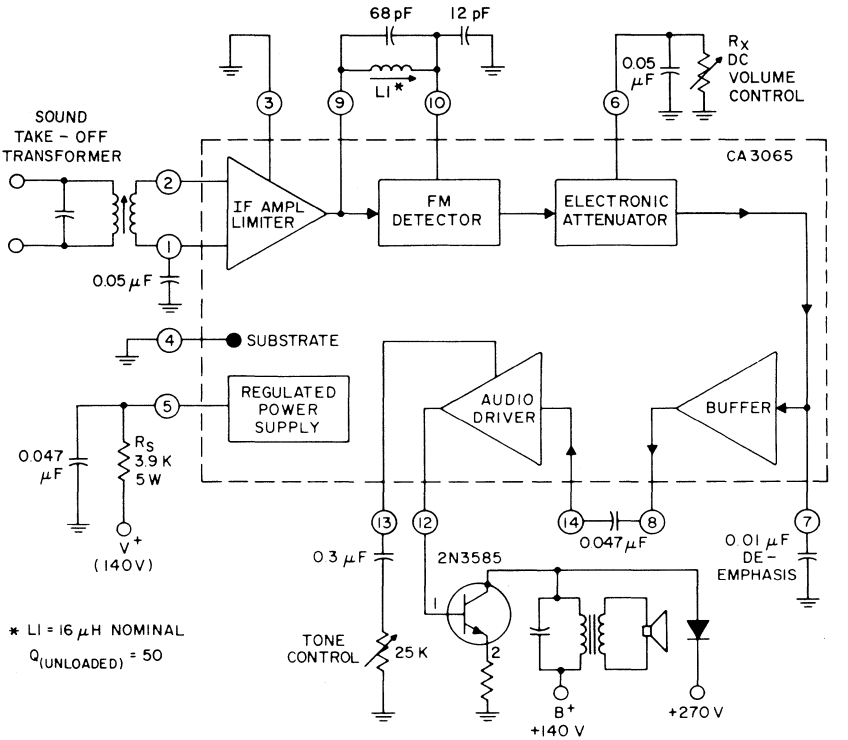
Fig. 331 — CA3065 integrated-circuit television sound system.
(Continued on page 267)



* INTERNAL CONNECTION; DO NOT USE.
** SUBSTRATE CONNECTION; ALWAYS CONNECT TO TERMINAL 3

All resistance values in ohms unless otherwise specified.

Fig. 331 — CA3065 integrated-circuit television sound system.
(Continued from page 266)



All resistance values in ohms unless otherwise specified.

Fig. 332 — Block diagram of CA3065 in a typical circuit application.

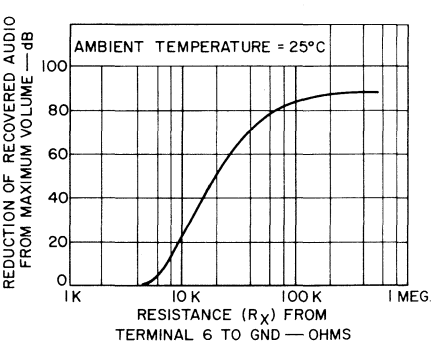


Fig. 333 — Gain reduction as a function of resistance (terminal 6 to ground).

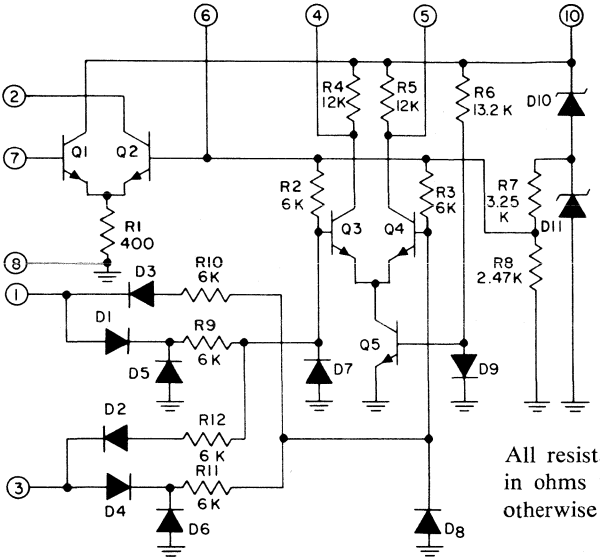
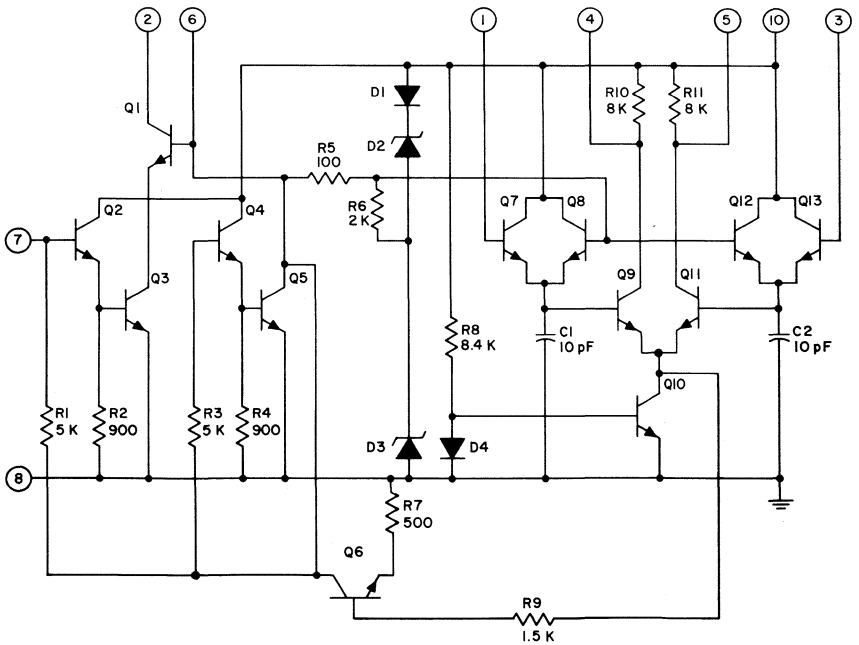
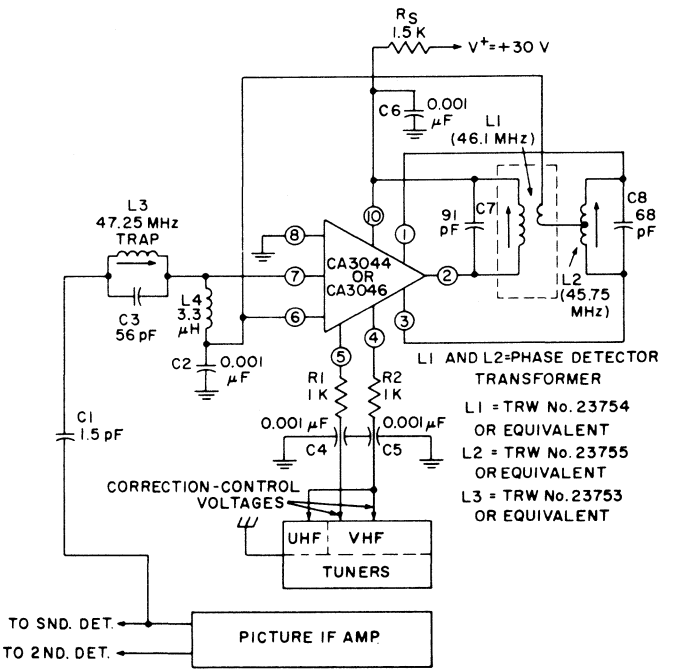


Fig. 334 — CA3044 integrated-circuit AFT system.



All resistance values in ohms unless otherwise specified.

Fig. 335 — CA3064 integrated-circuit AFT system.



All resistance values in ohms unless otherwise specified.

Fig. 336 — System diagram of a typical automatic-fine-tuning (AFT) application showing the CA3044 or CA3064 in use in a color-TV receiver.

between the cathodes of D2 and D3 and the substrate. In the CA3064, the detection function is performed by transistors Q7, Q8, Q12, and Q13. Capacitors C1 and C2 are provided to filter the output of the detector.

In the CA3044, transistors Q3, Q4, and Q5 form a constant-current-driven differential amplifier that is directly coupled to the output of the detector. The amplifier contributes greatly to the high sensitivity of the system and, in addition, provides sufficient power to allow the use of a low cost tuning element. The out-

put impedance at either output of the amplifier is approximately 12,000 ohms.

The constant-current-driven differential amplifier in the CA3064 is formed by transistors Q9, Q10, and Q11. The impedance at either output of the amplifier is approximately 8000 ohms.

The zener-diode regulator, comprising D10 and D11 for the CA3044 and D1, D2, and D3 for the CA3064, provides the regulation necessary for a differential post-detection amplifier that is both stable and independent of temperature and power-supply variations.

During normal operation, the proper dc bias for terminals 1, 3, and 7 of the CA3044 or CA3064 is supplied through terminal 6 and external rf coils, as shown in Fig. 336. RF bypassing is required both for terminal 6 and for terminal 10, which is connected through the primary winding of the detector transformer to terminal 2.

Operating Characteristics

The CA3044 is designed to operate from supply voltages greater than the zener regulating voltage of 10.5 to 11.9 volts at the 14-milliampere current-drain level. The CA3064 regulating voltage is 10.9 to 12.8 volts. For proper regulation and operation, the supply voltage, which is applied to terminal 10 through an appropriate dropping resistor, should be greater than 15 volts. Proper combinations of power-supply voltages and series dropping resistance can be determined by use of the same procedure as that employed for CA3041 and CA3042 integrated circuits, described previously in the discussion of **Television Sound-System Circuits.**

Dynamic Performance

The system diagram in Fig. 336 shows the CA3044 or CA3064 in its function as rf amplifier, frequency discriminator, and post-detection differential dc amplifier. The circuit shown is a portion of a color television receiver in which critical tuning is essential because of the presence of the color subcarrier and its sidebands. The CA3044 or CA3064 AFT system provides a uniform and accurate tuning reference. When the correction voltage developed at terminals 4 and 5 of the CA3044 or CA3064 is sufficient, the system locks on the picture-carrier intermediate frequency and holds the tuner oscillator within ±25 kHz of the picture carrier so that a high-quality picture is produced at all times. Operation within such a narrow band of oscillator frequencies represents a color-reference deviation of less than 5 per cent from the ±500-kHz color-subcarrier sidebands; this deviation is in general far smaller than the amplitude and phase-change errors that are introduced by other receiver and transmitter functions.

The system shown in Fig. 336 can be used in a typical color receiver. The sampling connection from the picture-if amplifier to the AFT circuit is made from the output of the last if stage directly to the input of the CA3044 or CA3064 rf amplifier. The loading effect of the AFT-system coupling circuit on the picture-if amplifier is negligible and does not distort the if response. Unless provision has been made to trap out the adjacent-channel sound carrier elsewhere in the circuit, such action must be taken at the input to the CA3044 or CA3064. Trapping of the adjacent-channel sound carrier is essential because it may have sufficient amplitude to cause limiting at

the rf amplifier-limiter stage of the CA3044 or CA3064. The trapping circuit, composed of L3 and C3 in Fig. 336, also helps to peak the picture carrier at 45.75 MHz while trapping the adjacent-channel sound carrier at 47.25 MHz. To compensate for an if response that places the picture carrier at the 50-per-cent point on the if slope, the input trap should be adjusted to peak the response above 45.75 MHz at the input to the CA3044 or CA3064.

Proper dc biasing of the amplifier/limiter stage requires that a small choke, L4, be used to couple terminal 6 to terminal 7. The common bias connection at terminal 6 is bypassed with a 0.001-microfarad disc capacitor. No form of external dc connection should be made to either terminal 6 or terminal 7.

The output load on the differential amplifier consists of the impedance of the phase-shift transformer comprising L1 and L2. The differential-amplifier stage assures symmetrical limiting above 100 millivolts at the input of terminal 7. The primary of the phase-shift transformer is typically tuned to 46.1 MHz as an additional error-correction device to help peak the picture carrier at 45.75 MHz. The secondary is tuned to 45.75 MHz and symmetrically drives the double-balanced detector.

The error signal detected by the double-balanced detector is fed to the inputs of the differential output amplifier. The differential output amplifier is compensated for all temperature-change effects including those of the zener-diode regulator. In the absence of an error signal, output terminals 4 and 5 are at a dc level of 6.5 volts; in mistuning or frequency correction, the output level varies from 33 to 85 per cent of the zener-regulated voltage over the ±25-kHz limits. Fig. 337 shows

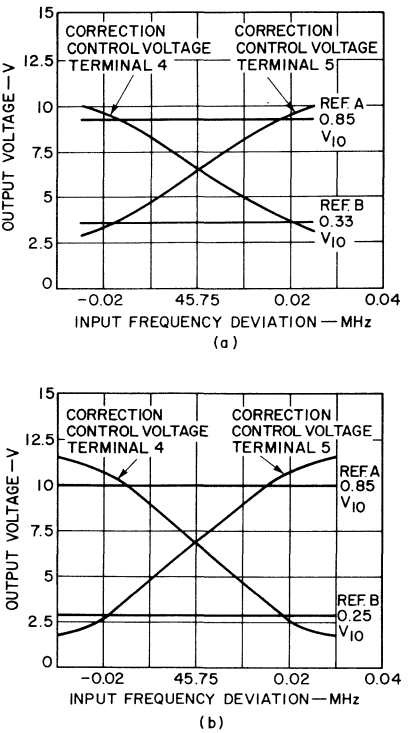


Fig. 337 — Typical narrow-band dynamic control voltage characteristic (a) for the CA3044 and (b) for the CA3064.

the typical narrow-band response of the system shown in Fig. 336; Fig. 338 shows the wide-band response. The curves shown are characteristic of the Fig. 336 circuit for an input rf signal level of 200 millivolts rms at terminal 7. Both narrow- and wide-band response characteristics are a function of the limiting level. The narrow-band crossover slope decreases and the wide-band response becomes narrower as the signal level decreases.

The reference levels (A, B, C, and D) indicated on the curves shown in Fig. 337 and 338 refer to the narrow- and wide-band control points expressed as a percentage of

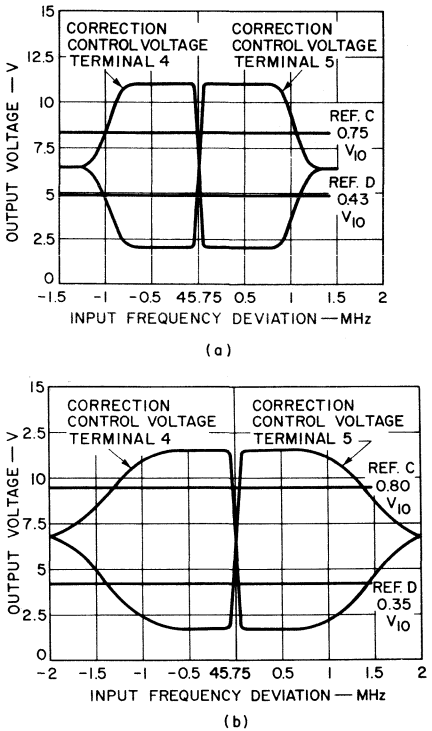


Fig. 338 — Typical wide-band dynamic control voltage characteristic (a) for the CA3044 and (b) for the CA3064.

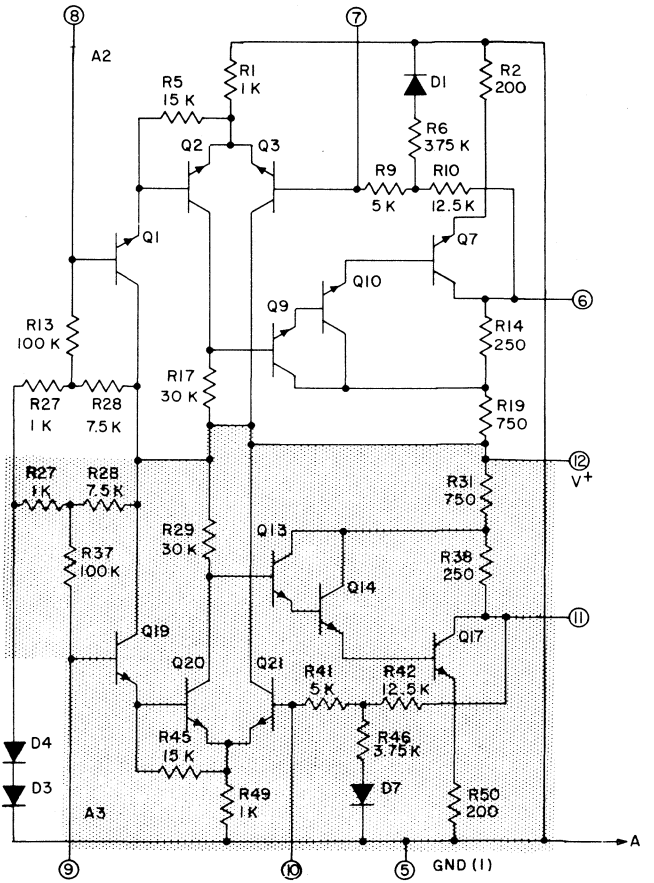
the zener reference voltage at terminal 10. References A and B are narrow-band (±25-kHz) control points at 85 and 33 per cent of the terminal 10 reference voltage, while references C and D are the wide-band (±0.9-MHz) control points at 75 and 43 per cent of the same voltage.

The correction voltages from terminals 4 and 5 are applied to the tuning elements of the voltage-controlled oscillator portion of the uhf and vhf tuners. These voltages may be used single-ended and in either phase-polarity for uhf oscillator control. The vhf oscillator may be controlled with a push-pull output to assure attainment of maximum tuning range. The channel-tuning defeat-switch function is normally accomplished by shorting the control-voltage terminals 4 and 5 together. For filtering purposes and to protect the integrated circuit, it is best to include a shunt capacitor and series resistor between the tuning elements and terminals 4 and 5; in Fig. 336, 1000-ohm resistors and 0.001-microfarad feed-through capacitors are used.

AUDIO AMPLIFIERS

The RCA CA3048 and CA3052 silicon monolithic integrated circuits are designed specifically for stereo preamplifier service. Each circuit consists of four identical independent amplifiers that can be connected to provide all the amplification necessary in a dual-channel preamplifier for a high-quality phonograph system. When a signal source is connected to the inputs of a CA3048 or CA3052 unit operated in this mode, the output of each channel may be used to drive a high-quality, high-power audio amplifier; all intermediate functions are accomplished by interconnection with the CA3048 or CA3052 preamplifier circuit. The CA3048 amplifier array is schematically identical with the CA3052. Each amplifier of the CA3048 is tightly specified for equivalent output noise under a variety of test methods. The CA3052 is specified using RIAA* test methods for equivalent input noise using one test method for amplifiers 1 and 4, and an appropriately different method for amplifiers 2 and 3. These circuits are supplied in 16-terminal dual-in-line plastic packages and may be operated over a temperature range of −25°C to +85°C.

* Record Industry Association of America



All resistance values in ohms unless otherwise specified.

Fig. 339 — CA3048 or CA3052 integrated-circuit amplifier array.
(Continued on page 275)

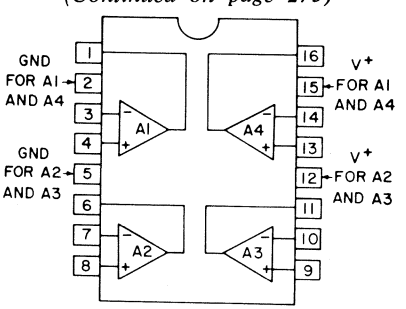
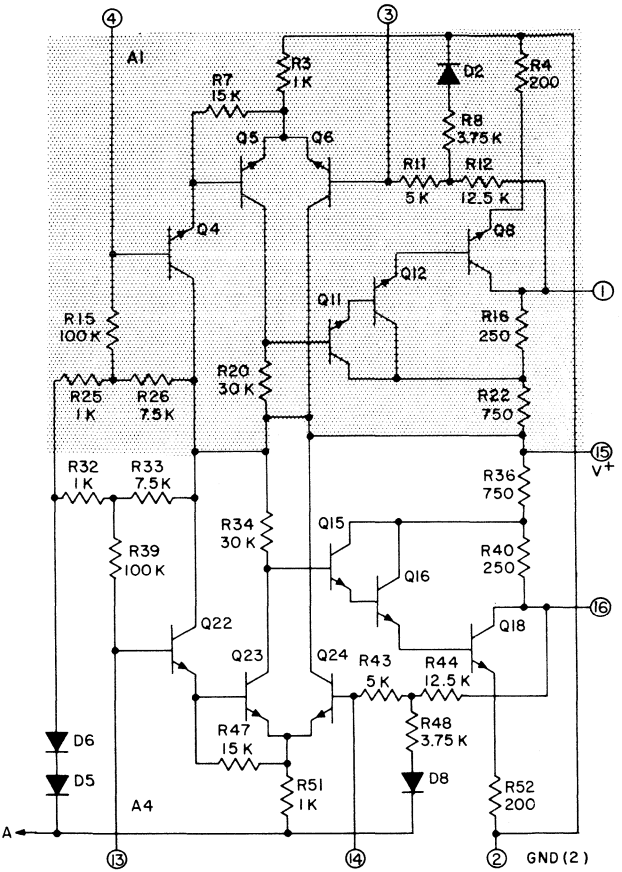


Fig. 340 — Block diagram of CA3048 or CA3052 integrated-circuit amplifier array.



All resistance values in ohms unless otherwise specified.

Fig. 339 — CA3048 or CA3052 integrated-circuit amplifier array. *(Continued from page 274)*

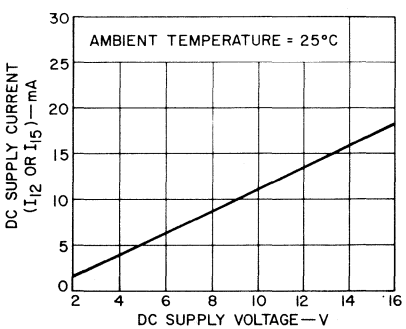


Fig. 341 — Typical dc supply current as a function of supply voltage.

Circuit Description

Fig. 339 and Fig. 340 on pages 274 and 275 show a detailed schematic and a block diagram, respectively, of the CA3048 or CA3052 integrated-circuit amplifier array. Each of the amplifiers A1 through A4 provides two stages of voltage gain. The input stage is basically a differential amplifier with a Darlington transistor added on one side. The output stage uses a combination of three transistors connected in an inverting configuration.

Input signals to the amplifiers in the CA3048 or CA3052 are normally applied to the noninverting input terminal (terminal 9 for amplifier A3) to the base of the Darlington input transistor (Q19). The 0.1-megohm resistor R37 supplies bias current for this transistor. The voltage drop across the resistor is small because the base current of the Darlington transistor is very small.

Each amplifier in the CA3048 or CA3052 array may be viewed as an ac operational amplifier in which a fixed resistance is permanently connected between the output and the inverting input. In amplifier A3, this resistance is provided by the series combination of resistors R41 and R42.

The amplifiers in the CA3048 and CA3052 arrays are normally operated in the noninverting configuration; it is important, therefore, to minimize the capacitance from output to input. Excessive capacitance between output and input can result in a peaked response, instability, or even oscillation in extreme cases. In general, however, if sound design practices, careful layout, and typical terminations are used, a stable predictable circuit results.

Operating Characteristics

Figs. 341 (on page 275) through 345 show typical dc and ac operating characteristics for the CA3048 or CA3052 as measured in the test circuits shown in Figs. 346 and 347.

Fig. 348 shows the curve of total harmonic distortion as a function of ambient temperature.

First Amplifier Section of Preamplifier

In order that the signal applied to the second amplifier section is not degraded in signal-to-noise ratio, the gain of the first amplifier section of the preamplifier should be sufficient to raise the signal more than 40 dB. The gain of the first amplifier, however, should not be so high that the amplifier overloads at maximum signal levels (i.e., at a recorded velocity of 25 centimeters per second).

Each amplifier of the CA3048 or CA3052 array has an open-loop gain of 58 dB which is sufficient to allow the design described above to be realized. A schematic of the first-section amplifier is shown in Fig. 349. The breakpoints ω_2 and ω_3 are determined as indicated in the figure. The low-frequency breakpoint ω_2 is caused mainly by C3 and the input impedance at the inverting input terminal.

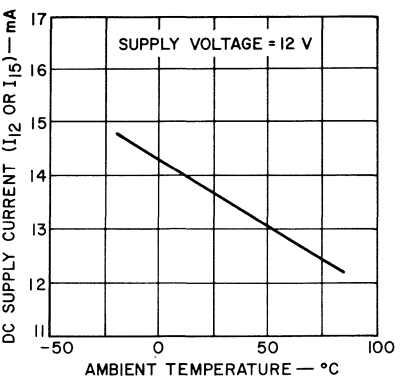


Fig. 342 — Typical dc supply current as a function of ambient temperature.

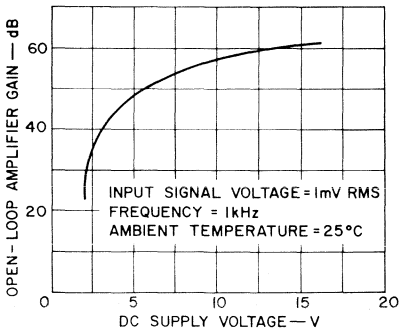


Fig. 343 — Typical amplifier gain as a function of supply voltage.

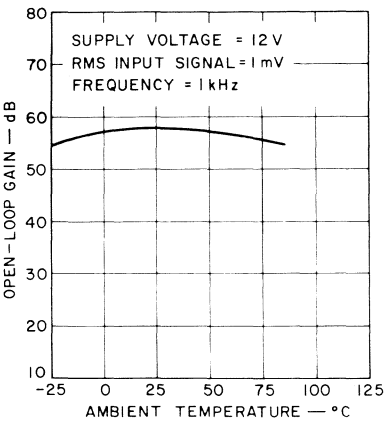


Fig. 344 — Typical open-loop gain as a function of ambient temperature.

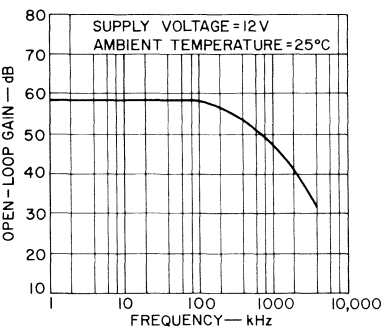


Fig. 345 — Typical open-loop gain as a function of frequency.

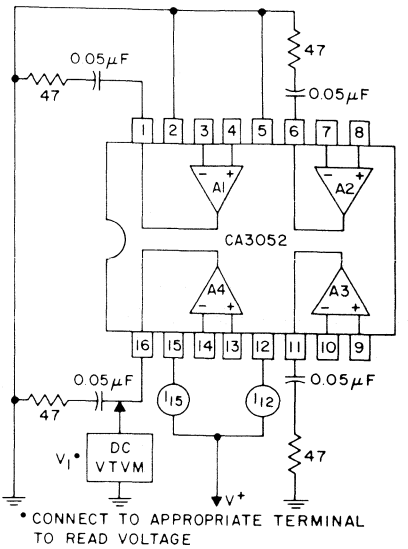


Fig. 346 — Test circuit for measurement of collector supply voltage and currents.

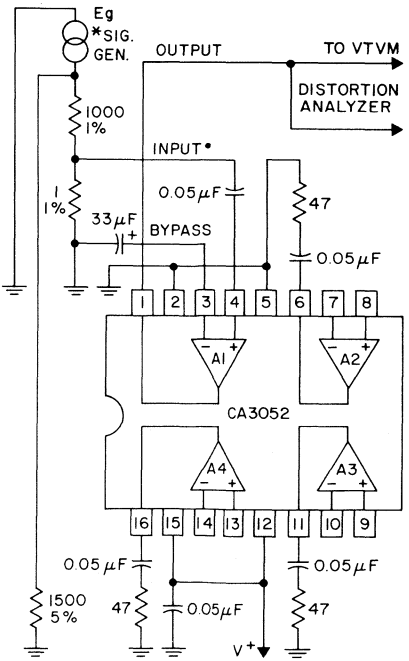


Fig. 347 — Test circuit for measurement of distortion, open-loop gain, and bandwidth characteristics.

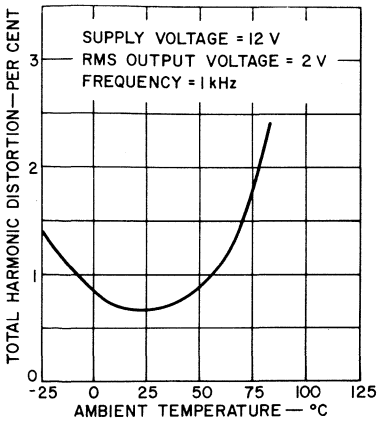
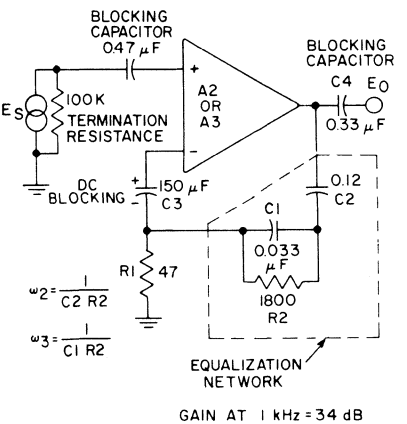


Fig. 348 — Typical total harmonic distortion as a function of ambient temperature.



All resistance values in ohms unless otherwise specified.

Fig. 349 — First-amplifier section of the CA3052 preamplifier (single channel) with RIAA equalization network.

Fig. 350 shows a family of curves of distortion as a function of supply voltage. The solid lines represent the most pessimistic performance possible because there is no negative feedback in the circuit. With a supply voltage of only 10 volts, a peak swing of 3 volts is available before the distortion reaches 2 per cent. In the equalizer circuit, there are varying amounts of negative feedback, depending on the frequency; the poorest situation occurs at low frequencies where there is maximum boost.

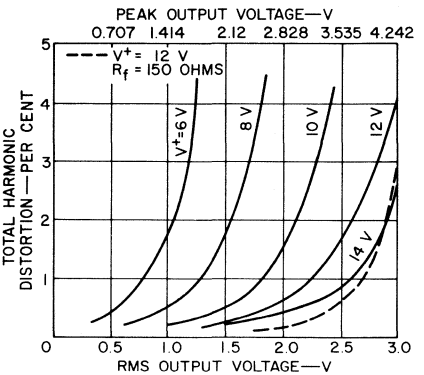


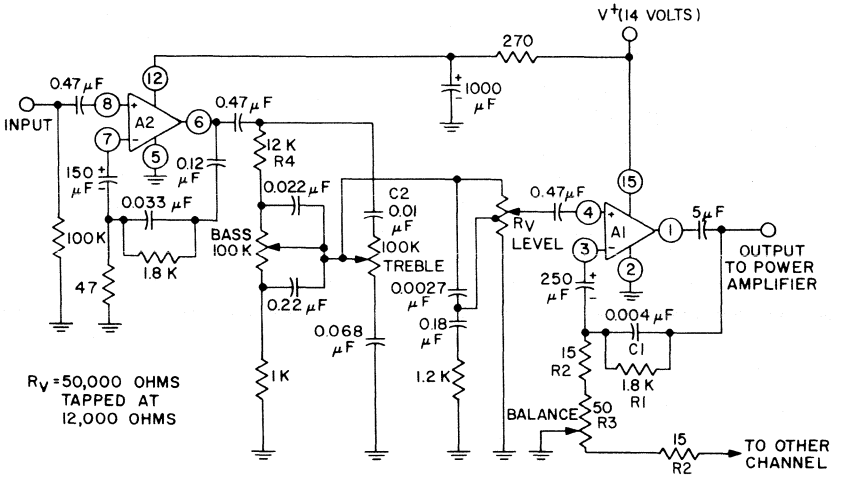
Fig. 350 — Total harmonic distortion of circuit shown in Fig. 349 as a function of output voltage for different dc supply voltages.

Complete Preamplifiers

A complete schematic diagram of a conventional single-channel preamplifier is shown in Fig. 351. The first amplifier/equalizer is the same as that shown in Fig. 349. Tone controls and a second amplifier have been added. The second amplifier provides a flat response in the audio range, but is rolled off at about 20 kHz by capacitor C1.

Because each amplifier of the CA3048 or CA3052 has an independent feedback point, it is possible to vary the gain for balancing. With this arrangement, the gain of one channel is increased while that of the other is decreased as the balance control is varied. The result is negligible change in level throughout the range of the control.

The resistor R1 in Fig. 351 acts in parallel with the feedback resist-



All resistance values in ohms unless otherwise specified.

Fig. 351 — One channel of a complete stereo preamplifier.

ance already on the integrated-circuit chip to reduce the gain. The resistors R2 and R3 reduce the negative feedback supplied by R1. This same amount of gain could have been programmed by omission of R1 and a corresponding increase in the values of R2 and R3. Analysis of differential-amplifier stages has shown that the equivalent noise source resistance comes from both inputs. Therefore, the low resistor values achieved by the use of R1 result in a decrease in the noise output by about 4 dB. This noise reduction is important when the level control is at the minimum setting and the signal-to-noise ratio is 0 dB. A schematic diagram of a second preamplifier (one channel only) is shown in Fig. 352. In this circuit, the equalizer and second-amplifier stages have been kept intact, but the positions of the level and tone controls have been reversed. In some cases, the design of complete systems is complicated by the fact that many loudspeakers tend to overload at low frequencies. In addition, there may be acoustic coupling between the input and output that causes an unstable "microphonic" condition at full gain.

With the arrangement shown in Fig. 352, it is possible to realize a system which has a great deal of bass boost at normal listening levels, but in which the gain at the bass end is restricted as the maximum level is approached. The value of resistor R4 in the tone-control network is made smaller in this system. At average listening levels, the difference is made up by the reduced series impedance presented by R4. The treble-boost capacitor must be increased so that there is little apparent loss in treble at low settings. The gain of the second amplifier is reduced to make the system gain equivalent at the reference frequency, but in so doing the net gain at the bass end is less.

As the level control is advanced, the sensation is one of a small change in emphasis from lows to highs.

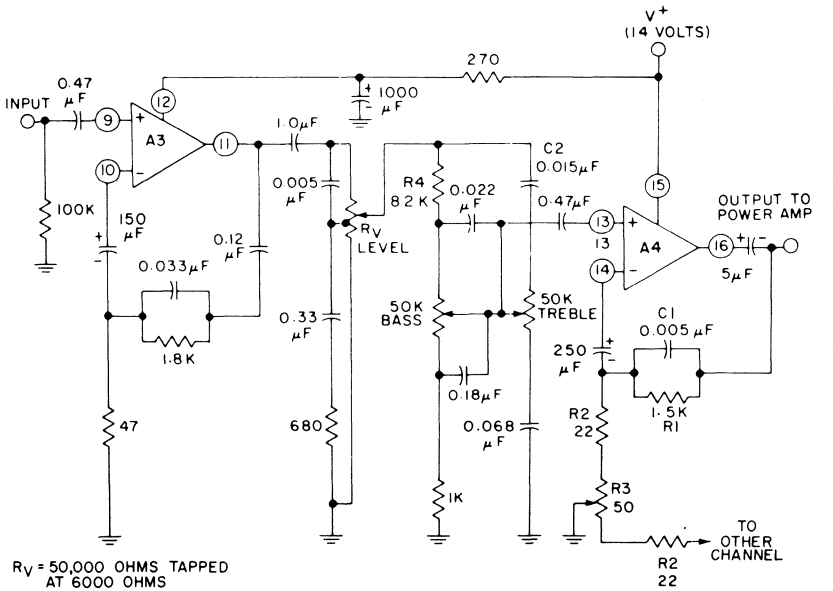
Feedback Level Control

Fig. 353 shows the use of the CA3048 or CA3052 in a preamplifier that employs feedback volume control. In a feedback-volume-control circuit, the gain, rather than the input level, of the amplifier is varied. The level control is located between the output and the inverting input of the CA3048 or CA3052. At minimum volume, the entire output is fed back to the input. With this amount of feedback, some external stabilization is required; C3 and R5 are used to provide this stabilization.

The maximum gain level of the second amplifier stage is determined by the ratio of R_v and R6. Adjustment of R_v also varies the ratio of feedback resistance to source resistance. The input impedance to the second stage varies from R6 at maximum volume to R6 + R_v at minimum volume. Adjustment of R_v, therefore, varies the loading on the preceding tone-control circuit. The circuit shown in Fig. 353 exhibits less bass boost at maximum volume than at lower levels, as does the circuit in Fig. 352. To maintains bass boost at higher levels, it is necessary to scale the impedances of the tone-control circuit to lower values.

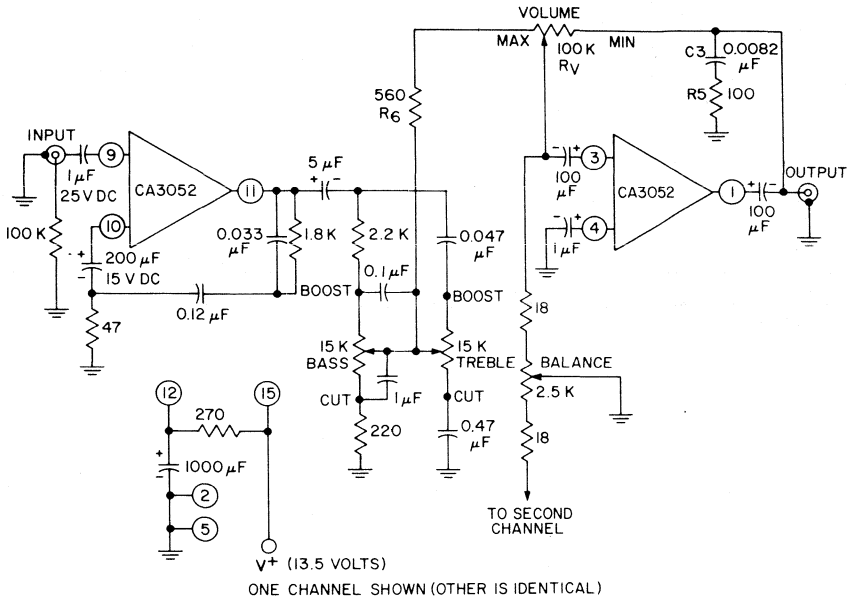
At minimum volume, the feedback-volume-control circuit effectively places the noise source for the second stage at the output of the preamplifier. Under these conditions, the source resistance seen by the power amplifier is reduced.

The feedback-volume-control circuit requires a special taper on the volume-control potentiometer. A linear taper acts rather like a switch in that it provides very little volume



All resistance values in ohms unless otherwise specified.

Fig. 352 — One channel of a complete stereo preamplifier in which the locations of the tone and level controls have been reversed from those in the preamplifier shown in Fig. 351.



All resistance values in ohms unless otherwise specified.

Fig. 353 — One channel of a complete stereo preamplifier that employs feedback volume control.

as the control is rotated up to about 90 per cent of its rotation. The level then rises very quickly to maximum. The correct taper is a counterclockwise logarithmic type, i.e., one in which the rate of change of resistance is very fast at first, and then slows down as maximum rotation is approached.

Musical Instruments

The four independent amplifiers of the CA3048 or CA3052 make possible simple designs for circuits normally used in electronic musical instruments.

Tone Generator—The tone-generation system for musical instruments may be a system of oscillators and frequency dividers designed for particular characteristics. The oscillators should be stable and tunable; each frequency divider is then phased-locked to its synchronizing source so that its output is exactly one-half the synchronizing frequency. As each divider is added, another tone is generated which is one octave below the input frequency. It is desirable for each element of the string to exhibit an identical waveform, which is rich in harmonics. The tones may then be mixed and passed through various filters so that different frequency bands are passed to the power amplifier to provide a variety of tonal colors.

Fig. 354 shows the CA3048 or CA3052 connected as a tone generator for an electronic organ. Amplifier A3 is connected as a Hartley oscillator, with its frequency governed by the relationship $\omega_0 = 1/(L1C1)^{1/2}$.

Amplifiers A1, A2, and A4 are set up as astable multivibrators. The

period of A4 is made somewhat longer than one-half the period of A3 by timing capacitor C3. Capacitor C2 provides a synchronizing signal to amplifier A4 by triggering A4 before its natural period is completed. In similar fashion, amplifier A4 provides a synchronizing signal to amplifier A1 by means of capacitor C4, and to amplifier A2 by means of capacitor C5.

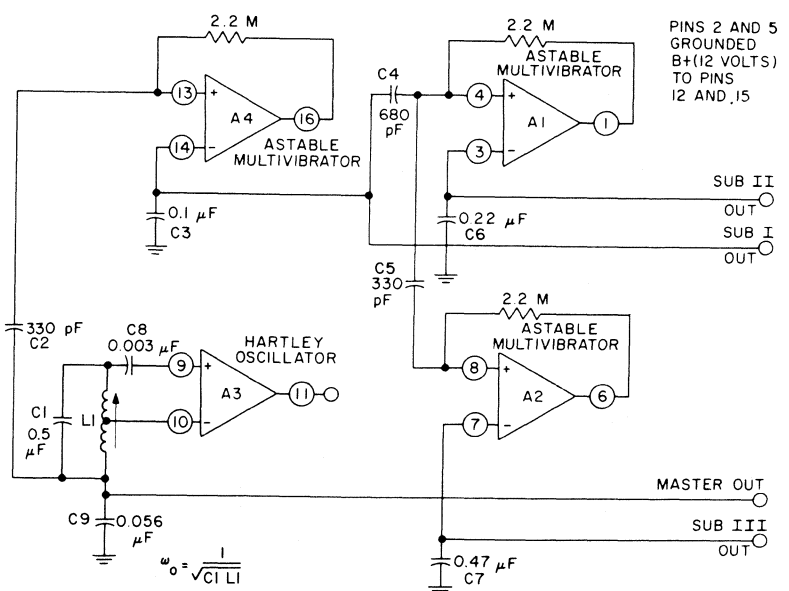
Outputs are taken from the timing capacitors C3, C6, and C7 in the multivibrators, and from the integrating capacitor C8 in the master oscillator. In each case, a triangular waveform, approximately 200 millivolts peak-to-peak, is obtained.

Twelve generators of this type would constitute the tone-generation system for a four octave electronic organ.

Tremolo—Tremolo is widely used in musical-instrument amplifiers to create effects which add to the capability of the instrument itself. It is a musical effect characterized by a sub-audio modulation of the musical tone. When amplitude modulation is used, it is called tremolo; a frequency-modulation effect is termed vibrato.

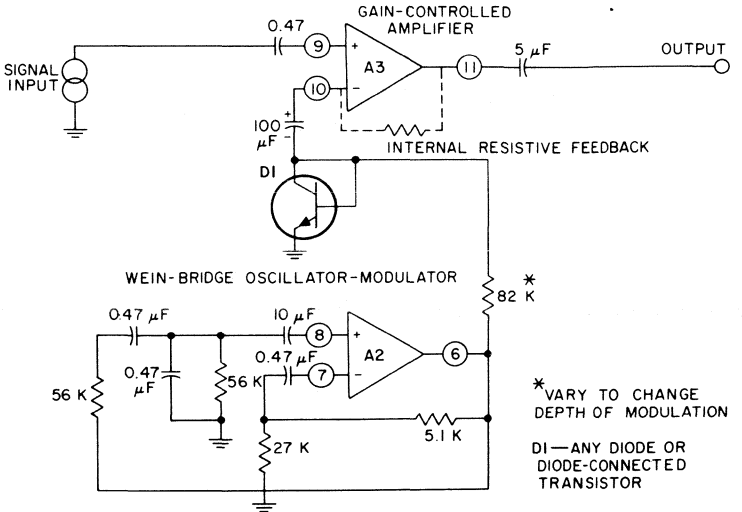
If a variable impedance is connected in the feedback loop of the CA3048 or CA3052, it is possible to vary its gain by a modulating signal. This feature is used in the circuit shown in Fig. 355.

Amplifier A2 is connected as a Wien-bridge oscillator that operates at about 6 Hz. Amplifier A3 is operated as a voltage amplifier with a variable impedance between the inverting input and ground. The resistors internal to the CA3048 or CA3052 chip, in combination with the variable impedance, control the gain. The output of the Wien-bridge



All resistance values in ohms unless otherwise specified.

Fig. 354 — Tone-generator circuit.



All resistance values in ohms unless otherwise specified.

Fig. 355 — Tremolo circuit.

oscillator is coupled directly into the variable impedance to vary the gain at a 6-Hz rate to produce the tremolo effect. The variable impedance may be either a diode (or a diode-connected transistor) or an MOS transistor in which the source-to-drain impedance is varied by variation of the gate bias.

VOLTAGE REGULATOR

The RCA-CA3055 is a silicon monolithic integrated circuit designed specifically for service as a voltage regulator. The circuit is supplied in an 8-terminal TO-5-style package and operates over a temperature range of −55°C to +125°C. It can deliver output currents up to 100 milliamperes without the use of external pass transistors. A block diagram of the CA3055, shown in Fig. 356, indicates the terminal connections which provide access to the temperature-compensated reference voltage (terminal 5), booster input (terminal 2), frequency compensation (terminal 7), and short-circuit protection (terminal 1).

The CA3055 can be used in conjunction with any suitable external pass transistor to provide voltage regulation at load currents greater than 100 milliamperes.

Fig. 357 shows the schematic diagram for the CA3055. The CA3055 can handle input voltages from 7.5 to 40 volts and provide adjustable voltage from 1.8 to 34 volts.

Dynamic Characteristics

The CA3055 has an equivalent noise output voltage of 0.7 millivolt (typical) for a reference capacitance of zero and of 0.45 millivolt for a reference capacitance of 0.22 microfarad. Fig. 358 shows the test circuit for the noise-voltage measurements.

The input or line regulator for the CA3055, as measured in the test circuit shown in Fig. 359, is 45 dB minimum for a reference capacitance of 2 microfarads. Output re-

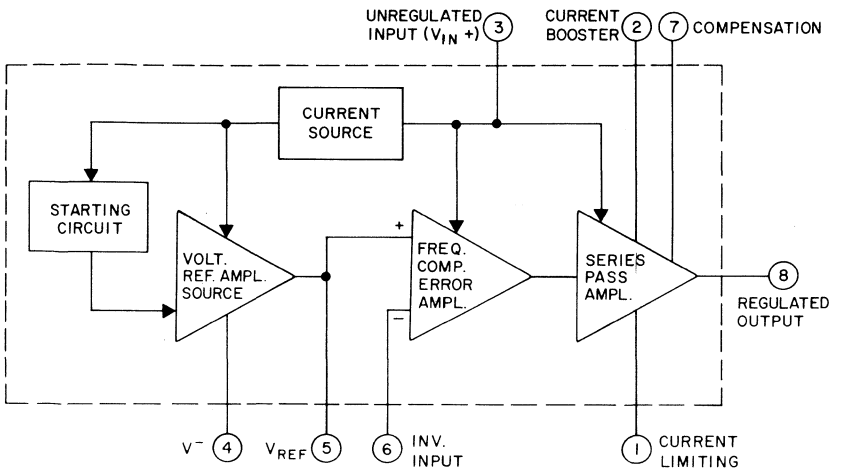
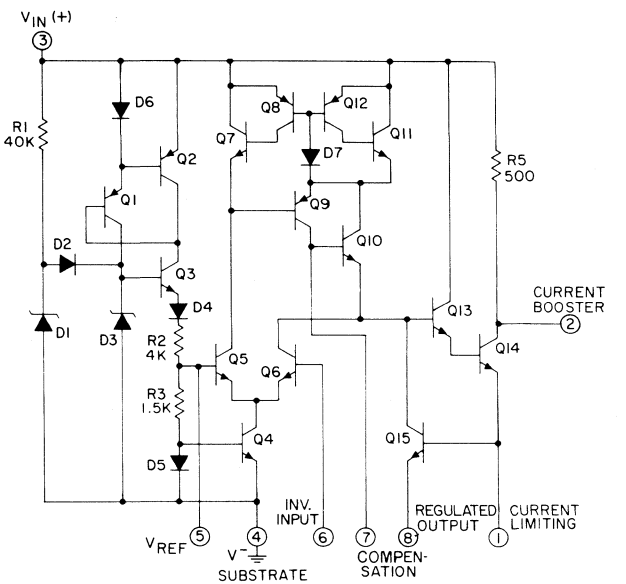
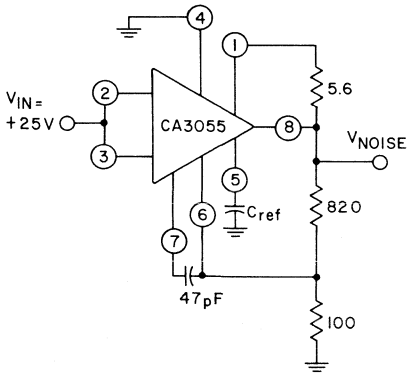


Fig. 356 — Block diagram of the CA3055 integrated-circuit voltage regulator.



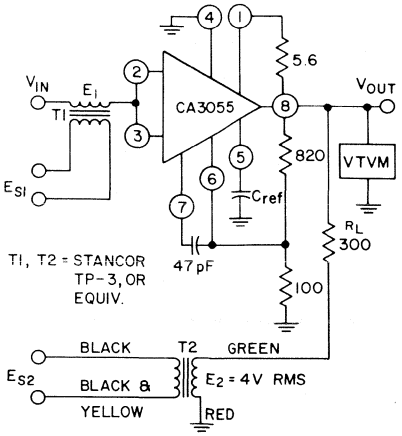
All resistance values in ohms unless otherwise specified.

Fig. 357 — CA3055 integrated-circuit voltage regulator.



All resistance values in ohms unless otherwise specified.

Fig. 358 — Test circuit for noise voltage (V_{noise}).



All resistance values in ohms unless otherwise specified.

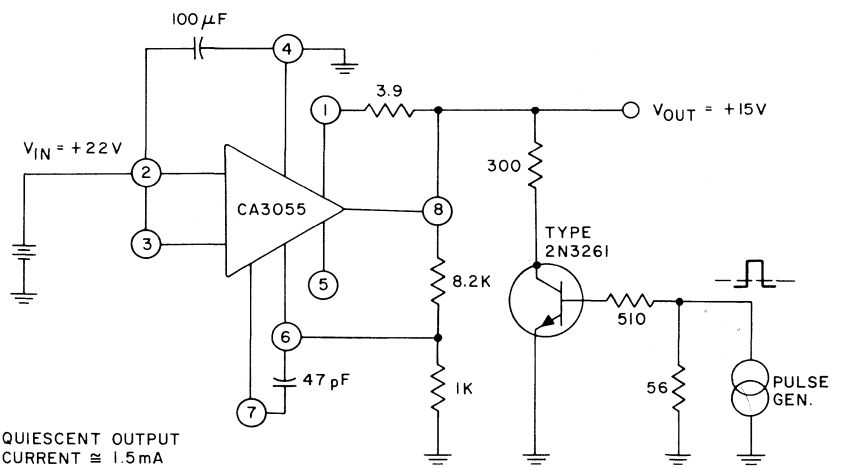
Fig. 359 — Test circuit for input regulation and output resistance.

sistance at 1 kHz is 0.3 ohm maximum.

Transient response of the CA3055 is 1 microsecond (typical) for turn-on time and 3 microseconds (typical) for the turn-off time. Fig. 360 shows the test circuit for these measurements, and Fig. 361 shows the turn-off and turn-on waveforms.

Applications

The CA3055 can be used as a shunt voltage regulator, a current regulator, a switching voltage regu-



All resistance values in ohms unless otherwise specified.

Fig. 360 — Turn-on and turn-off recovery time test circuit.

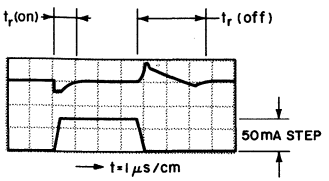


Fig. 361 — Turn-on and turn-off recovery time waveforms.

lator, and a high-current voltage regulator. Fig. 362 shows the CA3055 in a high-current voltage regulator circuit. The application of the CA3055 in a typical power supply is shown in Fig. 363.

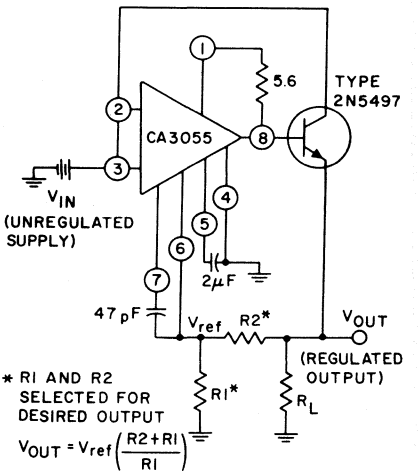
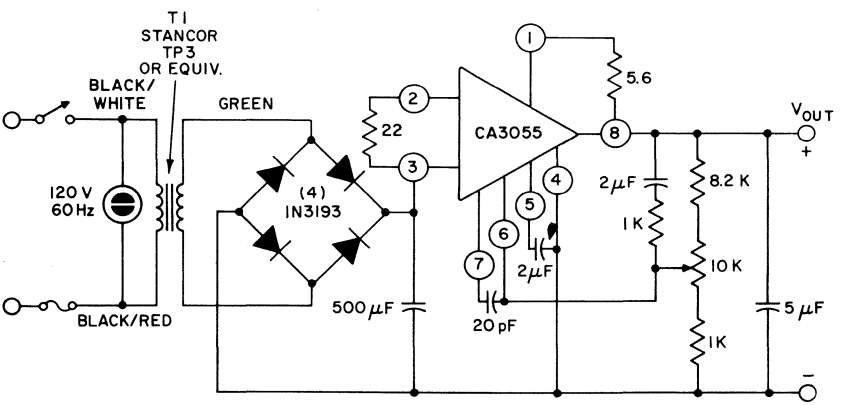


Fig. 362 — High-current voltage regulator circuit.

PHOTODETECTOR AND POWER AMPLIFIER

The RCA CA3062 integrated circuit consists of a photosensitive section and a power amplifier on a single monolithic silicon chip in a modified TO-5-style package. The single chip includes a photosensitive element consisting of two photosensitive Darlington pairs connected in parallel and a power amplifier element having two outputs. The CA3062 can be connected as an amplifier to provide a linear output or



V_{OUT} = 3.5 V TO 20 V (0 TO 90 mA)
REGULATION = 0.2% (LINE AND LOAD)
RIPPLE < 0.2 mV AT FULL LOAD

All resistance values in ohms unless otherwise specified.

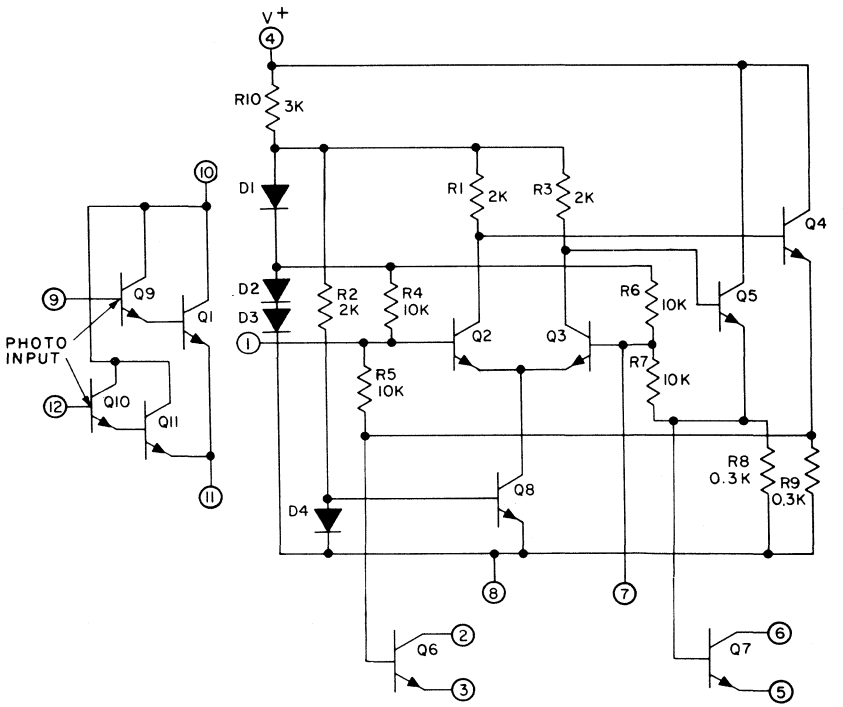
Fig. 363 — Application of the CA3055 in a typical power supply.

it can be connected to an "on-off" output. One output terminal energizes a load in the presence of light and the other output terminal energizes a load in the absence of light. This flexible arrangement, with its high output-current capabilities, provides the user with a complete system particularly useful in a wide range of photoelectric control applications. Fig. 364 shows the schematic diagram for the CA3062.

Operating Considerations

The CA3062 can be connected as an amplifier to provide a linear output or it can be connected to provide an "on-off" output. Optimum operation in this device is achieved when the load current is in a total ON-state or OFF-state condition. Intermediate values of load current between these ON and OFF states cause power to be dissipated in the silicon chip. The heat rise in the silicon chip induced by the power dissipation causes the load current to shift in the same direction as though additional illumination were applied to the device. The maximum intensity of illumination should be adjusted so that the signal-input-voltage rating of 3 volts is not exceeded.

If the load impedance is inductive, as in a relay, a diode should be connected across the load to absorb the energy of the pulse voltages generated during switching. When the CA3062 is connected to provide a linear output, the value of the load resistance should be greater than 1000 ohms.



All resistance values in ohms unless otherwise specified.

Fig. 364 — CA3062 integrated-circuit photodetector and power amplifier.

The CA3062 can operate from dc supply voltages to +9 volts and has an output-current capability of 100 milliamperes. A relay can be directly driven by the CA3062. Figs. 365 through 372 show typical characteristics of the CA3062.

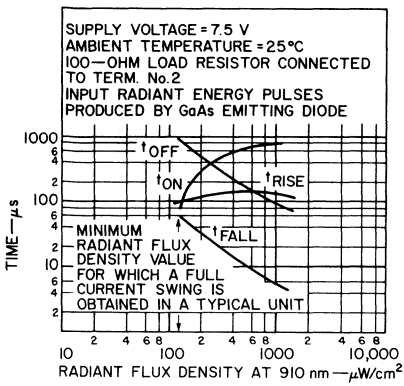


Fig. 365 — Response time as a function of radiant flux density.

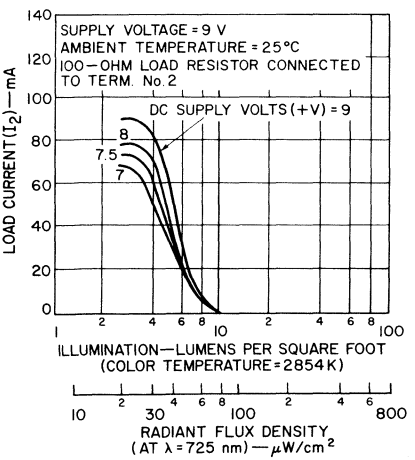


Fig. 366 — Load current I_2 as a function of illumination for different supply voltages.

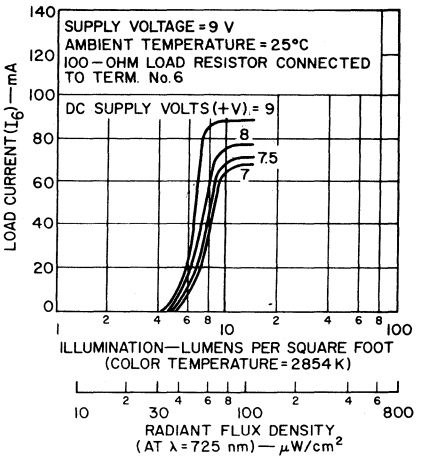


Fig. 367 — Load current I_6 as a function of illumination for different supply voltages.

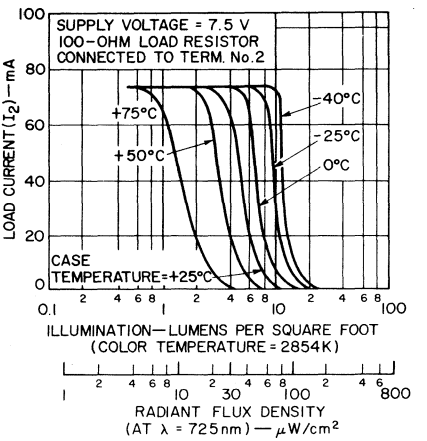


Fig. 368 — Load current I_2 as a function of illumination for different case temperatures.

Applications

The CA3062 is useful in various applications such as edge-monitoring systems, vending-machine systems, ON-OFF control applications, and photoelectric keyboards. Fig. 373 shows the application of the CA3062

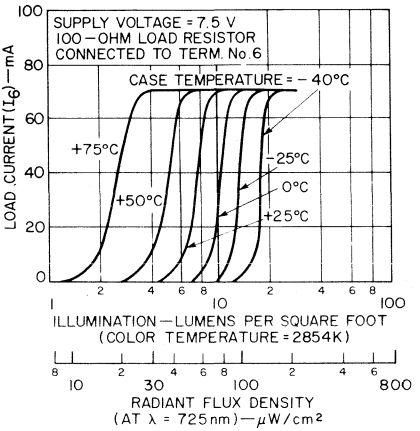


Fig. 369 — Load current I_6 as a function of illumination for different case temperatures.

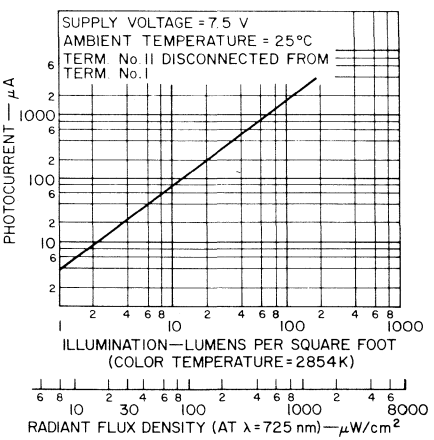


Fig. 371 — Photocurrent as a function of illumination.

in an ON-OFF photoelectric control circuit. Fig. 374 shows a circuit diagram that illustrates the use of the CA3062 in linear-output photoelectric applications.

POWER-CONTROL CIRCUIT

The RCA-CA3059 zero-voltage switch is a monolithic integrated circuit used primarily as a trigger circuit

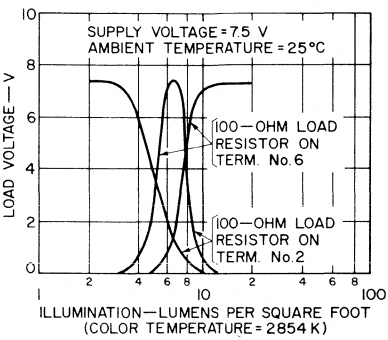


Fig. 370 — Load voltage as a function of illumination for various load-resistance values.

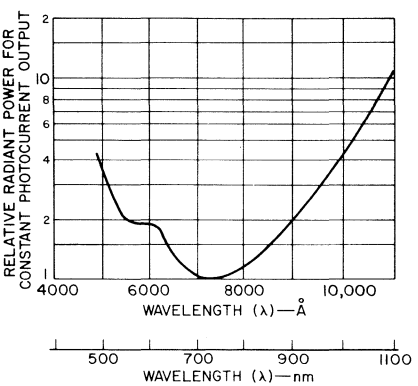
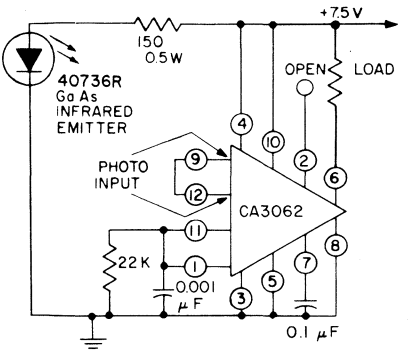


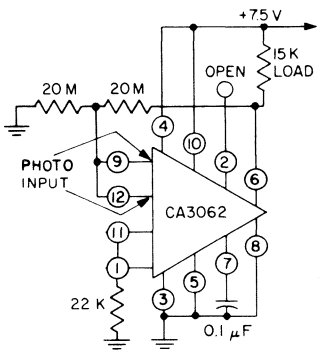
Fig. 372 — Typical spectral response of the photosensitive Darlington unit.

for the control of thyristors. This multistage circuit employs a diode limiter, a threshold detector, a differential amplifier, and a Darlington output driver to provide the basic switching action. The dc supply voltage for these stages is supplied by an internal zener-diode-regulated power supply that has sufficient current capability to drive external circuit elements, such as transistors and other integrated circuits. An important feature of the CA3059 is that the trigger pulses developed by this circuit can be applied directly



All resistance values in ohms unless otherwise specified.

Fig. 373 — Circuit diagram for "ON-OFF" photoelectric control applications.



All resistance values in ohms unless otherwise specified.

Fig. 374 — Circuit diagram for linear-output photoelectric applications.

to the gate of a silicon controlled rectifier (SCR) or a triac. A built-in fail-safe circuit inhibits the application of these pulses to the thyristor gate circuit in the event that the external sensor for the integrated-circuit switch should be inadvertently opened or shorted.

The CA3059 is particularly suited for use in thyristor temperature-control applications. The integrated circuit may be employed as either an on-off type of controller or a proportional controller, depending upon the degree of temperature regulation required. The availability of numerous terminal connections to internal circuit points greatly increases the flexibility of the CA3059 and permits the circuit designer to exercise his creativity to employ the integrated switch in unique ways. The circuit is supplied in a 14-terminal dual-in-line plastic package and operates over a temperature range of 0°C to +70°C.

Circuit Operation

Fig. 375 shows a functional block diagram of the CA3059 integrated-circuit zero-voltage switch. Any triac that is driven directly from the output terminal of this circuit should be characterized for operation in the I(+) or III(+) triggering modes, i.e., with positive gate current (current flows into the gate for both polarities of the applied ac voltage). The circuit operates directly from a 60-Hz ac line voltage of 120 or 240 volts.

The limiter stage of the CA3059 clips the incoming ac line voltage to approximately plus and minus 8 volts. This signal is then applied to the zero-voltage-crossing detector, which generates an output pulse during each passage of the line voltage through zero. The limiter output is also applied to a rectifying diode and an external capacitor that comprise the dc power supply. The power supply provides approximately 6 volts as the V+ supply to the other stages of the CA3059. The on/off sensing amplifier is basically a differential comparator. The triac gating circuit contains a driver for direct triac triggering. The gating circuit is enabled when all the inputs are at a high voltage, i.e., the line voltage must be approximately zero volts,

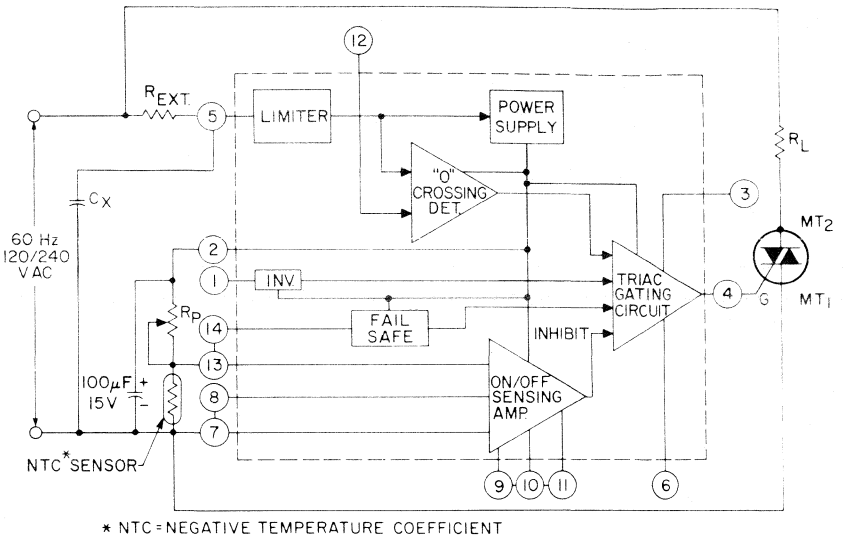


Fig. 375 — Functional block diagram of the CA3059 integrated-circuit zero-voltage switch.

the sensing-amplifier output must be "high," the external voltage to terminal 1 must be a logical "1," and the output of the fail-safe circuit must be "high."

Fig. 376 shows the circuit diagram of the CA3059. The zero-voltage threshold detector consists of diodes D3, D4, D5, and D6, and transistor Q1. The differential amplifier consists of transistor pairs Q2-Q4 and Q3-Q5. Transistors Q1, Q6, Q7, Q8, and Q9 comprise the triac gating circuit and driver stage. Diode D12, zener diode D15, and transistor Q10 constitute the fail-safe circuit. The power supply consists of diodes D7 and D13 and an external resistor and capacitor connected to terminals 5 and 2, respectively, and to ground through pin 7. If the transistor pair Q2-Q4 and transistor Q1 are turned off, an output appears at terminal 4. Transistor Q1 is in the OFF state if the incoming line voltage is less than approximately the voltage drops across three silicon diodes (2.1 volts) for either the positive or negative excursion of the line voltage. Transistor pair Q2-Q4 is OFF if the voltage across the sensor, connected from terminals 13 to 7, exceeds the reference voltage from terminals 9 to 7. If either of these conditions is not satisfied, pulses are not supplied to terminal 4. Fail-safe operation requires that terminal 13 be connected to 14. The addition of hysteresis and elimination of half-cycling can be obtained by a resistive voltage divider connected from 13 to 8 and from 8 to 7.

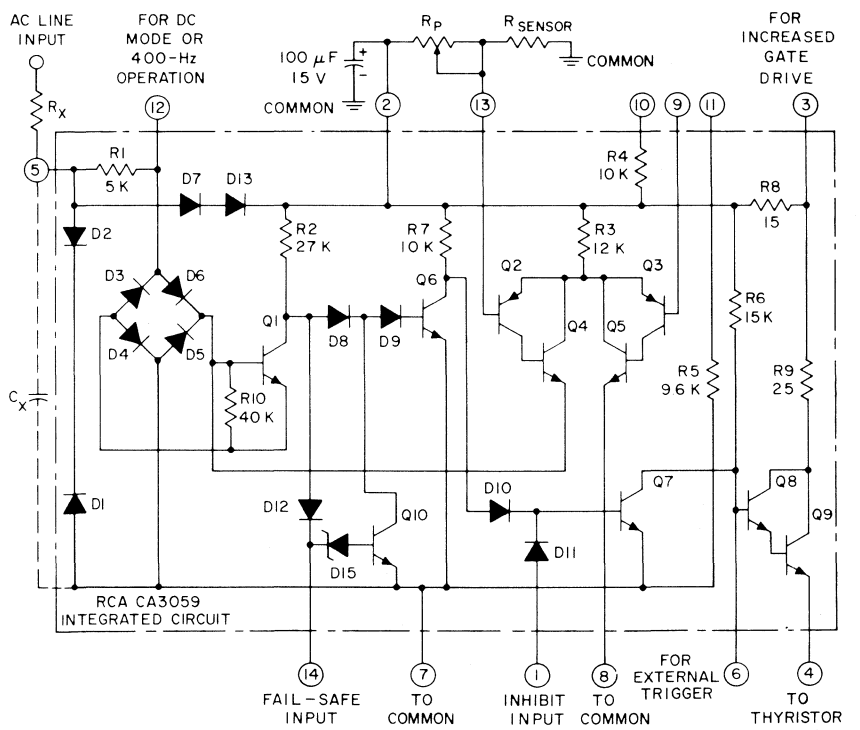
Fig. 377 shows the position and width of the pulses supplied to the gate of a thyristor with respect to the incoming ac line voltage. The CA3059 can supply sufficient gate voltage and current to trigger most RCA thyristors at ambient temperatures of 25°C. *However, under worst-case conditions (i.e., at ambient temperature extremes and maximum*

triggering requirements), selection of the higher-current thyristors may be necessary for particular applications. For example, the RCA-2N5444 40-ampere triac has a maximum gate trigger voltage V_{gt}(max) of 2.5 volts and a maximum gate trigger current I_{gt} (max) of 80 milliamperes in the III(+) quadrant at 25°C. Because the CA3059 cannot guarantee a drive of 80 milliamperes for a V_{gt} of 2.5 volts, triac selection will be required.

Effect of CA3059 on Thyristor Load Characteristics

The CA3059 is designed primarily to gate a thyristor that switches a resistive load. Because the output pulse supplied by the CA3059 is of short duration, the latching current* of the triac becomes a significant factor in determining whether other types of loads can be switched. (The latching-current value determines whether the triac will remain in conduction after the gate pulse is removed.) Provisions are included in the CA3059 to accommodate inductive loads and low-power loads. For example, for loads that are less than approximately 4 amperes rms or that are slightly inductive, it is possible to retard the output pulse with respect to the zero-voltage crossing by

* The latching current is the minimum current required to sustain conduction immediately after the thyristor is switched from the OFF to the ON state and the gate signal is removed.



All resistance values in ohms unless otherwise specified.

Fig. 376 — Circuit diagram for the CA3059 zero-voltage switch.

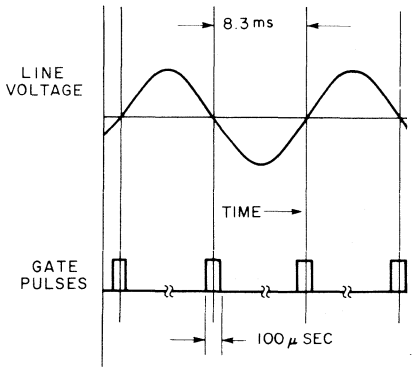


Fig. 377 — Timing relationship between the output pulses of the CA3059 and the ac line voltage.

insertion of the capacitor C_x from terminal 5 to terminal 7, as shown in Fig. 375. The insertion of capacitor C_x permits switching of triac loads that have a slight inductive component and that are greater than approximately 200 watts (for operation from an ac line voltage of 120 volts rms). However, for loads less than 200 watts (for example, 70 watts), it is recommended that the user employ the RCA-40526 sensitive-gate triac with the CA3059 because of the low latching-current requirement of this triac.

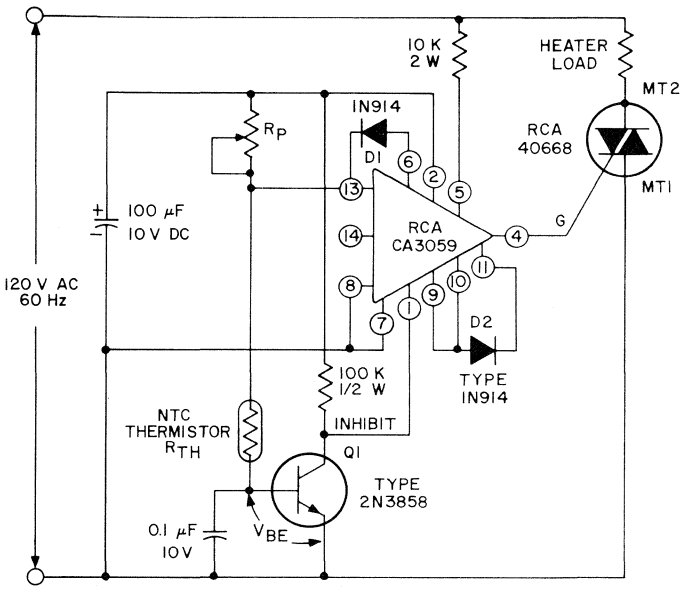
For loads that have a low power factor, such as a solenoid valve, the user may operate the CA3059 in the dc mode. In this mode, terminal 12 is connected to terminal 7, and the zero-crossing detector is inhibited. Whether a "high" or "low" voltage is produced at terminal 4 is then dependent only upon the state of the differential comparator within the CA3059 integrated circuit, and not upon the zero crossing of the incoming line voltage. Of course, in this mode of operation, the CA3059 no longer operates as a zero-voltage switch. However, for many applications that involve the switching of low-current inductive loads, the amount of radio-frequency interference (RFI) generated can frequently be tolerated.

For switching of high-current inductive loads, which must be turned on at zero line current, the triggering technique employed in the dual-output over-under temperature controller and the transient-free switch controller, described later (see Figs. 387, 399, and 400), is recommended.

Fail-Safe Feature

As shown in Figs. 375 and 376, when terminal 13 is connected to terminal 14, the fail-safe circuit of the CA3059 is operable. If the sensor should then be accidentally opened or shorted, power is removed from the load (i.e., the triac is turned OFF). The internal fail-safe circuit functions properly, however, only when the ratio of the sensor impedance at 25°C, if a thermistor is the sensor, to the impedance of the potentiometer R_p is less than 4 to 1. It is readily apparent that, if the potentiometer is adjusted for 1000 ohms and the sensor is 100,000 ohms, the zener diode D15 (shown in Fig. 376) would conduct because virtually all the dc power-supply voltage (from terminal 2 to terminal 7) would appear across the sensor. The CA3059 would then detect this condition as an open sensor.

For ratios greater than 4 to 1, for example 100 to 1, the circuit shown in Fig. 378 may be employed to provide fail-safe operation. In this circuit, transistor Q1 and diode D1 are components external to the CA3059. Transistor Q1 detects the sensor current which maintains this transistor in saturation so that terminal 1 is effectively shorted to terminal 7 through the collector-to-emitter junction of the transistor. Transistor Q1 provides sufficient current gain to permit operation with a sensor



All resistance values in ohms unless otherwise specified.

Fig. 378 — CA3059 on-off controller that uses an external fail-safe circuit.

impedance greater than 1 megohm. If the sensor becomes open-circuited, transistor Q1 turns OFF, and current then flows into terminal 1, the inhibit terminal of the CA3059, and results in the removal of power to the load. For the shorted-sensor condition, the external diode D1 conducts and causes triac Y1 to turn OFF. Diode D2 compensates for variations in the base-to-emitter voltage of transistor Q1 with temperature. Terminals 13 and 14 on the CA3059 should not be connected when the external fail-safe circuit shown in this illustration is employed.

Half-Cycling and Hysteresis Characteristics

The method by which the CA3059 senses the zero crossing of the ac power results in a half-cycling phenomenon at the control point. Fig. 379 illustrates this phenomenon. The

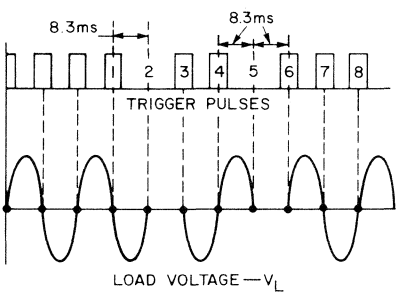


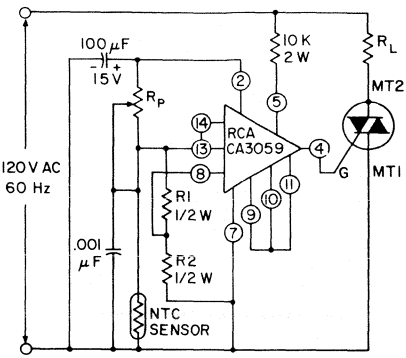
Fig. 379 — Half-cycling phenomenon in the CA3059.

CA3059 senses the zero-voltage crossing every half-cycle and an output, for example pulse No. 4, is produced to indicate the zero crossing. During the remaining 8.3 milliseconds, however, the differential amplifier in the CA3059 may change state and inhibit any further output pulses. The uncertainty region of the differential amplifier, therefore, prevents pulse No. 5 from triggering the triac

during the negative excursion of the ac line voltage.

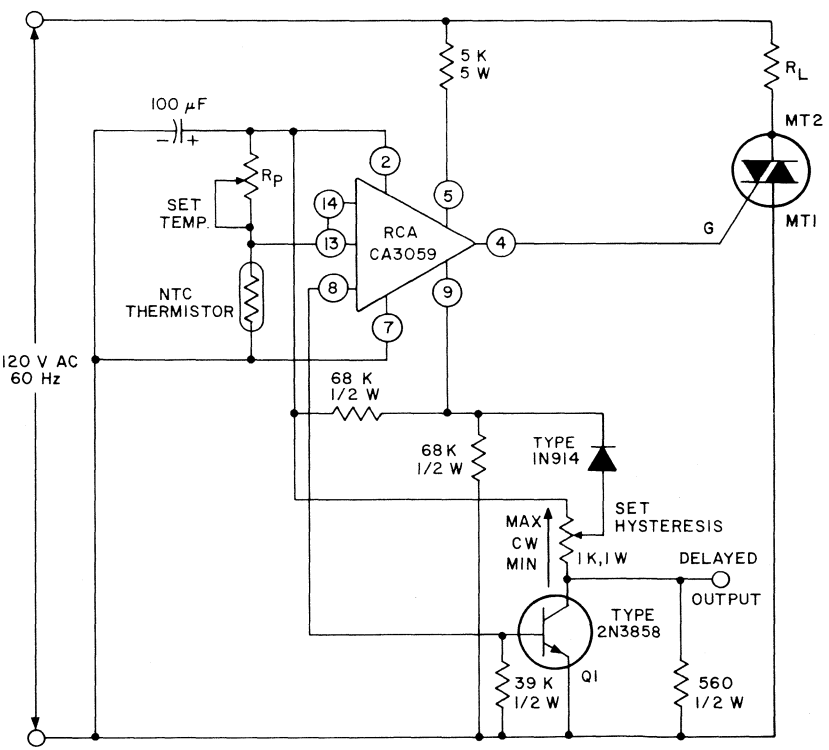
Several solutions exist for elimination of the half-cycle phenomenon. If the user can tolerate some hysteresis in the control, then positive feedback can be added around the differential amplifier. Fig. 380 illustrates this technique. The tabular data in the figure lists the recommended values of R1 and R2 for different sensor impedances at the control point.

If a significant amount (greater than ±10%) of controlled hysteresis is required, then the circuit shown in Fig. 381 may be employed. In this configuration, external transistor Q1 provides a means for addition of positive feedback to the CA3059. It



THERMISTOR →	NTC	R1	R2
	5 K	12 K	12 K
	12 K	68 K	12 K
	100 K	200 K	18 K

Fig. 380 — CA3059 on-off controller with hysteresis.



All resistance values in ohms unless otherwise specified.

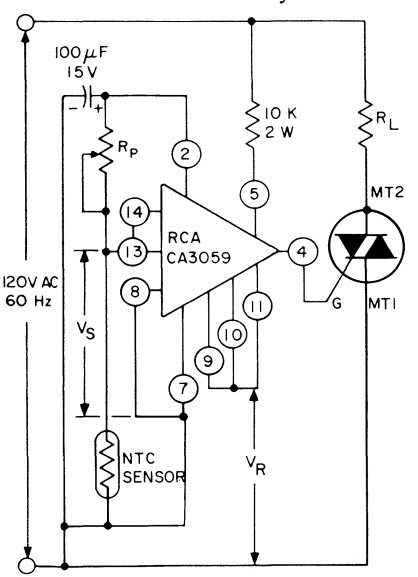
Fig. 381 — CA3059 on-off controller with controlled hysteresis.

should be noted that the signal developed at the collector to Q1 could perhaps be used to provide an auxiliary time-delay function.

For applications which require complete elimination of half-cycling without the addition of hysteresis, the *integral-cycle* temperature controller (described later in this section), which senses the zero-voltage crossing only once during the ac power cycle, can be used.

Temperature Controllers

Fig. 382 shows a triac used in an on-off temperature-controller configuration. The triac is turned on at zero voltage whenever the voltage V_s exceeds the reference voltage V_r. The transfer characteristic of this system, shown in Fig. 383(a), indicates significant thermal overshoots and undershoots, a well known characteristic of such a system. The



All resistance values in ohms unless otherwise specified.

Fig. 382 — CA3059 on-off temperature controller.

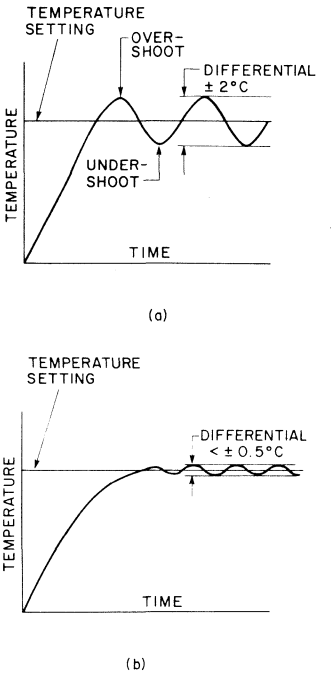


Fig. 383 — Transfer characteristics of (a) on-off and (b) proportional control systems.

hysteresis of this system, however, can be further increased, if desired, by the addition of positive feedback.

For precise temperature-control applications, the proportional-control technique with synchronous switching is employed. The transfer curve for this type of controller is shown in Fig. 383(b). In this case, the duty cycle of the power supplied to the load is varied with the demand for heat required and the thermal time constant (inertia) of the system. For example, when the temperature setting is increased in an "on-off" type of controller, full power (100-per-cent duty cycle) is supplied to the system. This effect results in significant temperature excursions *because there is no anticipatory circuit* to reduce the power

gradually before the actual set temperature is achieved. However, in a proportional control technique, less power is supplied to the load (reduced duty cycle) as the error signal is reduced (sensed temperature approaches the set temperature).

Before such a system is implemented, a time base is chosen so that the ON-time of the triac is varied within this time base. The ratio of the ON-to-OFF time of the triac within this time interval depends on the thermal time constant of the system and the selected temperature setting. Fig. 384 illustrates the principle of proportional control. For this operation, power is supplied to the load until the ramp voltage reaches a value greater than the dc control signal supplied to the opposite side of the differential amplifier. The triac then remains OFF for the remainder of the time-base period. As a result, power is "proportioned" to the load in a direct relation to the heat demanded by the system.

For this application, a simple ramp generator can be realized with a minimum number of active and passive components. It is noted that a

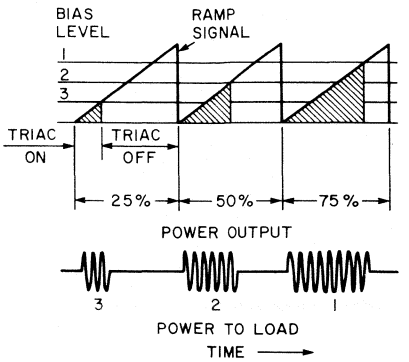


Fig. 384 — Principles of proportional control.

ramp having good linearity is not required for proportional operation because of the nonlinearity of the thermal system and the closed-loop type of control. In the circuit shown in Fig. 385, ramp voltage is generated when the capacitor C1 charges through resistors R0 and R1. The time base of the ramp is determined by resistors R2 and R3, capacitor C2, and the breakover voltage of the 1N5411 diac. When the voltage across C2 reaches approximately 32 volts, the diac switches and turns on the 2N3241A transistor. The capaci-

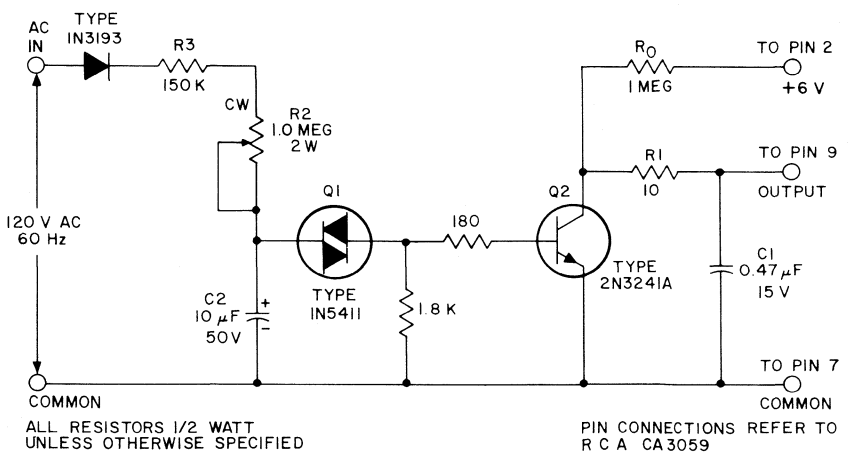
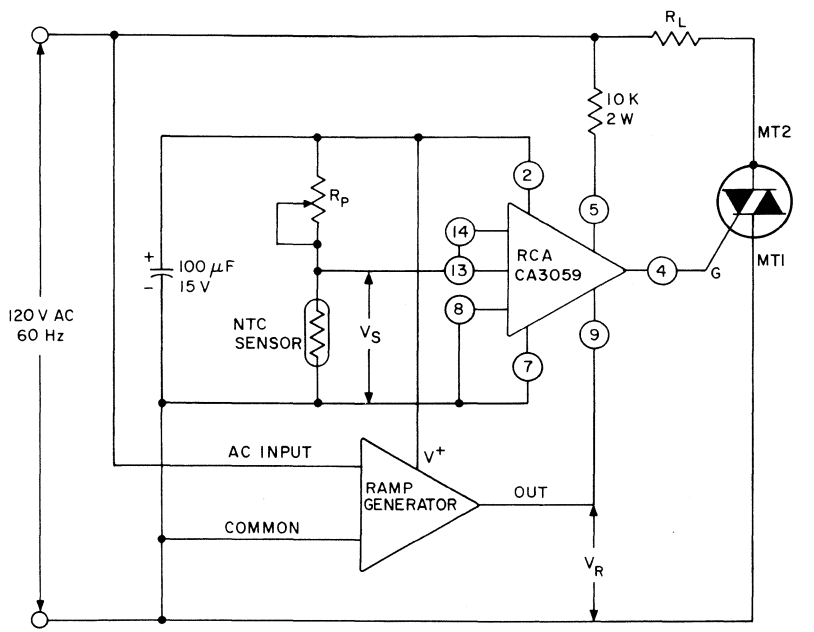


Fig. 385 — Ramp generator.

tor C1 then discharges through the collector-to-emitter junction of the transistor. This discharge time is the retrace or flyback time of the ramp. The circuit shown can generate ramp times ranging from 0.3 to 2.0 seconds through adjustment of R2. For precise temperature regulation, the time base of the ramp should be shorter than the thermal time constant of the system, but long with the respect to the period of the 60-Hz line voltage. Fig. 386 shows a triac connected for the proportional mode.

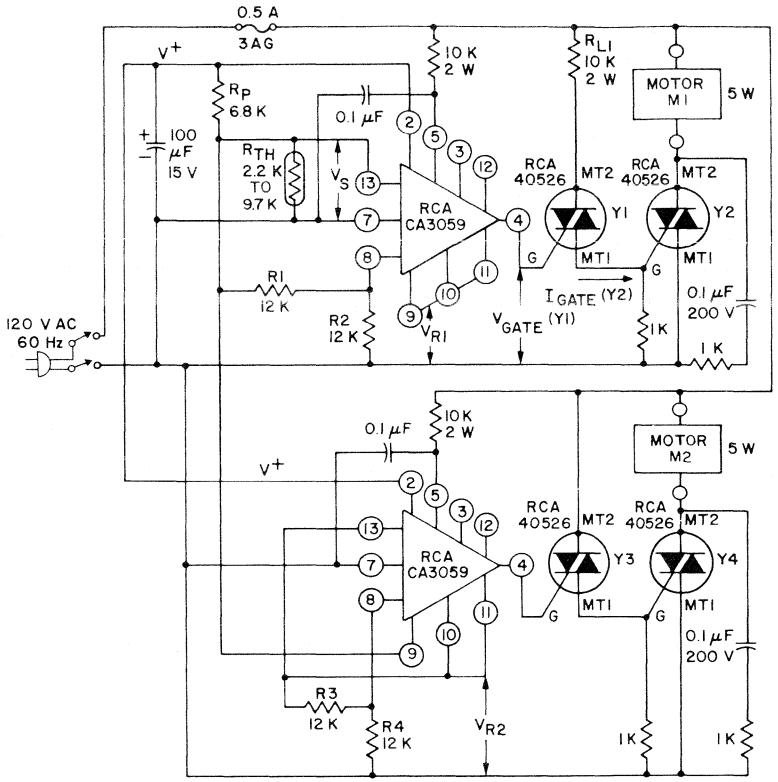
Fig. 387 shows a dual-output temperature controller that drives two triacs. When the voltage V_s developed across the temperature-sensing network exceeds the reference voltage V_{R1}, motor M1 turns on. When the voltage across the network drops below the reference voltage V_{R2}, M2 turns on. Because the motors are inductive, the currents I_{M1} and I_{M2} lag the incoming line voltage. The motors, however, are switched by the triacs at zero current, as shown in Fig. 388.

The problem of driving inductive loads such as these motors by the narrow pulses generated by the CA3059 circuit is solved by use of the sensitive-gate RCA-40526 triac. The high sensitivity of this device (3 milliamperes maximum) and low latching current (approximately 9 milliamperes) permit synchronous operation of the temperature-controller circuit. In Fig. 387, it is apparent that, although the gate pulse V_g of triac Y1 has elapsed, triac Y2 is switched on by the current through R_{L1}. The low latching current of the RCA-40526 triac results in dissipation of only 2 watts in R_{L1}, as op-



All resistance values in ohms unless otherwise specified.

Fig. 386 — CA3059 proportional temperature controller.



All resistance values in ohms unless otherwise specified.

Fig. 387 — Dual-output, over-under temperature controller using two CA3059 integrated-circuits.

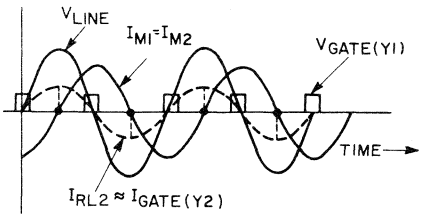


Fig. 388 — Voltage and current waveforms for the dual-output temperature controller.

posed to 10 to 20 watts when devices that have high latching currents are used.

Electric-Heat Application

For electric-heating applications, the RCA-2N5444 40-ampere triac and the CA3059 circuit constitute an optimum pair. Such a combination provides synchronous switching and effectively replaces the heavy-duty contactors which easily degrade as a result of pitting and wearout from the switching transients. The salient features of the 2N5444 40-ampere triac are as follows:

(1) 300-ampere single-surge capability (for operation at 60-Hz),

(2) a typical gate sensitivity of 20 milliamperes in the I(+) and III(+) modes,

(3) low ON-state voltage of 1.5 volts maximum at 40 amperes, and

(4) available V_{DROM} equal to 600 volts.

Fig. 389 shows the circuit diagram of a synchronous-switching heat-staging controller that is used for electric heating systems. Loads as heavy as 5 kilowatts are switched sequentially at zero voltage to eliminate RFI and prevent a dip in line voltage that would occur if the full 25 kilowatts were to be switched simultaneously.

Transistor Q1 is used as a constant-current source to charge capacitor C in a linear manner. Transistor Q2 acts as a buffer stage. When the thermostat is closed, a ramp voltage is provided at output E_o. At approximately 3-second intervals, each 5-kilowatt heating element is switched onto the power system by its respective triac. When there is no further demand for heat, the thermostat opens, and capacitor C discharges through R1 and R2 to cause each triac to turn OFF in the reverse heating sequence. It should be noted that some half-cycling occurs before the heating element is switched fully ON. This condition can be attributed to the inherent dissymmetry of the CA3059 and is further aggravated by the slow-rising ramp voltage ap-

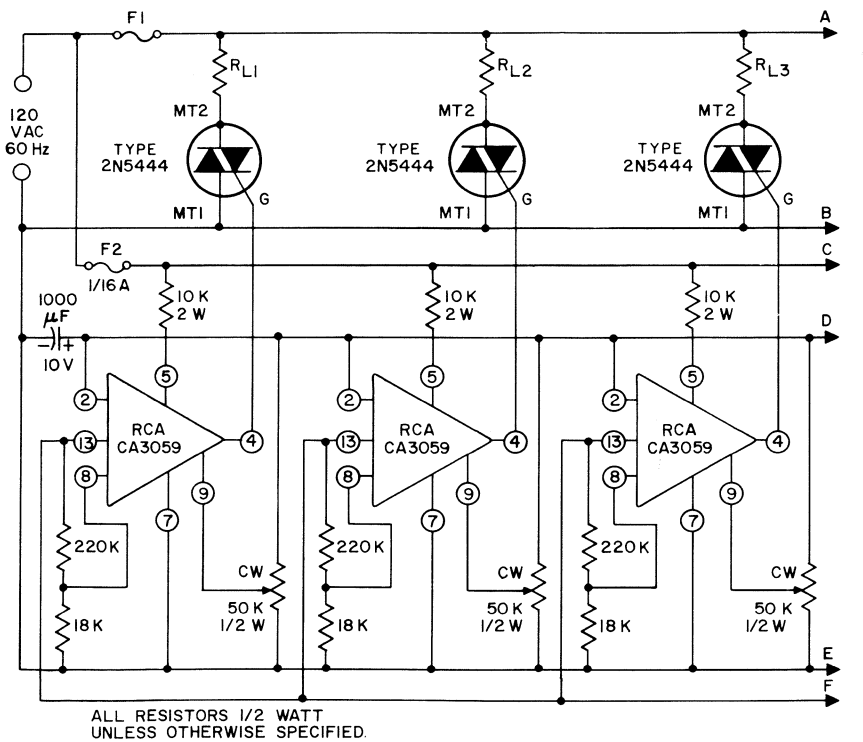
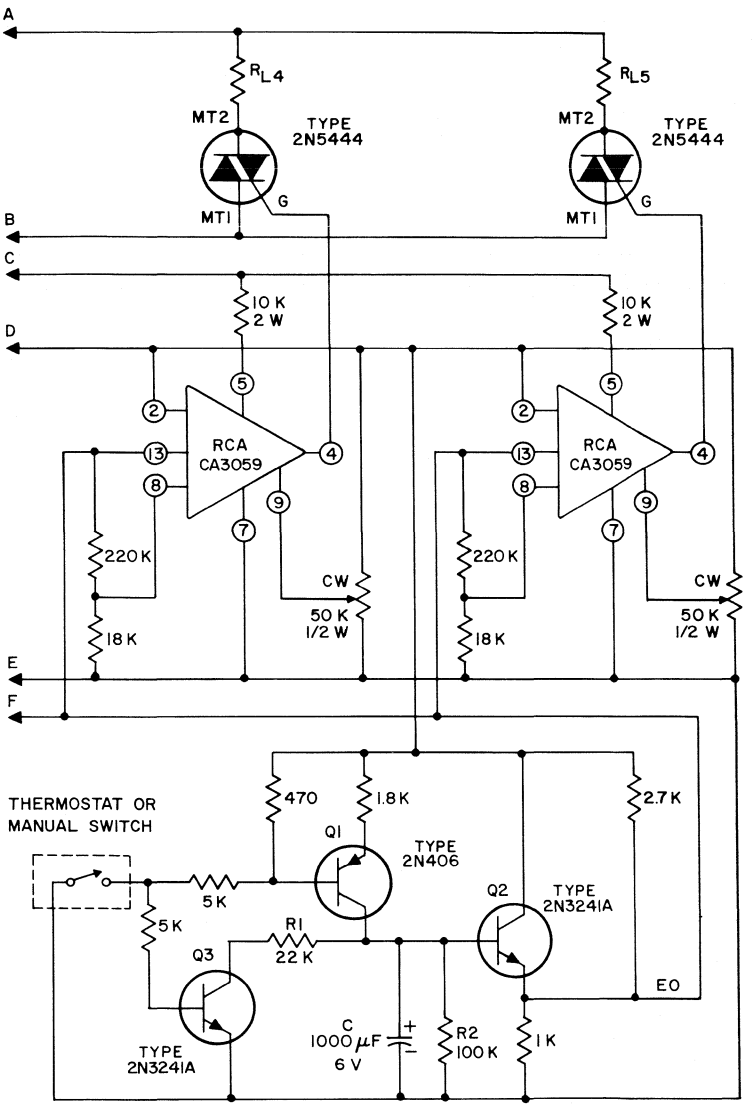


Fig. 389 — Synchronous-switching heat-staging controller using a series of CA3059 integrated circuits.

(Continued on page 301)



All resistance values in ohms unless otherwise specified.

Fig. 389 — Synchronous-switching heat-staging controller using a series of CA3059 integrated-circuits.
(Continued from page 300)

plied to one of the inputs. The timing diagram in Fig. 390 shows the turn-on and turn-off sequence of the heating system being controlled.

Seemingly, the basic method shown in Fig. 389 could be modified to provide proportional control in which the number of heating elements switched into the system, under any given thermal load, would be a function of the BTU's required by the system or the temperature differential between an indoor and outdoor sensor within the total system environment. That is, the closing of the thermostat would not switch in all the heating elements within a short time interval, which inevitably results in undesired temperature excursions, but would switch in only the number of heating elements required to satisfy the actual heat load.

Integral-Cycle Temperature Controller (No half-cycling)

If a temperature controller which is completely devoid of half-cycling and hysteresis is required, then the circuit shown in Fig. 391 may be used. This type of circuit is essential for applications in which half-cycling and the resultant dc component could cause overheating of a power transformer on the utility lines.

In the circuit shown in Fig. 391, the sensor is connected between terminals 7 and 9 of the CA3059. This arrangement is required because of the phase reversal introduced by SCR Y1. With this configuration, terminal 12 is connected to terminal 7 for operation of the CA3059 in the dc mode (however, the load is switched at zero voltage). Because the position of the sensor has been changed for this configuration, the internal fail-safe circuit cannot be used (terminals 13 and 14 are not connected).

In the integral-cycle controller, when the temperature being controlled is low, the resistance of the thermistor is high and an output signal at terminal 4 of zero volts is obtained. The SCR (Y1), therefore, is turned off. The triac (Y2) is then triggered directly from the line on positive cycles of the ac voltage. When Y2 is triggered and supplies power to the load R_L, capacitor C is charged to the peak of the input voltage. When the ac line swings negative, capacitor C discharges through the triac gate to trigger the triac on the negative half-cycle. The diode-resistor-capacitor "slaving network" triggers the triac on negative half-cycles of the ac input voltage after it is triggered on the positive half-cycle to provide only *integral cycles* of ac power to the load.

When the temperature being controlled reaches the desired value, as determined by the thermistor, then a positive voltage level appears at terminal 4 of the CA3059. The SCR then starts to conduct at the beginning of the positive input cycle to shunt the trigger current away from the gate of the triac. The triac is then turned OFF. The cycle repeats when the SCR is again turned OFF by the CA3059.

The circuit shown in Fig. 392 is similar to the configuration in Fig. 391 except that the fail-safe circuit incorporated in the CA3059 can be used. In this new circuit, the negative-temperature-coefficient (NTC) sensor is connected between terminals 7 and 13, and transistor Q_o inverts the signal output at terminal 4 to nullify the phase reversal introduced by the SCR (Y1). The internal power supply of the CA3059 supplies bias current to transistor Q_o.

Of course, the circuit shown in Fig. 392 can readily be converted to a *true proportional integral-cycle*

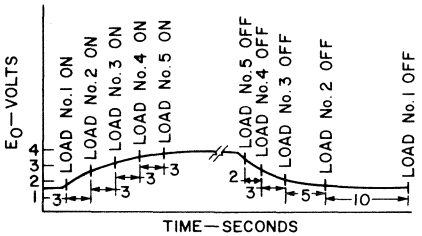


Fig. 390 — Ramp-voltage waveform for the heat-staging controller.

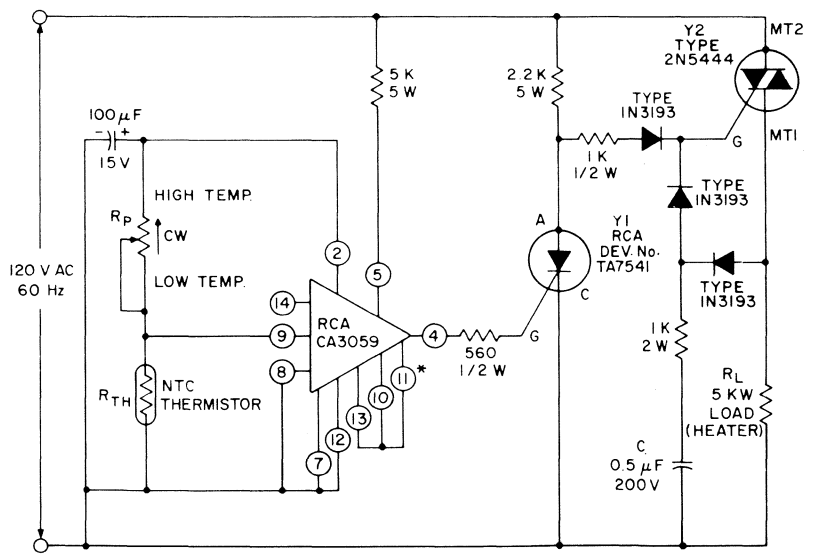
temperature controller simply by connection of a positive-going ramp voltage to terminal 9 (with terminals 10 and 11 open), as previously discussed.

Sensor Isolation

For some applications, electrical isolation of the sensor from the incoming ac power lines may be desired. Fig. 393 shows such a configuration. The pulse transformer T1 isolates the sensor from main terminal No. 1 of the triac Y1, and transformer T2 isolates the CA3059 from the power lines. Capacitor C1 shifts the phase of the output pulse at terminal 4 in order to retard the gate pulse delivered to triac Y1 to compensate for the small phase shift introduced by transformer T1.

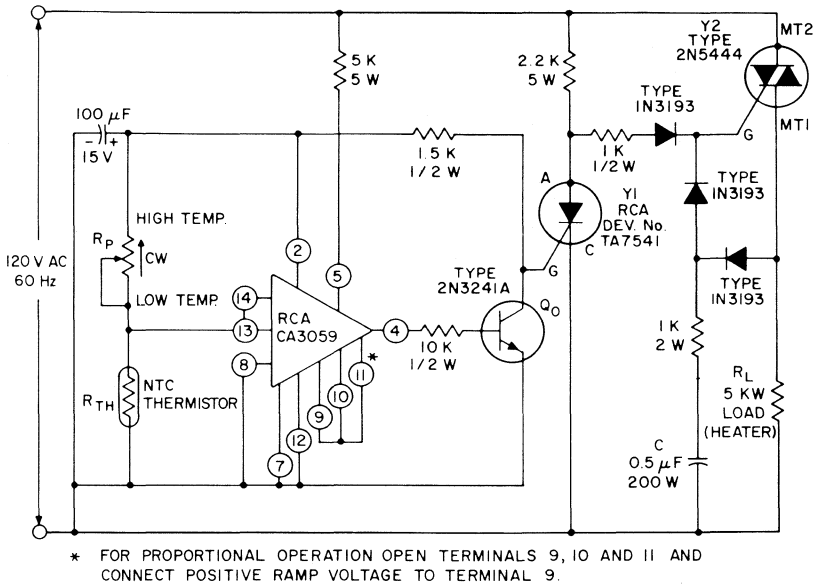
Differential Comparator for Industrial Use

Differential comparators have found widespread use as limit detectors which compare two analog input signals and provide a go/no-go, logic "one" or logic "zero" output, depending upon the relative magnitudes of these signals. Because the signals are often at very low voltage levels and very accurate discrimination is normally required between them, differential comparators in



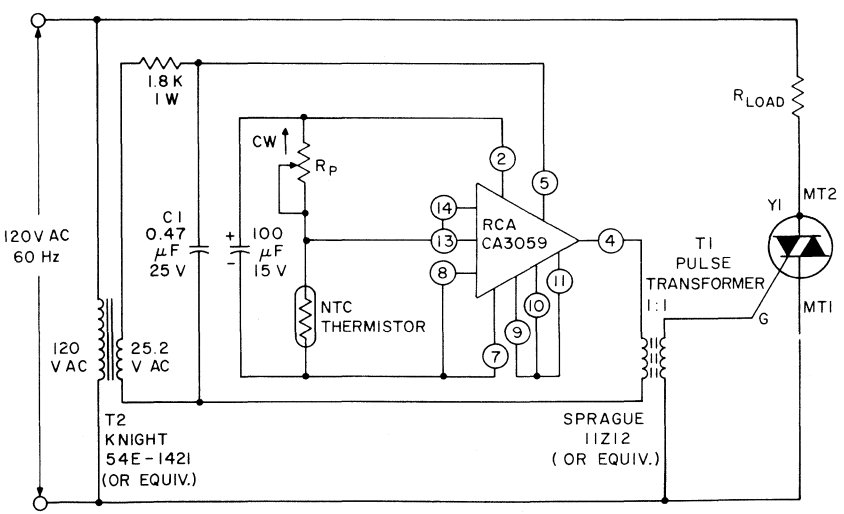
All resistance values in ohms unless otherwise specified.

Fig. 391 — CA3059 integral-cycle temperature controller in which half-cycling effect is eliminated.



All resistance values in ohms unless otherwise specified.

Fig. 392 — CA3059 integral-cycle temperature controller that features fail-safe operation and no half-cycling effect.



All resistance values in ohms unless otherwise specified.

Fig. 393 — CA3059 on-off controller with an isolated sensor.

many cases employ differential amplifiers as a basic building block. However, in many industrial control applications, a high-performance differential comparator is not required. That is, high resolution, fast switching speed, and similar features are not essential. The CA3059 is ideally suited for use in such applications. Connection of terminal 12 to terminal 7 inhibits the zero-voltage threshold detector of the CA3059, and the circuit becomes a differential comparator.

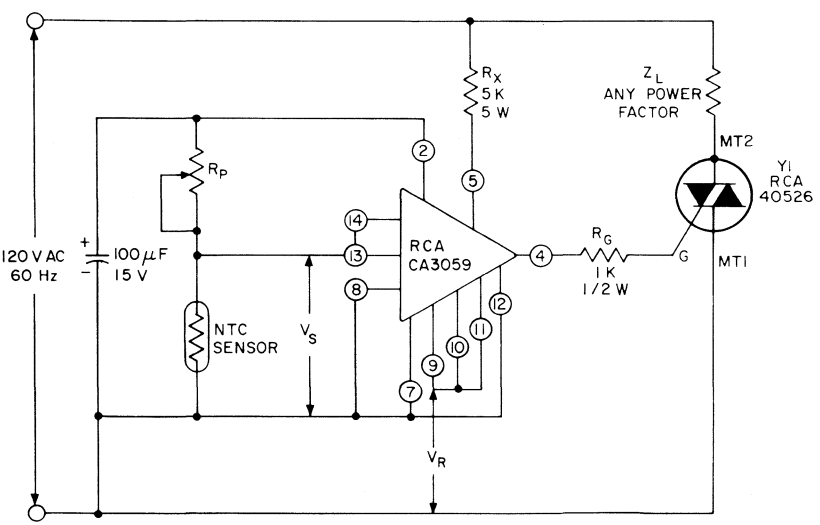
Fig. 394 shows the circuit arrangement for use of the CA3059 as a differential comparator. In this application, no external dc supply is required, as is the case with most commercially available integrated-circuit comparators; of course, the output-current capability of the CA3059 is reduced because the circuit is operating in the dc mode. The 1000-ohm resistor R_G, connected between terminal 4 and the gate of the triac, limits the output current to approximately 3 milliamperes.

When the CA3059 is connected in the dc mode, the drive current for terminal 4 can be determined from a curve of the external load current as a function of dc voltage from terminals 2 and 7. This curve is shown in the technical bulletin for the CA3059 integrated circuit. Of course, if additional output current is required, an external dc supply may be connected between terminals 2 and 7, and resistor R_X (shown in Fig. 394) may be removed

Table XXXII compares some of the operating characteristics of the CA3059, when used as a comparator, with a typical high-performance commercially available integrated-circuit differential comparator.

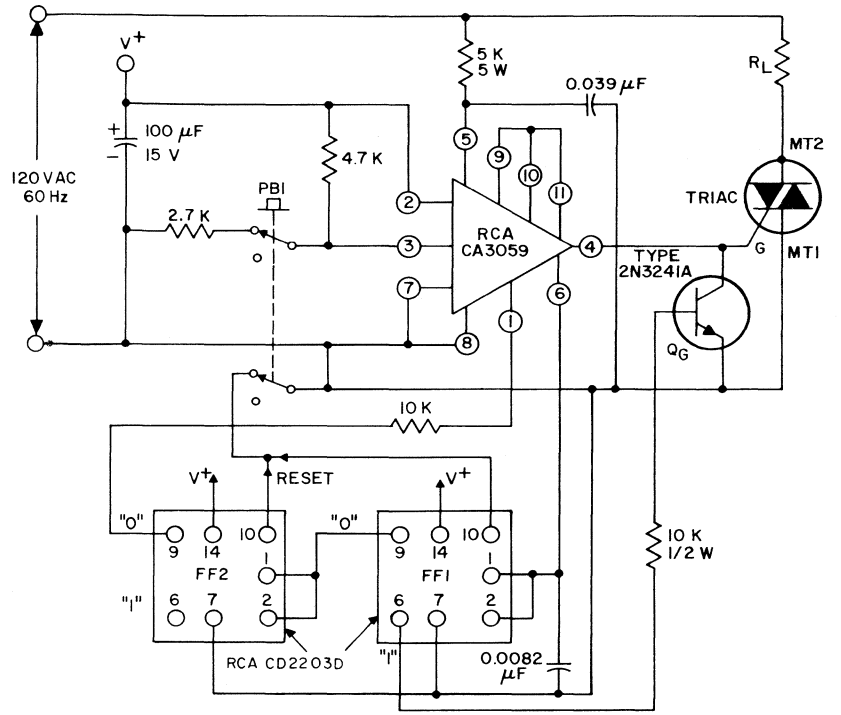
Power One-Shot Control

Fig. 395 shows a circuit which triggers a triac for one complete half-cycle of either the positive or negative alternation of the ac line voltage.



All resistance values in ohms unless otherwise specified.

Fig. 394 — Differential comparator using the CA3059.



All resistance values in ohms unless otherwise specified.

Fig. 395 — Block diagram of a power one-shot control using the CA3059.

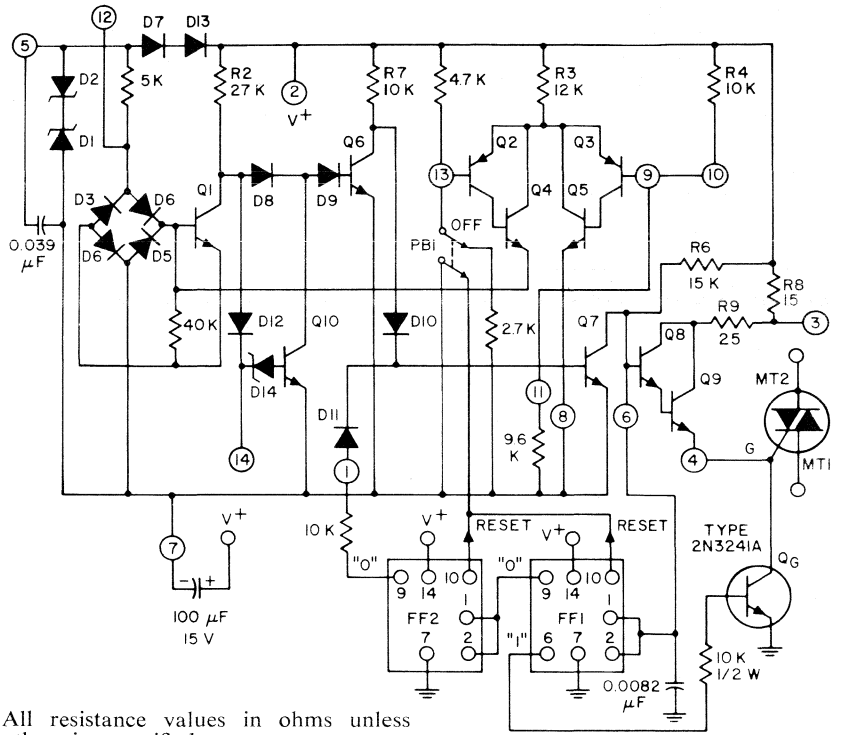
In this circuit, triggering is initiated by the push button PB1, which produces triggering of the triac near zero voltage even though the button is randomly depressed during the ac cycle. The triac does not trigger again until the button is released and again depressed. This type of logic is required for the solenoid drive of electrically operated stapling guns, impulse hammers, and similar equipment in which load-current flow is required for only one complete half-cycle. Such logic can also be adapted to keyboard consoles in which contact bounce produces transmission of erroneous information.

In the circuit of Fig. 395, before the button is depressed, both flip-flop outputs are in the "zero" state.

Table XXXII — *Comparison of the Operating Characteristics of a CA3059 Comparator with those of a Commercial Integrated-Circuit Differential Comparator*

PARAMETERS	CA3059 (typical values)	Typical Integrated-Circuit Comparator (710)
1. Sensitivity	50 mV	2mV
2. Switching speed (rise time)	>20 μs	90 ns
3. Output drive capability	*4.5V at ≤ 4mA	3.2V at ≤ 5.0mA

* Refer to Fig. 394; R_x equals 5000 ohms.



All resistance values in ohms unless otherwise specified.

Fig. 396 — Circuit diagram for the power one-shot control.

Transistor Q_G is biased ON by the output of flip-flop FF1. The differential comparator which is part of the CA3059 circuit is initially biased to inhibit output pulses. When the push button is depressed, pulses are generated, but the state of Q_G determines the requirement for their supply to the triac gate. The first pulse generated serves as a "framing pulse" and does not trigger the triac but toggles FF1. Transistor Q_G is then turned off. The second pulse triggers the triac and FF1 which, in turn, toggles the second flip-flop FF2. The output of FF2 turns on transistor Q7, as shown in Fig. 396, which inhibits all further output pulses. When the pushbutton is released, the circuit resets itself until the process is repeated with the button. Fig. 397 shows the timing diagram for the operating sequence.

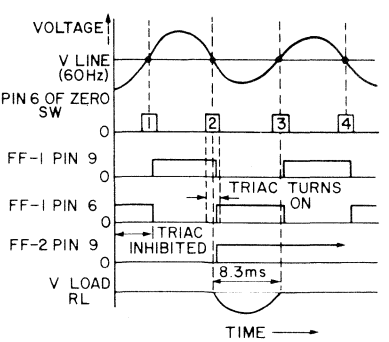


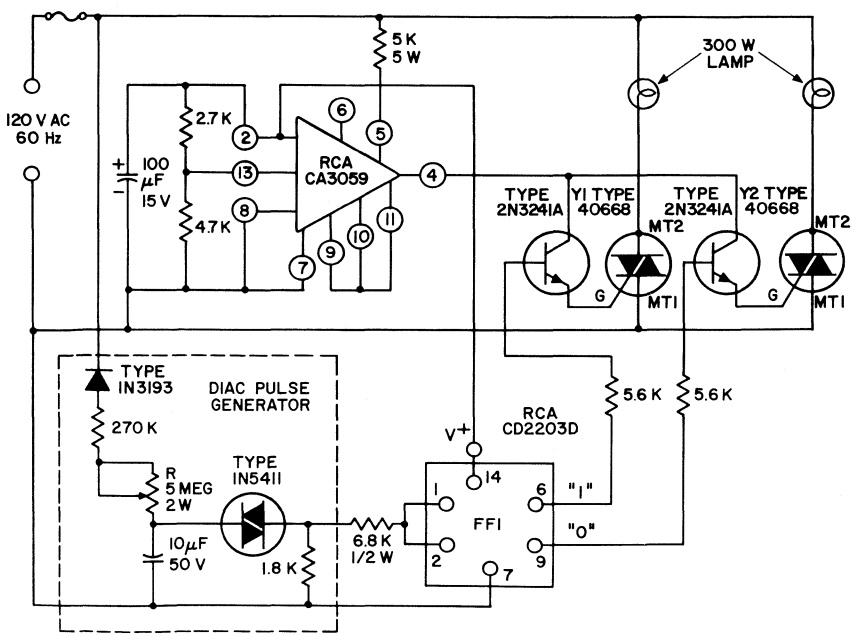
Fig. 397 — Timing diagram for the power one-shot control.

Solid-State Traffic Flasher

Another application which illustrates the versatility of the CA3059, when used with RCA thyristors, involves switching traffic-control lamps. In this type of application, it is essential that a triac withstand a current surge of the lamp load on a continuous basis. This surge results from the difference between the cold and hot resistance of the tungsten filament. If it is assumed that triac turn-on is at 90 degrees from the zero-voltage crossing, the first current-surge peak is approximately ten times the peak steady-state value or fifteen times the steady-state rms value. The second current-surge peak is approximately four times the steady-state rms value.

When the triac randomly switches the lamp, the rate of current rise di/dt is limited only by the source inductance. The triac di/dt rating may be exceeded in some power systems. In many cases, exceeding the rating results in excessive current concentrations in a small area of the device which may produce a hot spot and lead to device failure. Critical applications of this nature require adequate drive to the triac gate for fast turn-on. In this case, some inductance may be required in the load circuit to reduce the initial magnitude of the load current when the triac is passing through the active region. Another method may be used which involves the switching of the triac at zero line voltage. This method involves the supply of pulses to the triac gate only during the presence of zero voltage on the ac line.

Fig. 398 shows a circuit in which the lamp loads are switched at zero line voltage. This approach reduces



All resistance values in ohms unless otherwise specified.

Fig. 398 — Synchronous-switching traffic flasher using the CA3059.

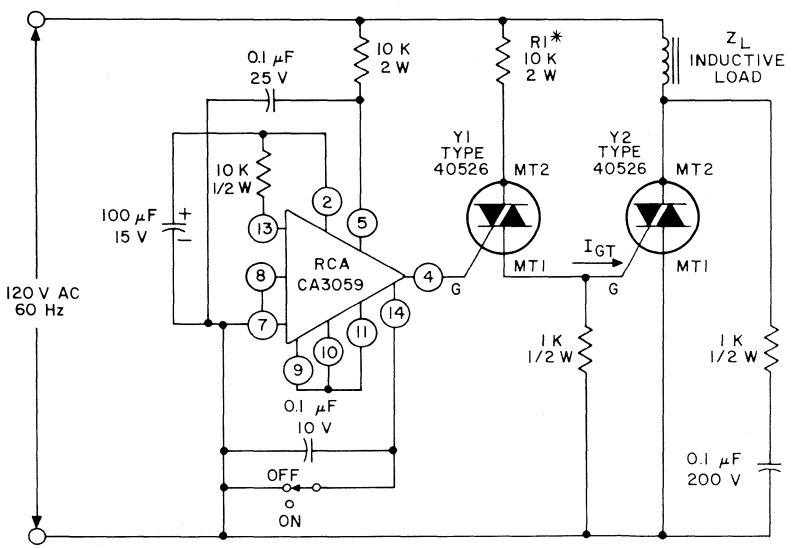
the initial di/dt, decreases the required triac surge-current ratings, increases the operating lamp life, and eliminates RFI problems. This circuit consists of two triacs, a flip-flop (FF1), the CA3059, and a diac pulse generator. The flashing rate in this circuit is controlled by potentiometer R, which provides between 10 and 120 flashes per minute. The state of FF1 determines the triggering of triacs Y1 or Y2 by the output pulses at terminal 4 generated by the zero-crossing circuit. Transistors Q1 and Q2 inhibit these pulses to the gates of the triacs until the triacs turn on by the logical "1" (V_{CC} high) state of the flip-flop.

The arrangement described can also be used for a synchronous, sequential traffic-controller system by addition of one triac, one gating transistor, a "divide-by-three" logic circuit, and modification in the design of the diac pulse generator. Such a system can control the familiar red, amber, and green traffic signals that are found at many intersections.

Transient-Free Switch Controller

The CA3059 can be used as a simple solid-state switching device that permits ac currents to be turned on or off with a minimum of electrical transients and circuit noise.

The circuit shown in Fig. 399 is connected so that, after the control terminals (14 and 7) are opened, electronic logic waits until the power-line voltage reaches a zero crossing before power is applied to the load Z_L. Conversely, when the control terminals are shorted, the load current continues until it reaches a zero



*IF Y2, FOR EXAMPLE, IS A 40-AMPERE TRIAC, THEN R1 MUST BE DECREASED TO SUPPLY SUFFICIENT I_{GT} FOR Y2

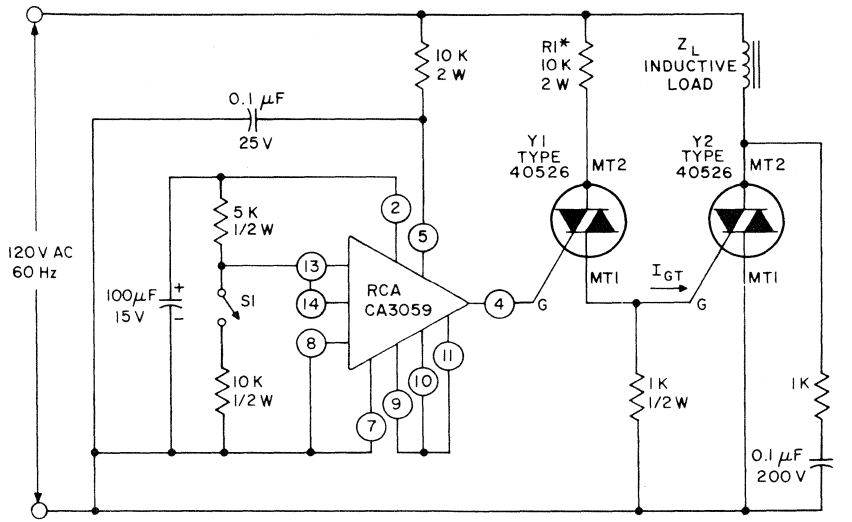
All resistance values in ohms unless otherwise specified.

Fig. 399 — CA3059 transient-free switch controller in which power is supplied to the load when the switch is open.

crossing. This circuit can switch a load at zero current whether it is resistive or inductive.

The circuit shown in Fig. 400 is connected to provide the opposite control logic to that of the circuit shown in Fig. 399. That is, when the switch is closed, power is supplied to the load, and when the switch is opened, power is removed from the load.

In both configurations, the maximum rms load current that can be switched depends on the rating of triac Y2. If Y2 is an RCA-2N5444 triac, an rms current of 40 amperes can be switched.



* IF Y2, FOR EXAMPLE, IS A 40-AMPERE TRIAC, RI MUST BE DECREASED TO SUPPLY SUFFICIENT I_{GT} FOR Y2.

All resistance values in ohms unless otherwise specified.

Fig. 400 — CA3059 transient-free switch controller in which power is applied to the load when the switch is closed.

Transistor, Diode, and Amplifier Arrays

RCA has developed a number of integrated-circuit arrays of active devices that offer the user numerous options in circuit design and a wide selection of the types of applications in which they may be employed. Active-device arrays are extremely useful in circuit design because they provide the close electrical and thermal matching of device characteristics inherent in all monolithic integrated circuits, but are not limited by the restrictions applicable to passive elements (resistors, capacitors, and inductors) in the monolithic system. These arrays make practical many circuits that cannot be provided economically with discrete devices and may also be used for breadboard designs of complex monolithic circuits.

Several RCA integrated-circuit arrays contain two or more complete circuits. This group includes the CA3060 array of three OTA circuits and a bias regulator, described in the section on the **Operational Transconductance Amplifier,** and the CA3048 and CA3052 arrays of four independent ac amplifiers, described in the section on **Special-Purpose Circuits,** as well as the general-purpose amplifier arrays described in this section.

GENERAL CONSIDERATIONS

If linear integrated-circuit arrays are to be used to best advantage in circuit design, the following basic rules must be observed to assure proper device operation and to avoid damage to the integrated circuit (detailed discussions of these rules were given previously in the section on **Effects of Monolithic Fabrication on Circuit Design):**

1. The collector of all array transistors must be maintained positive with respect to the integrated-circuit substrate to assure that the substrate diode remains reverse-biased.
2. For normal circuit operation, forward-biasing of the array transistors must be prevented (base-to-collector voltage should not be allowed to exceed 0.6 volt unless the current in the base lead is limited by a resistance of at least 1000 ohms); otherwise, the associated "parasitic" p-n-p transistor operates and causes high currents to flow into the substrate.
3. The maximum dissipation rating of an integrated circuit is based on the sum of the dissipations of individual devices; the total dissipation of the array, therefore, must be

calculated on the basis of all devices operating in a given application.

4. The close electrical and thermal matching of monolithic devices applies only to devices fabricated on the same integrated-circuit chip. When several arrays are to be used in a circuit, the design should employ devices on the same array when matched characteristics are required.

The various RCA active-device arrays consist of several closely matched general-purpose silicon n-p-n transistors (or such transistors conected as diodes) on a common monolithic substrate. Although the specification limits for the different circuit types vary (as shown in the published data for each device), the transistors in all these arrays have the following typical characteristics:

Collector-to-base voltage, V_{CBO}	60 volts
Collector-to-emitter voltage, V_{CEO}	24 volts
Emitter-to-base voltage, V_{EBO}	7 volts
Small-signal forward current-transfer ratio, h_{fe} (at I_C = 1 mA)	100
Gain-bandwidth product, f_T	550 MHz

TRANSISTOR ARRAYS

RCA offers four simple transistor arrays (CA3018, CA3018A, CA3045, and CA3046) that are especially suitable for applications in which closely matched device characteristics are required. The CA3018 and CA3018A contain two isolated transistors plus two transistors connected in a Darlington-pair configuration on a single silicon chip mounted in a 12-terminal TO-5-style package. Both types are rated for operation over the temperature range from −55°C to +125°C. Fig. 401 shows the circuit diagram for these

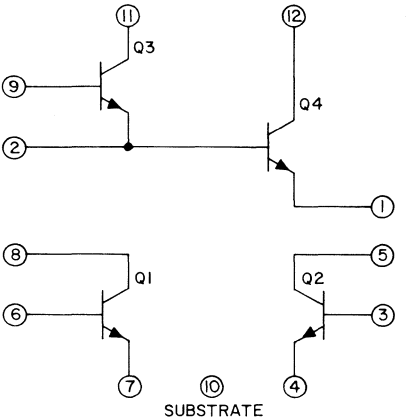


Fig. 401 — CA3018 or CA3018A integrated-circuit transistor array.

circuits, which are identical except that the CA3018A is more tightly controlled for certain characteristics (given in the **Technical Data** Section). The CA3045 and CA3046 consist of three isolated transistors plus two other transistors connected in an emitter-coupled differential-pair configuration. The two circuits are electrically identical. The CA3045, however, is supplied in a 14-terminal dual-in-line ceramic package, and the CA3046 is supplied in a 14-terminal dual-in-line plastic package. The CA3045 is rated for operation over the temperature range of −55°C to +125°C. The CA3046 is used in applications for which circuit operation over only a limited temperature range (0 to 70°C) is required. Fig. 402 shows the schematic diagram for the CA3045 or CA3046 array.

The applications for the transistor arrays are many and varied. The typical applications discussed in the following paragraphs have been selected to demonstrate the advantages of several matched devices available on a single chip. These few examples should stimulate the generation of a great many more applications.

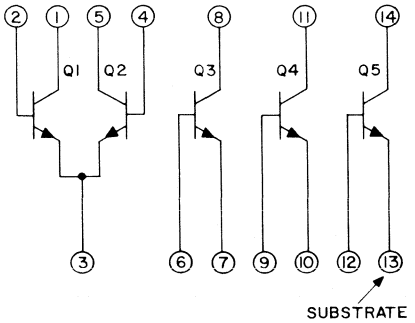


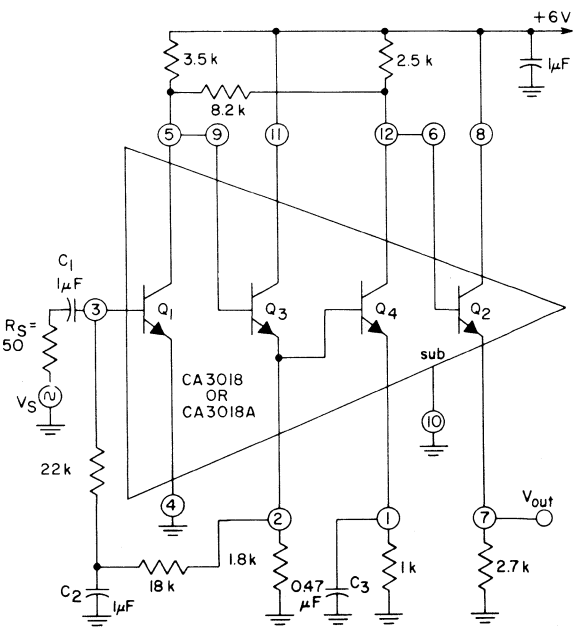
Fig. 402 — CA3045 or CA3046 integrated-circuit transistor array.

Wide-Band Video Amplifiers

Fig. 403 illustrates the use of the CA3018 or CA3018A (or four transistors of the CA3045 or CA3046) to provide a wide-band video amplifier with a gain of 49 dB and a bandwidth of 30 MHz. This amplifier may be considered as two dc-coupled stages, each consisting of a common-emitter, common-collector configuration. The common-collector transistor provides a low-impedance source to the input of the common-emitter transistor and a high-impedance, low-capacitance load at the common-emitter output. Iterative operation of the video amplifier can be achieved by capacitive coupling of stages.

Two feedback loops provide dc stability of the broadband video amplifier and exchange gain for bandwidth. The feedback loop from the emitter of Q3 to the base of Q1 provides dc and low-frequency feedback; the loop from the collector of Q4 to the collector of Q1 provides both dc feedback and ac feedback at all frequencies.

The frequency response of the broadband video amplifier is shown



All resistance values in ohms unless otherwise specified.

Fig. 403 — CA3018 broadband video amplifier.

in Fig. 404. The upper 3-dB break occurs at a frequency of 32 MHz. The low-frequency 3-dB characteristics are determined primarily by the values of capacitors C1, C2, and C3. The low-frequency 3-dB break occurs at 800 Hz. The mid-frequency gain of 49 dB is constant to within 1 dB over the temperature range from −55° to +125°C. The upper 3-dB break is constant at 32 MHz from −55°C to +25°C, and drops to 21 MHz at +125°C.

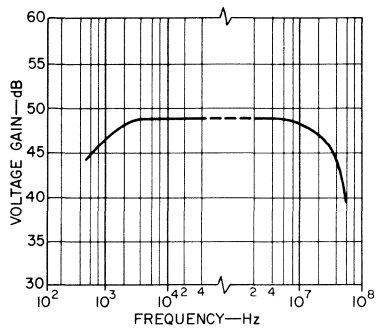


Fig. 404 — Voltage gain as a function of frequency for the broadband video amplifier shown in Fig. 403.

The total power dissipation over the entire temperature range is 22.8 milliwatts. The dc output voltage varies from 2.33 volts at −55°C to 3 volts at +125°C. The tangential sensitivity occurs at 20 microvolts peak-to-peak. The dynamic range is from 20 microvolts peak-to-peak to 11 millivolts peak-to-peak at the input.

The circuit of Fig. 403 demonstrates a typical approach that can be altered, especially with regard to gain and bandwidth, to meet specific performance requirements.

Differential Amplifiers

The CA3018, CA3018A, CA3045, and CA3046 arrays are suitable for use in a wide range of differential-amplifier applications, particularly in tuned-amplifier, mixer, if-amplifier, and limiter service. Because the transistors in these arrays are similar to those used in the CA3004, CA3005, CA3006, CA3028A, and CA3028B rf-amplifier integrated circuits (discussed in the section on **Differential-Amplifier Circuits),** the performance of the rf-amplifier types provides an excellent indication of the potential operation of the arrays. Some caution is required when the CA3045 and CA3046 dual-in-line circuits are used in high-frequency applications because capacitive coupling between the leads of these packages is greater than in the TO-5 packages. However, if care is taken to reduce capacitive coupling from input to output, these arrays are suitable for operation from dc to 100 MHz.

Fig. 405 shows the circuit diagram of a CA3018 or CA3018A differential-amplifier limiter. The collector-to-base diode of the transistor Q3 is used as the bias diode for the CA3018. However, because the diode

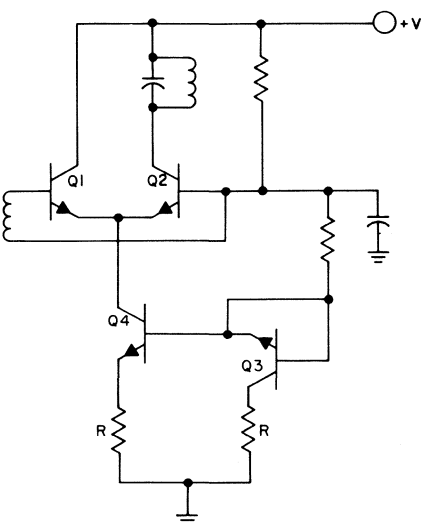


Fig. 405 — CA3018 or CA3018A differential-amplifier limiter circuit.

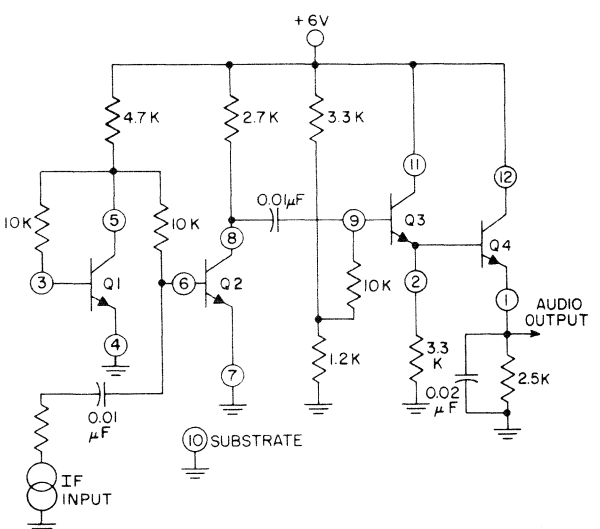
characteristics do not match those of the normally biased transistor Q4, small resistors are added to provide a voltage drop of about 50 millivolts at the operating current and thus re-establish a reasonable match. These resistors may be omitted if precise control of the operating current is not required.

Automatic gain control (agc) may be applied to the differential amplifiers by reduction of the current in the biasing device.

Final IF Amplifier Stage and Second Detector

Fig. 406 illustrates the use of the CA3018 or CA3018A as a last if amplifier and second detector (0.1-volt emitter voltage on terminal 1). The bias on transistor Q4 is maintained at approximately cutoff to permit the cascaded emitter-follower configuration (Q3 and Q4) to be used as a second detector. Because this stage is driven by a common collector configuration, the input impedance to the detector can be kept high. A low output load impedance can be used as a result of the output-current capability of the cascaded emitter-follower configuration. The input impedance (terminal 9) of approximately 9000 ohms is largely determined by the bias network. A minimum if input power of 0.4 microwatt must be delivered to terminal 9 for linear operation. The audio output power for 60-per-cent modulation for this drive condition is 0.8 microwatt. Linear detection is obtained through an input range of 20 dB for 60-per-cent modulation. This detector arrangement requires less power-output capability from the last if amplifier than a conventional diode detector, yet allows a low dc load resistor to achieve a good ac-to-dc ratio for the first audio amplifier.

The if amplifier of Fig. 406 has a voltage gain of 30 dB at 1 MHz. Transistor Q1 is used in the base-bias loop of the common-emitter



All resistance values in ohms unless otherwise specified.

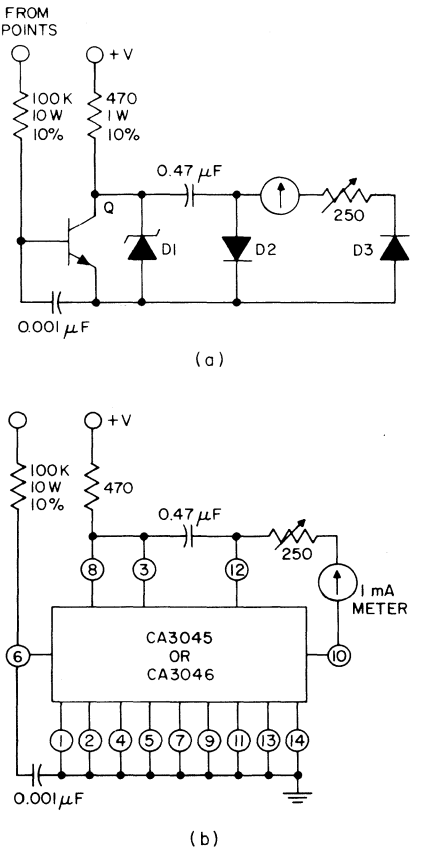
Fig. 406 — CA3018 or CA3018A final if amplifier and second detector.

amplifier Q2 to stabilize the output operating point against temperature variations. This arrangement also eliminates the need for an emitter resistor and bypass capacitor, and thus provides a larger voltage-swing capability for Q2. If Q2 is biased conventionally with base-bias resistors, Q1 can be made available for the first audio or agc amplifier.

Tachometer Circuit

The adaptability of the devices in the CA3045 and CA3046 arrays is best illustrated by the tachometer circuit shown in Fig. 407. This circuit is designed to provide a full-scale current to the meter of 1 milliampere at an engine speed of 6000 revolutions per minute when used with an eight-cylinder automotive engine. Linearity is better than 5 per cent, and accuracy for V^+ variations from 10 to 16 volts is approximately 5 per cent. The range of the instrument may be changed by selection of a different value of the timing capacitor Exact calibration may be obtained by adjustment of the resistor in series with the meter.

Fig. 407(a) shows the desired circuit configuration of the meter circuit, and Fig. 407(b) illustrates the realization of this circuit with the CA3045 or CA3046. Transistor Q3 of the integrated-circuit array serves as the transistor Q shown in the circuit of Fig. 407(a). The emitter-to-base junctions of transistors Q1 and Q2 are used in parallel to form a reasonably good 7-volt zener diode (D1). Transistors Q5 and Q4 are also connected as diodes (D2 and D3, respectively). The collector of Q5 is not connected to the base to form diode D2, however, because it is necessary to avoid conduction of the parasitic substrate diode; instead, the collector is grounded.



All resistance values in ohms unless otherwise specified.

Fig. 407 — Tachometer circuit: (a) desired configuration; (b) realization with CA3045 or CA3046.

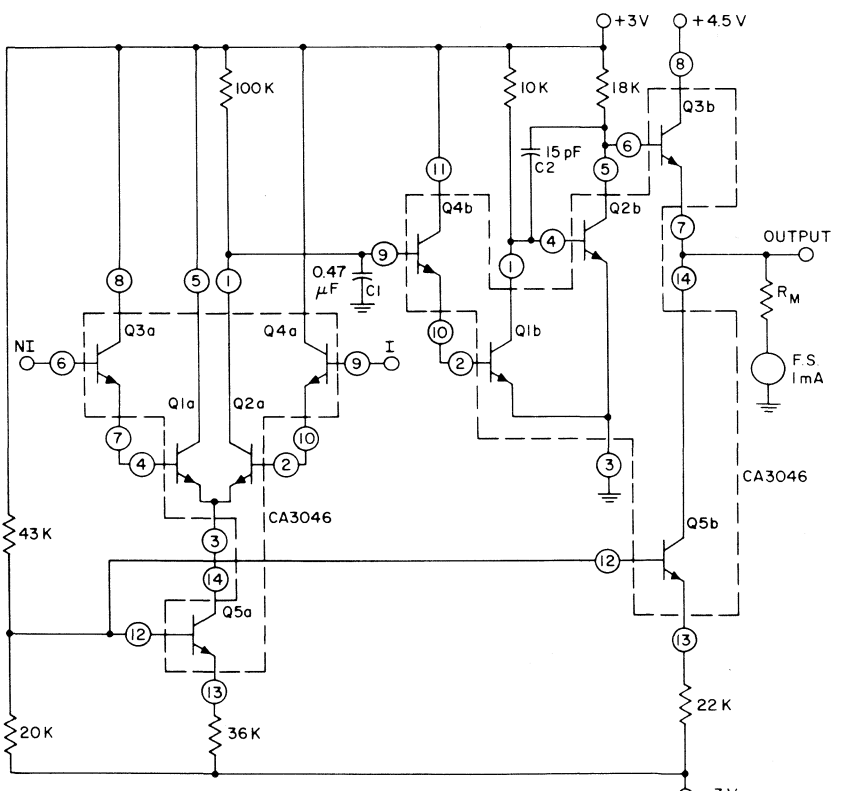
Operational Amplifiers

Although integrated-circuit operational amplifiers have become widely used general-purpose devices, many applications require features which are not readily available in fully integrated form. The CA3045 and CA3046 arrays are especially suited to the construction of special-purpose operational amplifiers for battery-

operated equipment in which low current drain and good performance at low supply voltage are extremely important.

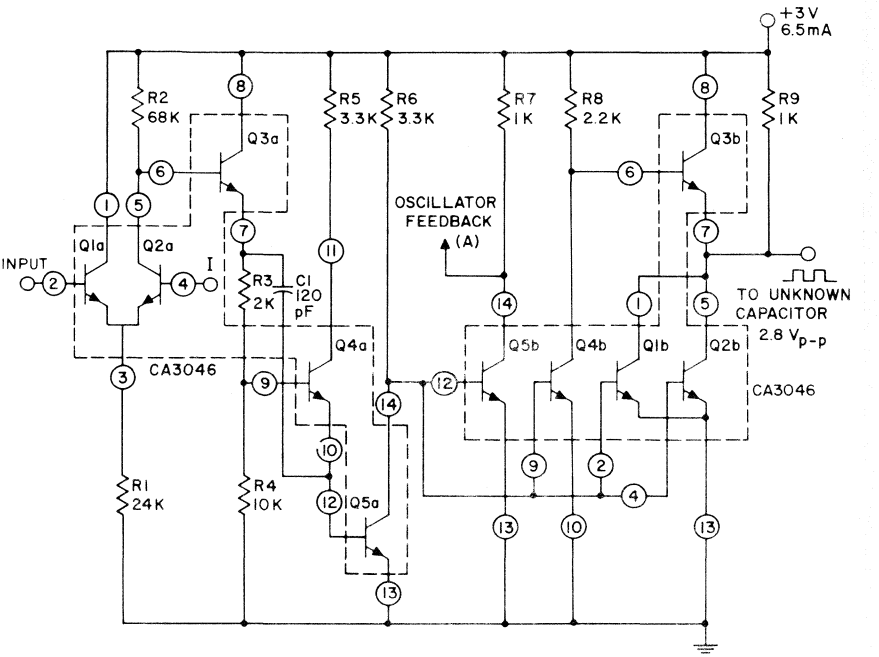
Fig. 408 shows the schematic diagram of an "op-amp" meter amplifier using two CA3046 arrays. The circuit is designed to drive a 1-milliampere dc meter to full scale in the positive direction only. The open-loop voltage gain is 80 dB, and the input bias current is less than 20 nanoamperes.

The first CA3046 is connected to form a Darlington-connected differential amplifier similar to the first stage of a CA3033 (described in the section on **Operational Voltage Amplifiers).** This stage operates at a current level of less than 40 microamperes. The Darlington-connected pairs have a composite beta in excess of 1000 and, therfore, provide an input bias current of less than 20 nanoamperes. Transistor Q4b of the second CA3046 is used as an impedance-matching level shifter to drive the voltage amplifier Q1b and Q2b. Transistor Q3b is an emitter-follower output. Q5b is used to keep Q3b from cutting off when the output is at zero volts. C1 and C2 reduce the high-frequency gain to avoid the possibility of oscillation with feedback. Standby current drains are 500 microamperes



All resistance values in ohms unless otherwise specified.

Fig. 408 — Operational-amplifier meter circuit using two CA3046 arrays.



All resistance values in ohms unless otherwise specified.

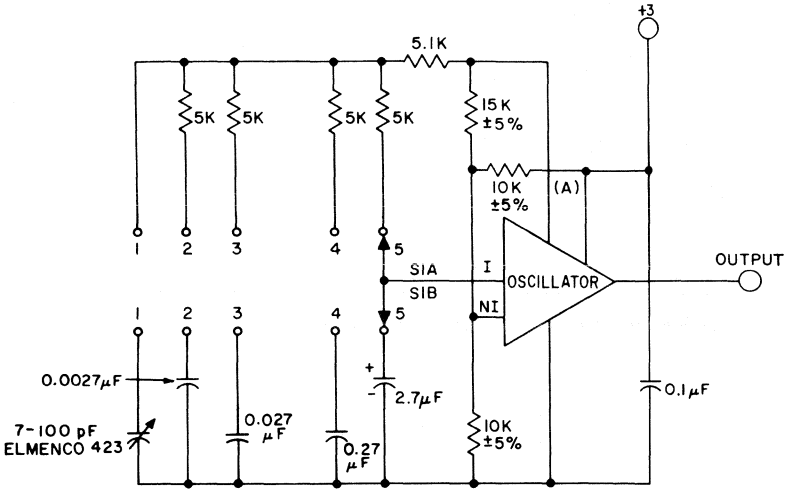
Fig. 409 — Pulse and square-wave generator using two CA3046 arrays.

from the positive supply and 200 microamperes from the negative supply, for a total dissipation of about 2 milliwatts. A total meter resistance (R_m) of 1000 ohms is recommended. Various feedback techniques can be used to tailor the amplifier to specific applications.

Fig. 409 shows an operational amplifier which is suitable for use as a pulse and square-wave generator. Although astable, bistable, and monostable circuits can be designed around simple flip-flops, the use of operational amplifiers permits the design of circuits which have characteristics dependent only on external resistor and capacitor values. Another advantage of operational amplifiers in astable circuits is that only one timing circuit is used; therefore, switching to permit operation at different frequencies is simplified.

In the circuit of Fig. 409, the first CA3046 provides most of the oscillator gain. One transistor of the second CA3046 (Q5b) completes the oscillator circuit. The other four transistors of the second CA3046 form a class B output stage similar to that used in the CA3033 operational amplifier. Q1b and Q2b are operated in parallel to achieve a lower output impedance in the negative direction than could be achieved with a single transistor. This connection is feasible because the matched characteristics of the monolithic transistors prevent "current hogging."

Fig. 410 illustrates the use of the circuit of Fig. 409 to form a square-wave generator in which the operating frequency can be switched in



All resistance values in ohms unless otherwise specified.

Fig. 410 — Frequency-adjustable square-wave generator.

decade steps from 46 Hz to 460 kHz. Separate resistors are used to allow precise setting of frequency.

Voltage Regulators

The connection flexibility and compactness of the CA3045 and CA3046 transistor arrays, shown in Fig. 402, make them attractive as low-power voltage regulators for laboratory use. Fig. 411 shows a circuit in which a CA3046 is used with an inexpensive 2N5183 transistor to construct a regulator which can provide current levels up to 500 milliamperes at a fixed voltage level of 8 to 8.5 volts. Transistor Q3 is used as a zener diode which, together with the input transistor Q2, forms a nominal 7.7-volt reference. The resistor R1 is selected to provide a current of approximately 0.5 milliampere through the zener diode. Q1, Q2, and Q5 form a high-gain voltage amplifier in which C1 provides compensation to avoid oscillation. Q4 is an emitter-follower which drives the output transistor. Current limiting is provided by the action of R4; an increase in the value of this resistor limits the output current to a lower value.

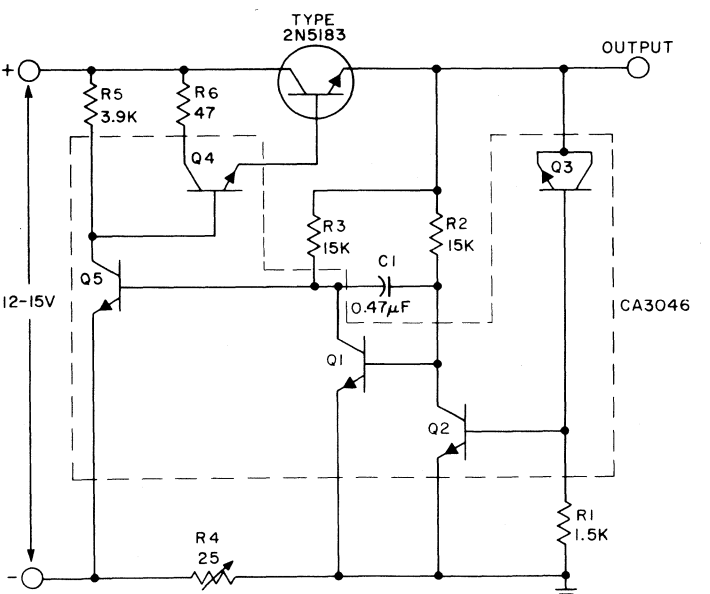
Fig. 412 shows a general configuration for a voltage regulator with a differential amplifier. This circuit provides better temperature stability than the single-ended amplifier of Fig. 411. In the circuit of Fig. 412, Q1 and Q2 form the differential amplifier. Q3 is an emitter-follower which drives the 2N5183 output transistor. Q4 is connected as a zener diode. Q5 activates the current-limiting circuit. When the voltage across R5 exceeds 600 millivolts, Q5 conducts and increases the current in both Q1 and Q2 to decrease the output voltage. Many variations of this circuit are possible. Q4 may be used as the output transistor when currents up to only 15 milliamperes are required. An external reference is then required for the circuit. (In this arrangement, special care must be taken to keep the total dissipation of the integrated-circuit array within

ratings.) Q4 and Q5 may also be used to form a constant-current source in place of R4. This modification can extend the useful range of the circuit to lower voltages.

DUAL INDEPENDENT DIFFERENTIAL-AMPLIFIER ARRAYS

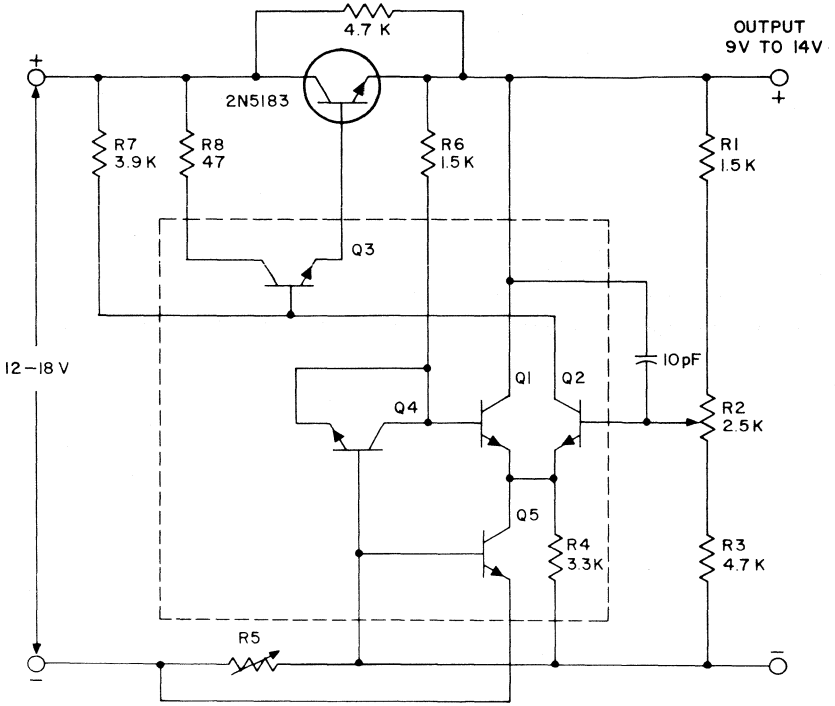
The CA3026, CA3049, and CA3054 each consist of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six n-p-n transistors which comprise the CA3026 and CA3054 amplifiers are general-purpose devices which exhibit low 1/f noise and a value of f_T in excess of 300 MHz. These features make the CA3026 and CA3054 useful from dc to 120 MHz. The CA3049 contains six general-purpose high-frequency n-p-n transistors that exhibit a value of f_T in excess of 1000 MHz. As a result, this amplifier array is useful at frequencies up to 500 MHz. Bias and load resistors have been omitted from the three amplifier arrays to provide maximum application flexibility.

The CA3026 and CA3049 are supplied in hermetic 12-lead TO-5-style packages and are rated for an operating-temperature range of −55°C to +125°C. The CA3054 is supplied in a 14-lead plastic dual-in-line package with a limited temperature range. The availability of extra terminals allows the introduction of an independent substrate connection for maximum flexibility. The monolithic construction of the CA3026, CA3049, and CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in



All resistance values in ohms unless otherwise specified.

Fig. 411 — Voltage regulator using a CA3046 array.



All resistance values in ohms unless otherwise specified.

Fig. 412 — Voltage regulator with a differential amplifier.

dual-channel applications in which matched performance of the two channels is required. Fig. 413 shows the schematic diagrams of these arrays.

Synthesizer Mixer

The synthesizer-mixer circuit shown in Fig. 414 consists of two differential amplifiers and their constant-current transistors, a configuration for which each of the three amplifier arrays is ideal. When the CA3054 is used, capacitor C6 can be omitted, because the independent substrate is available for dc or ac ground. The collector outputs for the differential pairs Q1-Q2 and Q5-Q6 are connected so that the balanced push-pull drive on the emitters and bases essentially cancels each output. Normally, frequency f_1 is applied to the bases of transistors Q1, Q2, Q5, and Q6. Frequency f_2 is applied to the bases of the constant-current transistors Q3 and Q4. If not overdriven, a single differential amplifier becomes a product mixer that reduces the generation of spurious signals. The linearizing effects of resistors R3 and R4 assure a current drive to the emitters of each differential pair that is similar to the voltage waveform at the bases of the constant-current transistors Q3 and Q4. With proper drive conditions, therefore, the outputs to T3 can be the desired sum and difference frequencies of f_1 and f_2 with

low spurious responses and with f_1 and f_2 suppressed. Applications for the synthesizer mixer include mixers, balanced modulators, and product detectors.

Synchronous Detector

A synchronous detector is another example of a doubly balanced circuit. Fig. 415 shows a simplified synchronous detector using the CA3026, CA3049, or CA3054 which can be used to detect both the phase and the amplitude of a television chroma signal. In this circuit, the reference signal is fixed in both phase and amplitude at 3.58 MHz. The chroma input signal varies in both phase and amplitude in accordance with the hue and saturation information, respectively. The TV detector must compare the steady reference signal and the varying chroma input signal without causing interaction between the two signals, and must cancel the reference signal without resorting to elaborate filtering systems in the output. A doubly balanced demodulator is an ideal means for accomplishment of this objective.

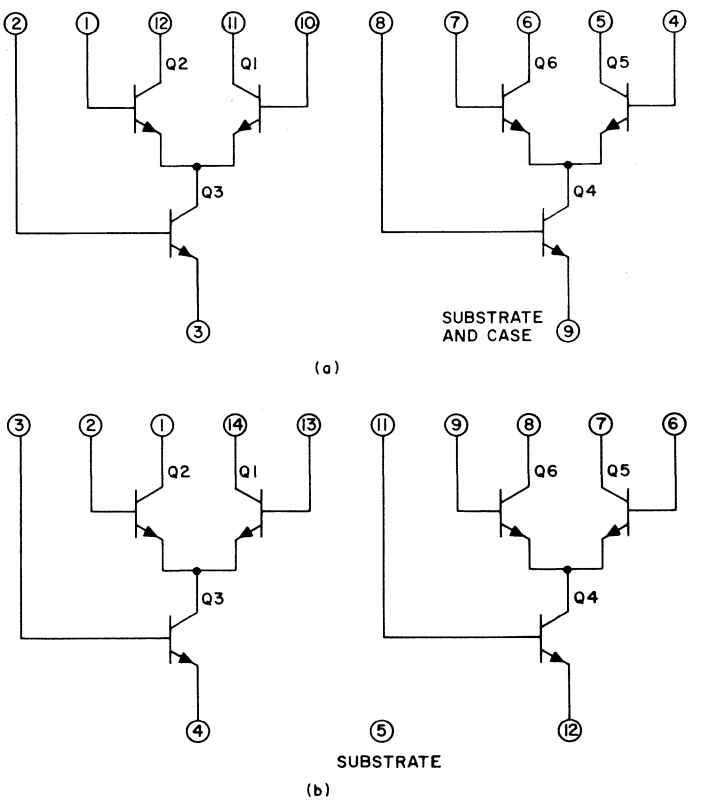
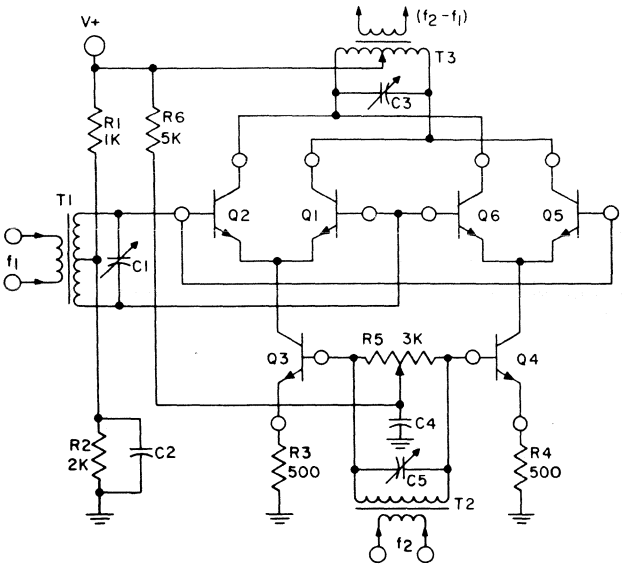


Fig. 413 — Integrated-circuit dual independent differential amplifiers: (a) CA3026 or CA3049; (b) CA3054.



All resistance values in ohms unless otherwise specified.

Fig. 414 — Synthesizer-mixer circuit using an integrated-circuit amplifier array in a doubly balanced circuit configuration.

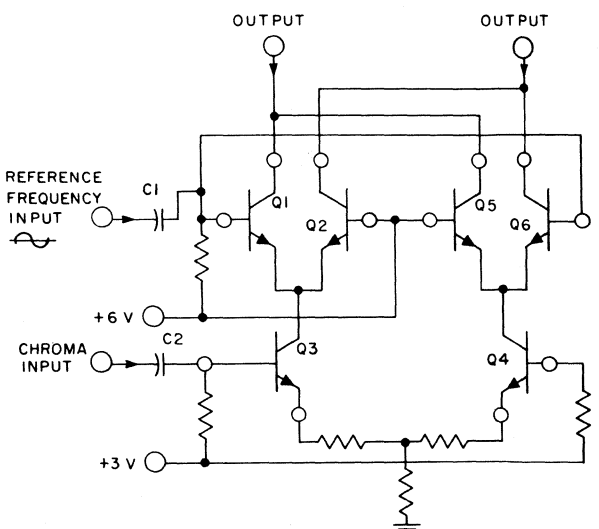


Fig. 415 — Synchronous detector using a doubly balanced circuit.

Transistors Q3 and Q4 are connected as a differential amplifier for the chroma signal input and supply opposite-phase chroma signals to the transistor switches Q1-Q2 and Q5-Q6. The chroma signal currents flow from Q3 and Q4 into either of the output leads in accordance with the instantaneous state of each transistor switch. The state of the switch is entirely dependent upon the reference signal applied to its base. In essence, the reference signal performs synchronous switching at its frequency of repetition. By the synchronous comparison process, it is possible to produce an output signal which is a function of the instantaneous phase difference between the chroma and reference signals. Because both the chroma and the reference signals enter into balanced-differential networks, the circuit is doubly balanced. It can also be shown that amplitude variation in the chroma input (with a fixed-amplitude reference input) produces corresponding amplitude variations in the chroma video output.

Although the doubly balanced circuit of Fig. 415 could be built with matched discrete transistors, the need for multiple matched devices would make it expensive. Furthermore, matching would deteriorate as a result of temperature variations and there would be a serious degradation in performance. The circuit could also be built with two single-stage differential amplifiers, such as a pair of CA3028A or CA3028B devices, with Q1 through Q3 in one package and Q4 through Q6 in another package. Even if selected pairs of CA3028A or CA3028B packages were used, however, serious mismatching could still occur with temperature variations. Because the CA3026 contains the required six transistors on the same chip, it has excellent pair-matching characteristics; in addition, tracking of characteristics is maintained with variations in temperature.

DIODE ARRAYS

The CA3019 and CA3039 arrays consist of six ultra-fast, low-capacitance diodes on a common monolithic substrate. Integrated-circuit construction assures excellent static and dynamic matching of the diodes and makes the arrays extremely useful in a wide variety of applications in communications and switching systems. In the CA3019, four diodes are internally connected in a diode-quad arrangement; the other two diodes are independent. In the CA3039, five of the diodes are independently accessible; the sixth shares a common terminal with the substrate. The schematic diagrams for these arrays are shown in Fig. 416.

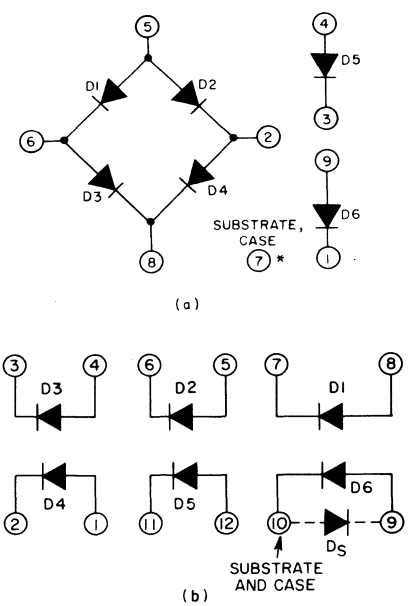


Fig. 416 — (a) CA3019 and (b) CA3039 integrated-circuit diode arrays.

Because all the diodes are fabricated simultaneously on a single silicon chip, they have nearly identical characteristics, and their parameters track each other with temperature variations as a result of their close proximity and the good thermal conductivity of silicon. Consequently, these arrays are particularly useful in circuit configurations which require either a balanced diode bridge or identical diodes. Similarly, the six diodes in the CA3039 can be connected in a number of ways for use in voltage-regulator circuits, bias and current-limiting circuits for push-pull amplifiers, temperature-compensation circuits for constant-current sources and SCR triggering circuits, direct-coupled transistor amplifiers, signal limiting and clamping circuits, logic gates, level-shifting circuits in DTL (diode-transistor-logic) circuits, and varistor circuits. The following paragraphs describe a few practical circuits to stimulate the thinking of potential users.

There are many possible applications for the CA3019. Besides the obvious uses as separate diodes and possible quad combinations, some of which are covered in the following discussion, it should be noted that shorting of terminals 2 and 6 in the quad effectively provides two diodes in series. This diode connection can be used as the elements of special balanced mixers, as ring modulators, and as compensating networks that provide two diode drops. Fig. 417 shows an example of a typical synthesizer mixer circuit. Shorting of terminals 5 and 8 provides two independent sets of back-to-back diodes useful for limiting and clipping, as shown in Fig. 418.

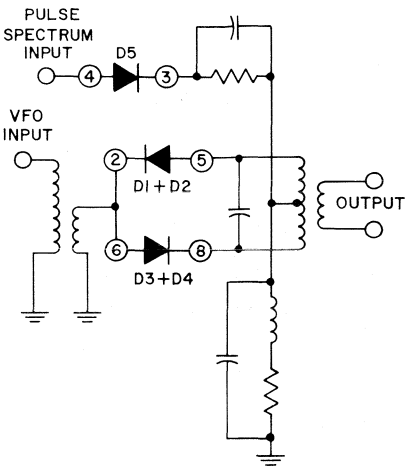


Fig. 417 — Typical synthesizer mixer circuit using the CA3019.

Balanced Modulator

Fig. 419 shows the use of the CA3019 as a balanced modulator which minimizes the carrier frequency from the output by means of a symmetrical bridge network. A carrier of one polarity causes all the diodes to conduct, and thus effectively short-circuits the signal source. A carrier of the opposite polarity cuts off all the diodes and allows signal current to flow to the load. If

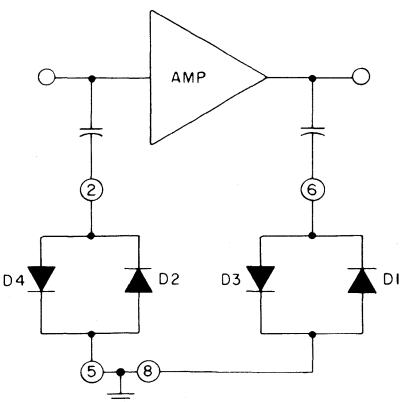
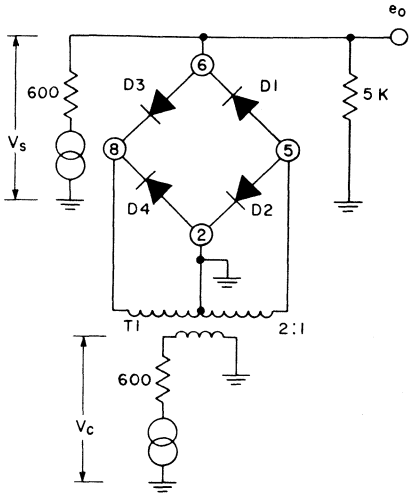


Fig. 418 — Limiters using the CA3019.



T1—TECHNITROL No. 85I166 OR EQUIV.

All resistance values in ohms unless otherwise specified.

Fig. 419 — Balanced modulator using the CA3019.

the four diodes are identical, the bridge is perfectly balanced and no carrier current flows in the output load. The circuit operates properly with the substrate (terminal 7) either floating or returned to a negative voltage. Table XXXIII lists the characteristics of the balanced modulator.

Balanced Mixer

Fig. 420 illustrates the use of the CA3019 as a conventional balanced mixer. The load resistor across the output tuned circuit is selected to provide maximum power output. The conversion gain of the mixer for a 45-MHz input signal and a 55-MHz oscillator signal is shown in Fig. 421. The input impedance at point A is approximately 600 ohms for a 0.6-volt-rms oscillator drive.

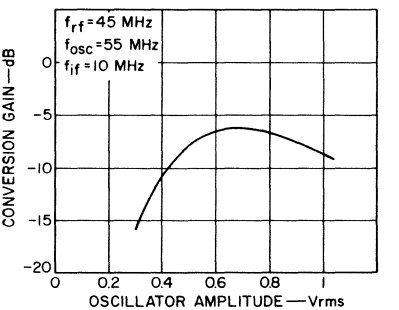
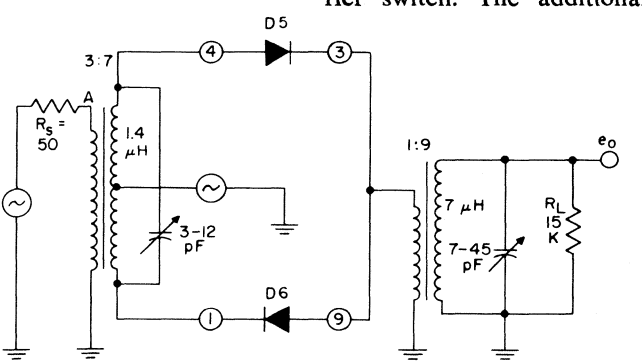


Fig. 421 — Conversion gain as a function of oscillator voltage for the balanced mixer shown in Fig. 420.

The CA3019 mixer shown in Fig. 422 is essentially a balanced mixer with two additional diodes (D3 and D4) added to form a half-wave carrier switch. The additional diodes



All resistance values in ohms unless otherwise specified.

Fig. 420 — Balanced mixer using the CA3019.

Table XXXIII — *Characteristics of Balanced Modulator of Fig. 419*

Carrier Voltage, V_C V rms at 30 kHz	0.75		0.75		0.75		0.50		1.0	
Signal Voltage, V_S mV rms at 2 kHz	77		245		770		245		245	
Output Frequency kHz	**Output Voltage mV rms**	**dB Below V_S**	**Output Voltage mV rms**	**dB Below V_S**	**Output Voltage mV rms**	**dB Below V_S**	**Output Voltage mV rms**	**dB Below V_S**	**Output Voltage mV rms**	**dB Below V_S**
28 and 32*	34	6.5	115	7	440	5	51	14	170	3
30	0.7	41	0.82	49	2.6	50	0.1	68	3.6	37
26 and 34	0.02	72	0.05	72+	0.48	64	0.04	72+	0.07	71
24 and 36	0.03	69	0.49	54	60	22	0.58	52.5	0.6	53
22 and 38	0.001	72+	0.01	72+	1.4	55	0.015	72+	0.02	72+

*** Double-Sideband, Suppressed-Carrier Output.**
All other outputs are spurious signals.

permit both legs of the circuit (D1 — D2 and D3 — D4) to function throughout the ac cycle. As compared with a conventional balanced mixer, shown in Fig. 420, this circuit effectively doubles the desired output voltage and reduces the output voltage at the oscillator frequency by half. However, the capacitances associated with the integrated

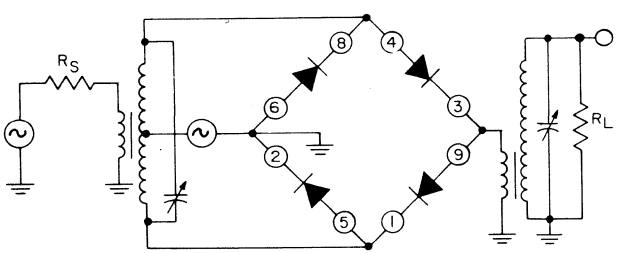


Fig. 422 — Balanced mixer with half-wave carrier switch using the CA3019.

diodes prevent this circuit configuration from realizing the improvement in conversion gain at frequencies above 20 MHz.

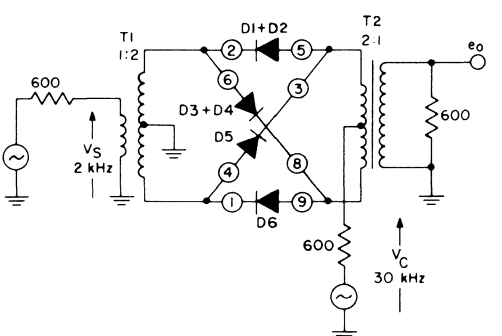
Ring Modulator

The use of the CA3019 as a ring modulator is shown in Fig. 423. If a perfectly balanced arrangement were used, carrier current of equal magnitude and opposite direction would flow in each half of the center-tapped transformer T2. Thus, the effect of the carrier current in transformer T2 would be cancelled, and the carrier frequency would not appear in the output. However, the ring modulator of Fig. 423 is not exactly balanced because diodes D1 + D2 and D3 + D4 are actually two diodes in parallel, while diodes D5 and D6 are individual diodes. Nevertheless, this circuit attenuates the carrier in the output as well as an arrangement that uses both individual diodes in two CA3019 circuits.

As the carrier passes through half of its cycle, diodes D1 + D2 and D6 conduct, and diodes D3 + D4 and D5 do not conduct. When the carrier passes through the other half of its cycle, the previously nonconducting diodes conduct, and vice versa. As a result, the output amplitude is alternately switched from plus to minus at the carrier frequency. The signal-frequency component of the output waveform is thus symmetrical about the zero axis and is not present in the output. Therefore, the ring modulator suppresses both the carrier frequency and the signal frequency so that the output theoretically contains only the upper and lower sidebands. For single-sideband transmission, one of these sidebands can be eliminated by selective filtering. The performance of the CA3019 as a ring modulator is shown in Table XXXIV.

Low-Voltage Regulator Circuit

The six diodes in the CA3039 may be connected in series, as shown in Fig. 424, to protect against voltage changes in a voltage source. Thus, the CA3039 is able to provide a regulated voltage output of approximately 4.5 volts. Higher voltages may be regulated by connection of an appropriate number of CA3039 arrays in series. The type of regulator shown in Fig. 424, when coupled with the package flexibility offered by the CA3039, can also supply intermediate values of voltage in applications requiring base-biasing. The schematic



All resistance values in ohms unless otherwise specified.

Fig. 423 — Ring modulator using the CA3019.

Table XXXIV — *Performance Characteristics of Ring Modulator*

Output Freq. (kHz)	V_S (mV)	For a given $V_S + V_g$, e_o in millivolts			
	V_C (mV)	300	350	450	500
28 or 32	Upper or Lower Sidebands	86	97	83	91
2	Sig. Freq.	0.042	0.02	0.015	0.020
30	Carrier Freq.	1.3(—37dB)*	0.88(—41dB)*	0.67(—42dB)*	0.62(—43dB)*
26 or 34	Higher Order Sidebands	0.018	0.016	0.036	0.043
24 or 36		0.021	0.054	0.047	5.0

* dB below the desired upper and lower sidebands

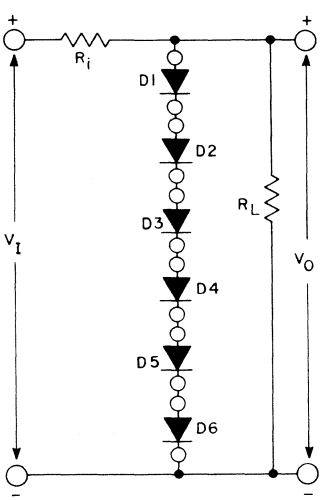


Fig. 424 — Low-voltage regulator circuit using the CA3039.

diagram of the CA3013 or CA3014 FM if amplifier/discriminator/af amplifier, shown previously in Fig. 309, illustrates the manner in which supply potentials for a complex solid-state circuit can be regulated by a diode-connected series-string configuration similar to that of the CA3039. A monolithic series-string regulator can also provide base and collector potentials which track in the face of temperature variations.

Fig. 425(a) shows a two-stage shunt-type configuration which provides even better regulation against a change in source voltage, but at the expense of efficiency and a reduction in output voltage to about 1.5 volts. Fig. 425(b) shows the CA3039 connected as a three-stage type of shunt regulator, again at the expense of efficiency and a reduction in voltage to approximately 0.75 volt.

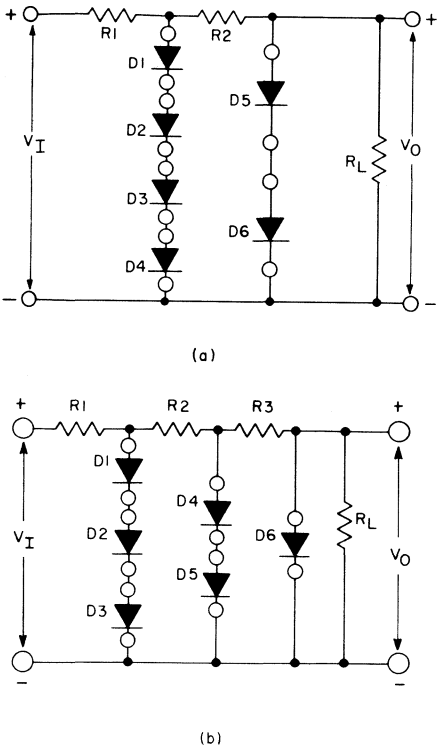


Fig. 425 — Shunt-type regulator circuits: (a) two-stage type; (b) three-stage type.

Fig. 426 illustrates the use of an emitter follower with the circuit shown in Fig. 424 to achieve better regulation.

Biasing and Current Limiting for Push-Pull Amplifiers

The amplifier shown in Fig. 427 is a complementary push-pull configuration driven by a class A driver-amplifier device. Resistor R2 serves as a common path for ac and dc feedback. The diode pair D1-D2 biases the output stage in such a way that cross-over distortion is minimized while temperature compensation is provided to keep the idling current stable. The other two diode pairs,

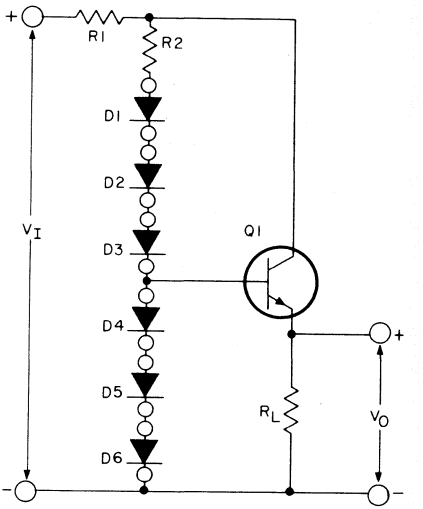


Fig. 426 — Emitter follower added to three-stage low-voltage regulator circuit.

D3-D4 and D5-D6 are connected in such a manner that they limit the emitter current in the output transistors and thereby protect them. This emitter-current limiting technique is also applicable to single transistors, as shown in Fig. 428. The maximum emitter current is equal to $(V^+ - 1V_{BE})/R_E$, and is relatively independent of load, base drive, and the power supply. This configuration can be used for current-limiting service in amplifiers, switching circuits, and voltage and current regulators.

Constant-Current-Source Temperature-Compensation Circuits

Fig. 429 illustrates the use of two of the CA3039 diodes to compensate for variations in transistor base-to-emitter voltages that result from temperature changes. This method of temperature compensation is used in a number of RCA linear integrated circuits (e.g., the CA3005). Single diodes are used to provide tempera-

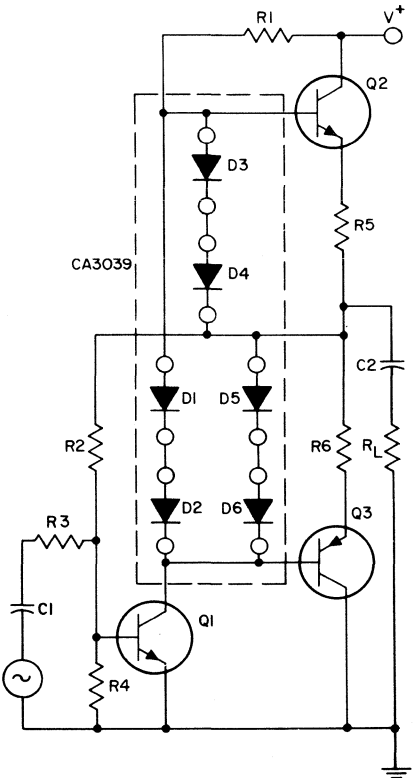


Fig. 427 — Complementary push-pull amplifier driven by class A driver-amplifier device.

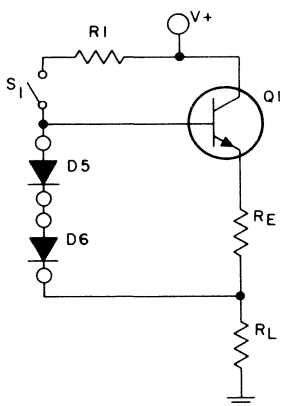


Fig. 428 — Emitter-current limiting circuits for single transistors.

ture compensation in various stages of all RCA operational amplifiers. The CA3039 is useful in simultaneous temperature-compensated tracking systems for arrays of discrete transistors or for linear integrated-circuit array systems (e.g., the CA3045).

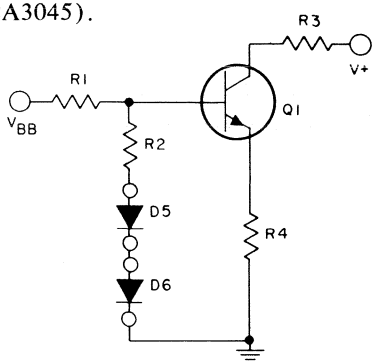


Fig. 429 — Use of two CA3039 diodes in a temperature-compensation circuit.

Direct-Coupled Transistor Amplifier Circuits

Fig. 430 shows a three-stage amplifier in which the six diodes of the CA3039 are used to provide low-ac-impedance voltage bias. Simplicity and good low-frequency response are the main advantages of this type of circuit.

Signal Limiting and Clamping Circuits

Four diodes of the CA3039 may be connected as shown in Fig. 431 to provide limiting or clamping and a choice of two voltage levels, approximately ±3 volts peak-to-peak or (with one diode of each series-connected pair shorted) ±1.5 volts peak-to-peak.

Logic Circuits

The diodes of the CA3039 can be connected to form either passive or

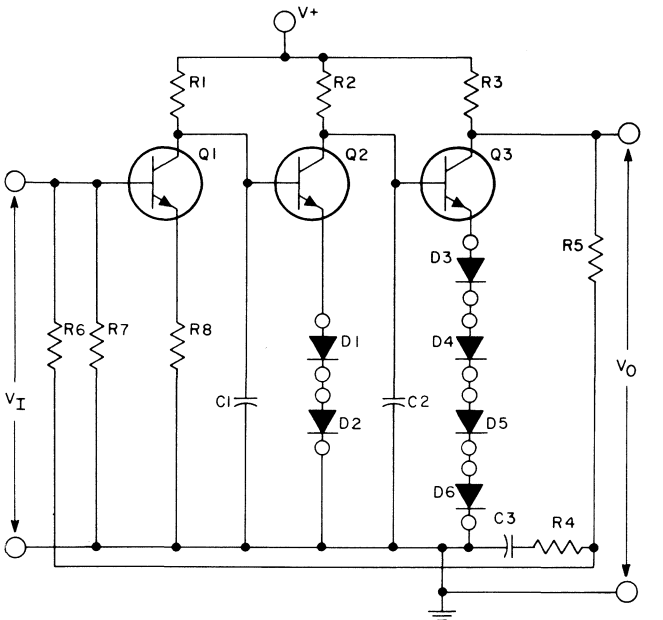


Fig. 430 — Three-stage amplifier employing diodes for low-ac-impedance voltage bias.

active logic gates. Fig. 432 shows 5-input "OR" and "NOR" gates using five of the CA3039 diodes. The diodes can also be connected to provide for level shifting in a NAND gate, as shown in Fig. 433, so that only one power supply is required.

Varistor Circuits

A varistor is a device consisting of two matched junctions of opposite polarity connected in parallel; it is used primarily for direct conversion of ac and dc information into logarithmic information over several decades. The transfer characteristics of the CA3039, shown in Fig. 434, illustrate the suitability of this array for such use. Three matched varistors can be provided by proper interconnection of diode pairs in the CA3039, as shown in Fig. 435. Varistors are applicable to fractional voltage regulators, meter protectors, telephone circuits, and negative-temperature-coefficient resistors.

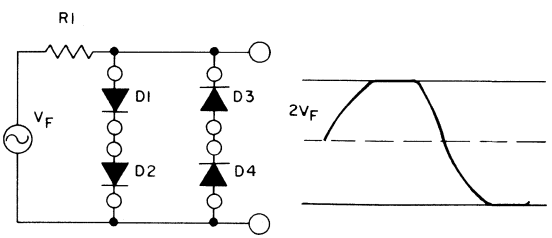


Fig. 431 — Use of four diodes of the CA3039 to form a limiting or clamping circuit.

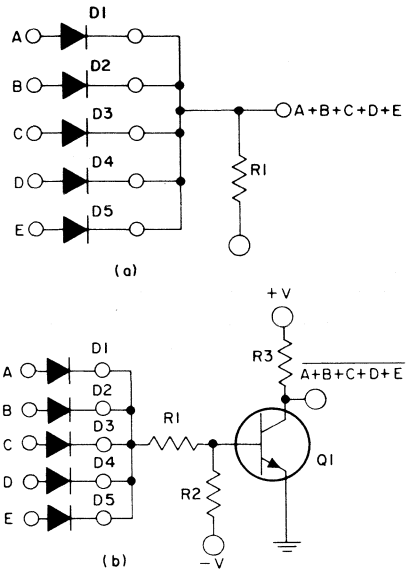


Fig. 432 — Five-input OR and NOR gates using CA3039 diodes.

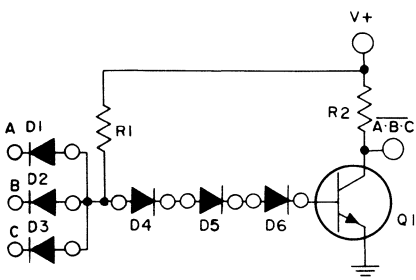


Fig. 433 — Use of CA3039 diodes in NAND gate to provide level shifting.

DUAL DARLINGTON ARRAY

The CA3036 integrated-circuit array may be used to provide two independent low-noise wide-band amplifier channels. These arrays are designed to operate over a range of ambient temperatures from −55°C to +125°C and are supplied in 10-terminal TO-5-style metal packages.

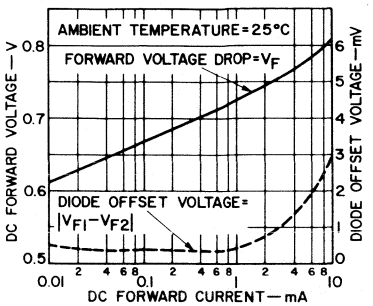


Fig. 434 — Transfer characteristics of a CA3039 diode.

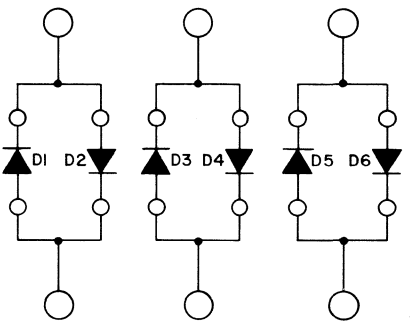


Fig. 435 — Three matched varistors composed of CA3039 diodes.

They are particularly useful for preamplifier and low-level amplifier applications in single-channel or stereo systems.

Fig. 436 shows the schematic diagram of the CA3036 array. The array consists of four transistors con-

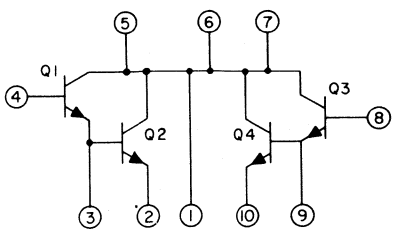


Fig. 436 — CA3036 integrated-circuit dual Darlington array.

nected to form two independent Darlington pairs. Fig. 437 shows a block diagram that illustrates the use of the array in a typical stereo phonograph. The CA3036 can be mounted directly on a stereo cartridge. Because of the low noise, high input impedance, and low output impedance of the array, only minimal shielding is required from the pickup to the amplifier. The buffering action of the CA3036 also substantially reduces losses and decreases hum pickup.

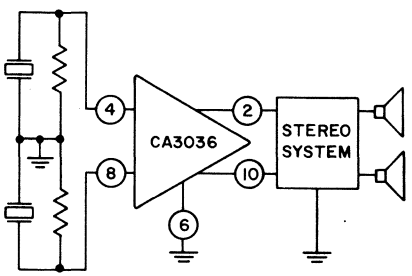


Fig. 437 — Block diagram of stereo system using a CA3036 in a phono preamplifier.

The CA3036 array features matched transistors with emitter-follower outputs, low-noise performance, and a gain-bandwidth product typically of 200 MHz. Typical applications of the array include stereo phonograph amplifiers, low-level stereo and single-channel stages, low-noise emitter-follower differential amplifiers, and operational-amplifier drivers.

DUAL INDEPENDENT DARLINGTON-CONNECTED DIFFERENTIAL AMPLIFIERS

The CA3050 and CA3051 each consist of two differential amplifiers with associated constant-current transistors on a common substrate. Each amplifier is driven by Darlington-connected emitter-follower inputs to provide high input impedance, low bias current, and low offset current. A string of diodes is included to provide temperature-compensated bias to the constant-current transistors and a low-impedance bias point for the inputs to the differential amplifiers when a single power supply is used.

The CA3050 is supplied in a hermetic 14-lead dual-in-line ceramic package rated for operation over the temperature range of −55°C to +125°C. The CA3051 is supplied in a dual-in-line plastic package for applications requiring only a limited temperature range of −25°C to +85°C. Fig. 438 shows the schematic diagram for the CA3050 or CA3051 integrated circuit.

The CA3050 and CA3051 are basically the same as the CA3026 dual independent differential-amplifier array discussed earlier in this section, except that the CA3050 and CA3051 have a higher input impedance and an additional three diodes for bias networks. The CA3050 and CA3051, therefore, can be used for all the applications in which the CA3026 can be used. Additional applications of the CA3050 and CA3051 include a single-sideband phase-shift modulator. Fig. 439 shows a typical single-sideband phase-shift modulator in which the audio phase-shift network makes it possible to change from the upper to the lower sideband.

WIDE-BAND AMPLIFIER ARRAY

The CA3035 integrated-circuit array is an ultra-high-gain, low-noise, wide-band device intended primarily for use as a remote-control amplifier in receiver applications. The circuit is supplied in a 10-terminal TO-5-style package. The circuit operates from a single dc power supply at various voltage levels up to 15

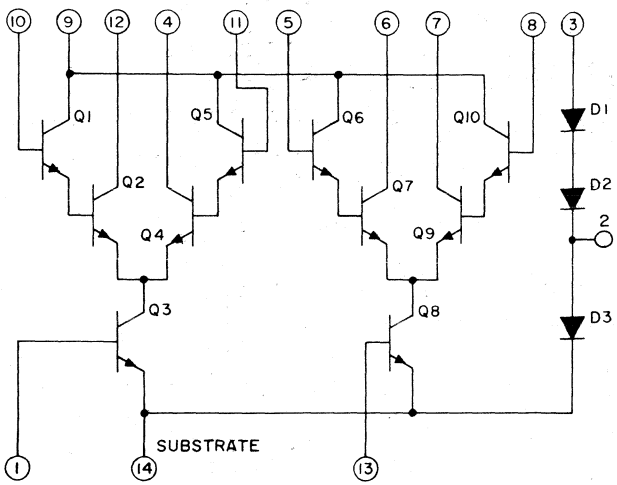


Fig. 438 — CA3050 or CA3051 integrated-circuit dual independent Darlington-connected differential amplifiers.

volts over an ambient-temperature range from −55°C to +125°C.

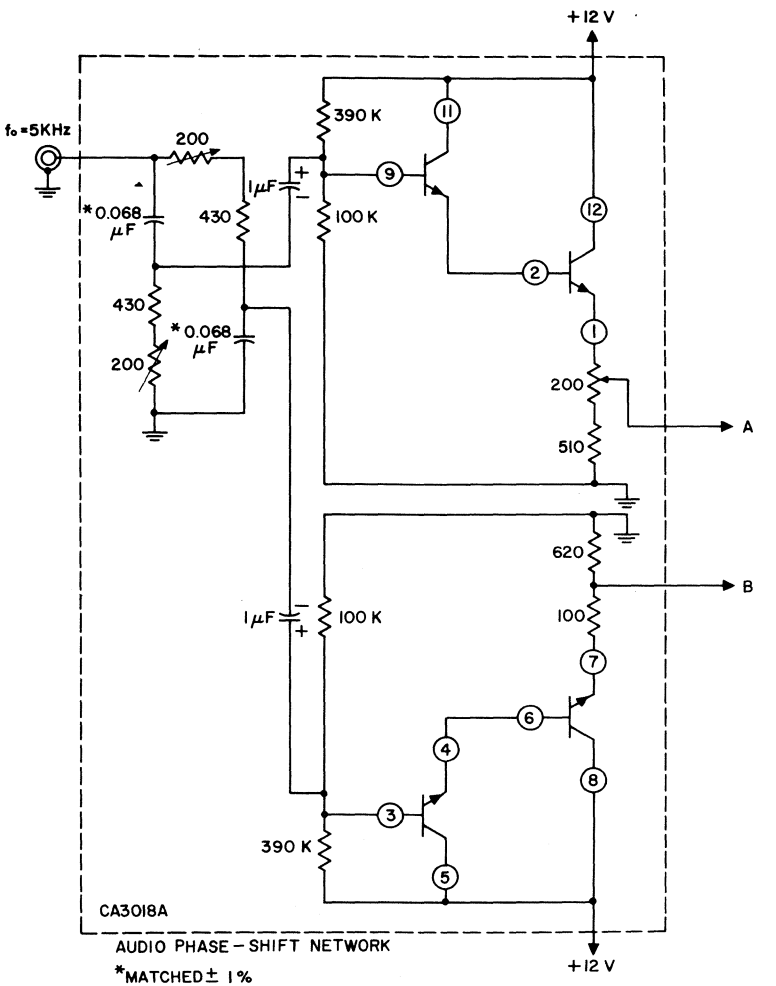
The CA3035 circuit consists of three general-purpose high-gain amplifier stages that may be operated independently or in cascade. Each stage can provide a voltage gain in excess of 40 dB and when the three amplifiers are operated in cascade, they provide an over-all voltage gain of 120 dB at 40 kHz. In addition to high gain, the amplifiers have low noise levels and good limiting capability. Amplifier performance is maintained over a wide temperature range and remains relatively constant with nominal changes in supply voltages.

Fig. 440 shows the schematic diagram for the wide-band integrated array. The first stage features a low-noise common-emitter amplifier combined with emitter-followers at both the input and the output. The second stage consists of a common-emitter input, an emitter-follower output, and a dc voltage regulator. The third stage consists of a common-emitter amplifier with an uncommitted collector and a voltage regulator. The uncommitted collector permits the use of tuned or resistive loads and an increased collector supply voltage for larger output swings. Fig. 441 shows the gain-frequency response for each amplifier stage.

Fig. 442 shows the CA3035 used in a remote-control system. An input signal of about 40 kHz is delivered to terminal 1 from the microphone pickup. The remote-control system requires a typical input voltage of 100 microvolts to pull in the relay driver. The amplifier operates over a frequency range of 35 to 45 kHz and provides a gain of 120 dB for the signal which is derived from a condenser microphone. The three stages of the CA3035 array are coupled by means of external capacitors, and the output signal is developed across the impedance of a tuned transformer. Optimum operation of the amplifier is achieved by selection of suitable circuit configuration for the individual stages.

In the input stage, the first two transistors form a Darlington ampli-

fier with an input impedance sufficiently high to avoid excessive loading of the microphone. The third transistor is connected as an emitter follower and furnishes amplified signals to the second stage by means of the external coupling capacitor connected from terminal 3 to terminal 4. An external feedback network, formed by resistor R17 and R18 and the capacitor C1, is provided to maintain the three transistors properly biased and also to establish a high-pass characteristic for this stage. The over-all frequency response of the first stage, shown in Fig. 443, is tailored to resemble a selectivity curve centered around 45 kHz. A 6-

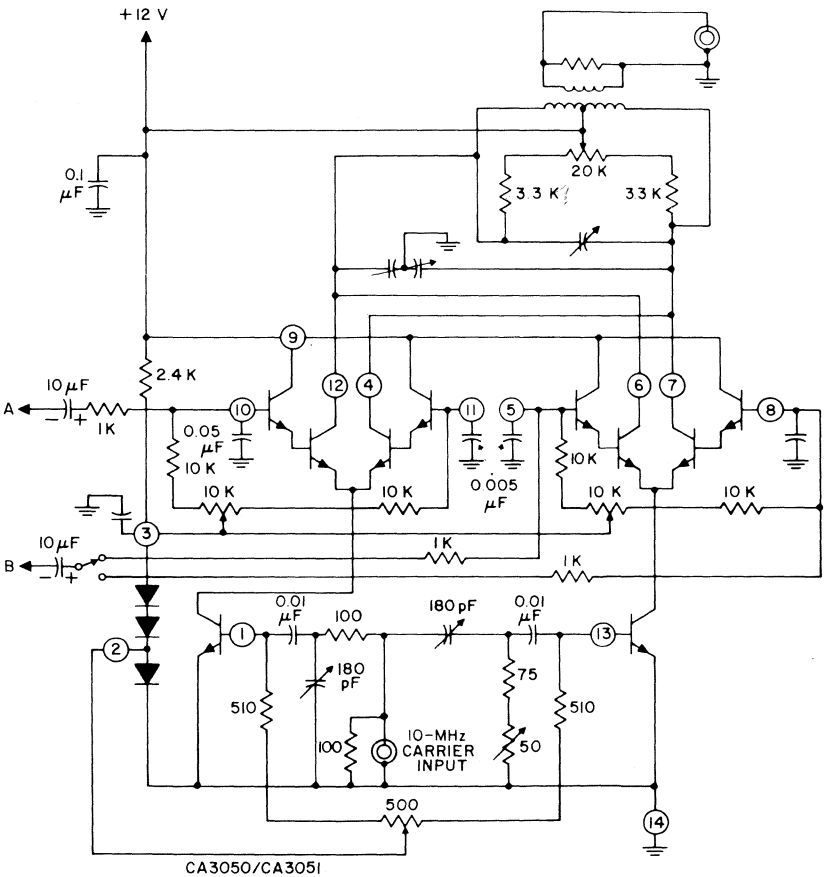


All resistance values in ohms unless otherwise specified.

Fig. 439 — Single-sideband phase-shift modulator using the CA3050 or CA3051.
(Continued on page 337)

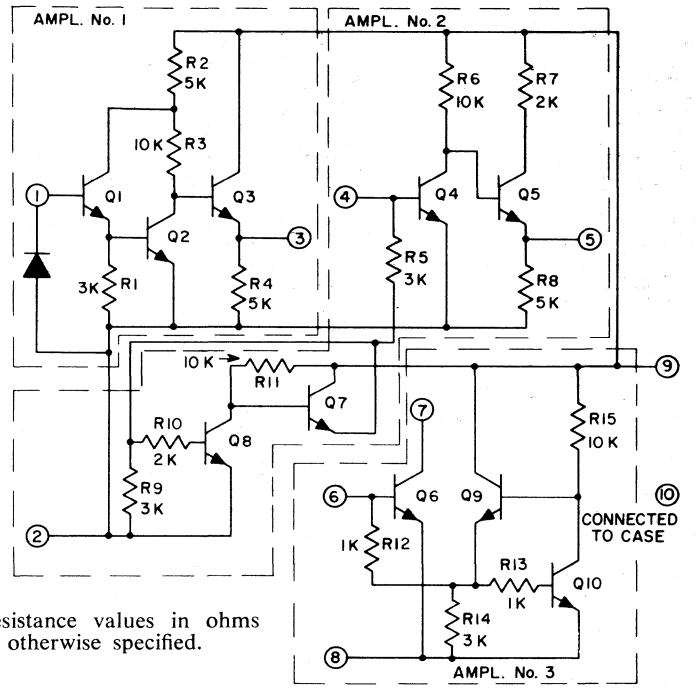
dB-per-octave roll-off at very low frequencies results from the divider action between the capacitive source impedance and the resistive termination of the first stage.

The second stage consists of a grounded-emitter amplifier followed by an emitter follower. The collector current in the input transistor of this stage (Q4 in Fig. 439) is regulated by an internal supply, and the gain of this stage is determined by the value of the resistor R6. The voltage gain, approximately 40 dB, is independent of temperature and transistor beta values. The emitter follower serves as an impedance transformer, and its output is fed to the third stage by means of the external coupling capacitor connected from terminal 5 to terminal 6. The last stage consists of a single grounded-emitter transistor together with a reference supply to control its collector



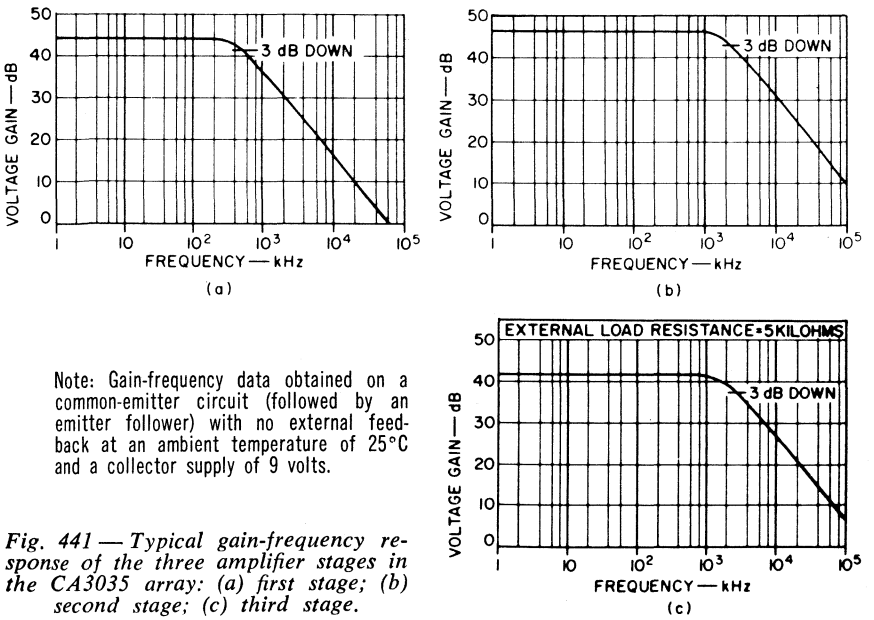
All resistance values in ohms unless otherwise specified.

Fig. 439 — Single-sideband phase-shift modulator using the CA3050 or CA3051.
(Continued from page 336)



All resistance values in ohms unless otherwise specified.

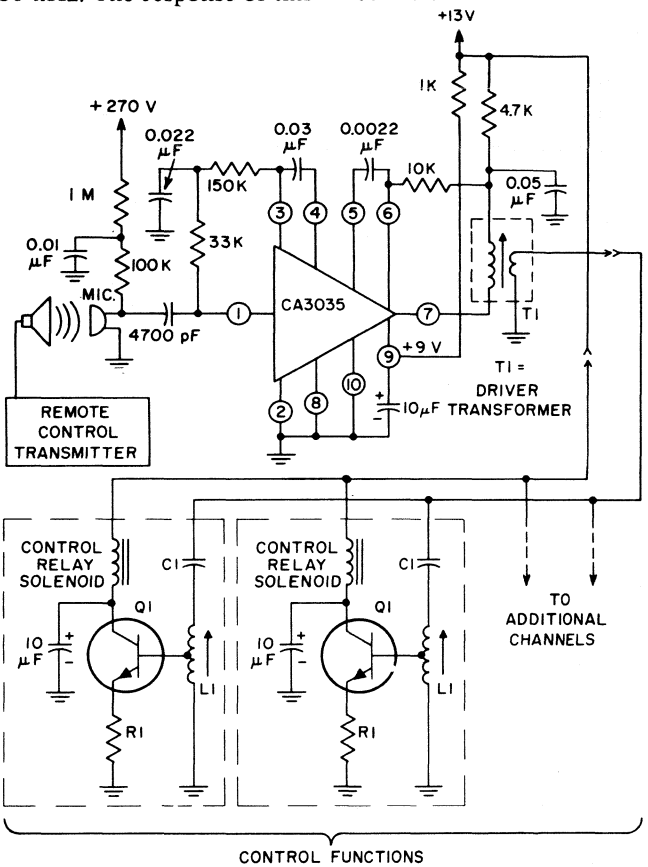
Fig. 440 — CA3035 integrated-circuit wide-band amplifier array.



Note: Gain-frequency data obtained on a common-emitter circuit (followed by an emitter follower) with no external feedback at an ambient temperature of 25°C and a collector supply of 9 volts.

Fig. 441 — Typical gain-frequency response of the three amplifier stages in the CA3035 array: (a) first stage; (b) second stage; (c) third stage.

current. The collector of the transistor is terminated in an output transformer which resonates with its collector capacitance and stray capacitance at a frequency of approximately 180 kHz. The response of this stage is shown in Fig. 444. The secondary winding of the output transformer feeds eight tuned circuits. These circuits correspond to the eight tuned circuits in the television receiver.



All resistance values in ohms unless otherwise specified.

Fig. 442 — Block diagram of a typical remote-control system using the CA3035.

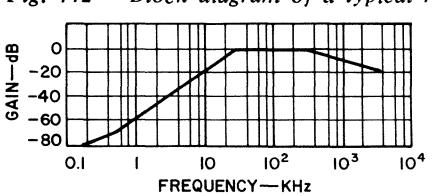


Fig. 443 — Frequency response of the first stage of the remote-control system shown in Fig. 442.

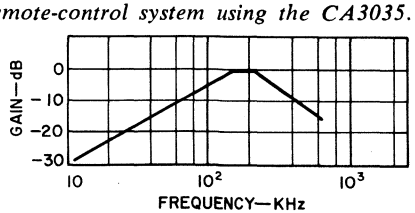


Fig. 444 — Frequency response of the third stage of the remote-control system shown in Fig. 442.

Application Guide

In the following Application Guide, RCA linear integrated circuits are classified by function and by package configuration. Circuit types are grouped according to package configuration under each functional classification. This Guide is particularly useful for an initial selection of suitable circuits for a specific application. More complete data on these circuits, given in the **Technical Data** section of this Manual or in the individual RCA Technical Bulletins, should then be consulted to determine the most suitable type.

Analog Switch

10-LEAD TO-5-STYLE
CA3019

12-LEAD TO-5-STYLE
CA3039

16-LEAD DUAL-IN-LINE CERAMIC
CA3060

Audio Amplifier

8-LEAD TO-5-STYLE
CA3028A CA3028B

10-LEAD TO-5-STYLE
CA3000 CA3035 CA3036
CA3002

10-FORMED-LEAD TO-5-STYLE
CA3035VI

12-LEAD TO-5-STYLE
CA3001 CA3018 CA3022
CA3004 CA3018A CA3023
CA3005 CA3020 CA3026
CA3006 CA3020A
CA3007 CA3021

14-LEAD DUAL-IN-LINE PLASTIC
CA3046

14-LEAD DUAL-IN-LINE CERAMIC
CA3045

16-LEAD DUAL-IN-LINE PLASTIC
CA3048 CA3052

Comparator

8-LEAD TO-5-STYLE
CA3056A

10-LEAD TO-5-STYLE
CA3000

12-LEAD TO-5-STYLE
CA3010 CA3015 CA3018
CA3010A CA3015A CA3018A

14-LEAD FLAT-PACK
CA3008 CA3008A

14-LEAD DUAL-IN-LINE PLASTIC
CA3029 CA3030 CA3047
CA3029A CA3030A CA3047A

14-LEAD DUAL-IN-LINE CERAMIC
CA3033 CA3037 CA3038
CA3033A CA3037A CA3038A

16-LEAD DUAL-IN-LINE CERAMIC
CA3060

DC Amplifier

8-LEAD TO-5-STYLE
CA3028B CA3056A

10-LEAD TO-5-STYLE
CA3000

12-LEAD TO-5-STYLE
CA3001 CA3006 CA3018A
CA3005 CA3018 CA3026

14-LEAD DUAL-IN-LINE CERAMIC
CA3045

14-LEAD DUAL-IN-LINE PLASTIC
CA3046 CA3054

Detector: AM, FM, Phase, Product

10-LEAD TO-5-STYLE
CA3002 CA3014 CA3034
CA3013 CA3019 CA3044

10-FORMED-LEAD TO-5-STYLE
CA3034VI CA3044VI CA3064

12-LEAD TO-5-STYLE
CA3004 CA3018 CA3039
CA3005 CA3018A CA3043
CA3006 CA3026 CA3049

14-LEAD DUAL-IN-LINE PLASTIC
CA3041 CA3046 CA3054
CA3042 CA3051 CA3065

14-LEAD DUAL-IN-LINE CERAMIC
CA3045 CA3050

Differential Amplifier

8-LEAD TO-5-STYLE
CA3028A CA3028B CA3053

10-LEAD TO-5-STYLE
CA3000 CA3002

12-LEAD TO-5-STYLE
CA3001 CA3006 CA3026
CA3004 CA3018 CA3040
CA3005 CA3018A CA3049

14-LEAD DUAL-IN-LINE PLASTIC
CA3046 CA3051 CA3054
14-LEAD DUAL-IN-LINE CERAMIC
CA3045 CA3050

FM IF Amplifier-Limiter

10-LEAD TO-5-STYLE
CA3011 CA3012
12-LEAD TO-5-STYLE
CA3043

FM-IF, Limiter, Detector, Audio

12-LEAD TO-5-STYLE
CA3043

IF Amplifier

8-LEAD TO-5-STYLE
CA3028A CA3053 CA3076
CA3028B
10-LEAD TO-5-STYLE
CA3002 CA3012 CA3014
CA3011 CA3013 CA3035
10-FORMED-LEAD TO-5-STYLE
CA3035VI
12-LEAD
CA3001 CA3018A CA3040
CA3004 CA3021 CA3043
CA3005 CA3022 CA3049
CA3006 CA3023
CA3018 CA3026
14-LEAD DUAL-IN-LINE PLASTIC
CA3041 CA3046 CA3065
CA3042 CA3054
14-LEAD DUAL-IN-LINE CERAMIC
CA3045

Limiter

8-LEAD TO-5-STYLE
CA3028A CA3028B CA3053
10-LEAD TO-5-STYLE
CA3011 CA3013 CA3019
CA3012 CA3014
12-LEAD TO-5-STYLE
CA3004 CA3018A CA3026
CA3005 CA3021 CA3039
CA3006 CA3022 CA3043
CA3018 CA3023 CA3049
14-LEAD DUAL-IN-LINE PLASTIC
CA3041 CA3046 CA3065
CA3042 CA3054
14-LEAD DUAL-IN-LINE CERAMIC
CA3045

Mixer: AF, RF

10-LEAD TO-5-STYLE
CA3000 CA3002
12-LEAD TO-5-STYLE
CA3001 CA3006 CA3026
CA3004 CA3018 CA3040
CA3005 CA3018A CA3049
14-LEAD DUAL-IN-LINE PLASTIC
CA3046 CA3051 CA3054
14-LEAD DUAL-IN-LINE CERAMIC
CA3045 CA3050
16-LEAD DUAL-IN-LINE PLASTIC
CA3048 CA3052
16-LEAD DUAL-IN-LINE CERAMIC
CA3060

Modulator

8-LEAD TO-5-STYLE
CA3028A CA3028B
10-LEAD TO-5-STYLE
CA3000 CA3002 CA3019
12-LEAD TO-5-STYLE
CA3001 CA3018 CA3039
CA3004 CA3018A CA3040
CA3005 CA3026 CA3049
CA3006
14-LEAD DUAL-IN-LINE CERAMIC
CA3045 CA3050
14-LEAD DUAL-IN-LINE PLASTIC
CA3046 CA3051 CA3054

Multivibrator

8-LEAD TO-5-STYLE
CA3056A
10-LEAD TO-5-STYLE
CA3000
12-LEAD TO-5-STYLE
CA3001 CA3015 CA3018A
CA3010 CA3015A CA3026
CA3010A CA3018 CA3049
14-LEAD DUAL-IN-LINE PLASTIC
CA3029 CA3030A CA3047A
CA3029A CA3046 CA3051
CA3030 CA3047 CA3054
14-LEAD DUAL-IN-LINE CERAMIC
CA3033 CA3045 CA3050
CA3033A
16-LEAD DUAL-IN-LINE PLASTIC
CA3048 CA3060

Operational Amplifier

8-LEAD TO-5-STYLE
CA3031 CA3032 CA3056A
12-LEAD TO-5-STYLE
CA3010 CA3015 CA3015A
CA3010A
14-LEAD FLAT PACK
CA3008 CA3016 CA3016A
CA3008A
14-LEAD DUAL-IN-LINE PLASTIC
CA3029 CA3030 CA3047
CA3029A CA3030A CA3047A
14-LEAD DUAL-IN-LINE CERAMIC
CA3033 CA3037 CA3038
CA3033A CA3037A CA3038A
16-LEAD DUAL-IN-LINE CERAMIC
CA3060

Oscillator

8-LEAD TO-5-STYLE
CA3028A CA3028B CA3053
10-LEAD TO-5-STYLE
CA3000 CA3002
12-LEAD TO-5-STYLE
CA3001 CA3018 CA3020A
CA3004 CA3018A CA3026
CA3005 CA3020 CA3049
CA3006
14-LEAD DUAL-IN-LINE PLASTIC
CA3046 CA3054
14-LEAD DUAL-IN-LINE CERAMIC
CA3045
16-LEAD DUAL-IN-LINE CERAMIC
CA3048 CA3052

RF Amplifier

8-LEAD TO-5-STYLE
CA3028A CA3028B
12-LEAD TO-5-STYLE
CA3004 CA3018 CA3026
CA3005 CA3018A CA3049
CA3006
14-LEAD DUAL-IN-LINE PLASTIC
CA3046 CA3054
14-LEAD DUAL-IN-LINE CERAMIC
CA3045

Schmitt Trigger

8-LEAD TO-5-STYLE
CA3028A CA3028B CA3053
10-LEAD TO-5-STYLE
CA3000 CA3002
12-LEAD TO-5-STYLE
CA3001 CA3018A CA3040
CA3018 CA3026 CA3049
14-LEAD DUAL-IN-LINE PLASTIC
CA3046 CA3051 CA3054
14-LEAD DUAL-IN-LINE CERAMIC
CA3045 CA3050

Sense Amplifier

8-LEAD TO-5-STYLE
CA3028 CA3028A
10-LEAD TO-5-STYLE
CA3000 CA3002
12-LEAD TO-5-STYLE
CA3001 CA3006 CA3026
CA3004 CA3018 CA3040
CA3005 CA3018A CA3049
14-LEAD DUAL-IN-LINE CERAMIC
CA3045 CA3050
14-LEAD DUAL-IN-LINE PLASTIC
CA3046 CA3051 CA3054

Stereo Preamplifier

16-LEAD DUAL-IN-LINE PLASTIC
CA3052

Switching: Analog, Power

10-LEAD TO-5-STYLE
CA3019
12-LEAD TO-5-STYLE
CA3020 CA3020A CA3039

Television: Automatic Fine Tuning

10-LEAD TO-5-STYLE
CA3034 CA3044
10-FORMED-LEAD TO-5-STYLE
CA3034VI CA3044VI CA3064

Television: Remote Control Amplifier

10-LEAD TO-5-STYLE
CA3035

Television: Sound IF, Detector, Audio

10-LEAD TO-5-STYLE
CA3013 CA3014
14-LEAD DUAL-IN-LINE PLASTIC
CA3041 CA3042 CA3065

Thyristor Control

12-LEAD TO-5-STYLE
CA3059

Video Amplifier

8-LEAD TO-5-STYLE
CA3028A CA3028B CA3053
10-LEAD TO-5-STYLE
CA3002
12-LEAD TO-5-STYLE
CA3001 CA3018 CA3026
CA3004 CA3018A CA3040
CA3005 CA3020 CA3049
CA3006 CA3020A
14-LEAD DUAL-IN-LINE CERAMIC
CA3045
14-LEAD DUAL-IN-LINE PLASTIC
CA3046 CA3054

Voltage Regulator

8-LEAD TO-5-STYLE
CA3055

Technical Data

This section lists ratings and typical operating characteristics for current RCA linear integrated circuits. These data provide a convenient, readily accessible source of information that is useful in the selection of the optimum circuit type for a particular application. For complete descriptive data on specific circuits being considered, as well as information on test setups and methods used to determine circuit operating characteristics, the prospective user should consult the RCA technical bulletins for individual types. Because the technical bulletins are frequently updated to include the latest available circuit information, reference to the appropriate bulletin is an important step in any proposed application of RCA linear integrated circuits.

Circuits are listed in this section according to the alphabetical-numerical sequence of their type designations. Unless otherwise specified, voltage and currents are dc values, and values are obtained at an ambient temperature of 25°C. For convenience of reference, diagrams are included with the data for each type to show external terminal connections and the functional relationship among internal circuit elements. The detailed circuit diagrams for each type are shown in the text section of the Manual or in the RCA technical bulletin for the specific type.

Maximum circuit ratings shown are based on the **Absolute Maximum** system and are limiting values of operating and environmental conditions that should not be exceeded by and circuit of a specified type under any conditions of operation. Effective use of these ratings requires close control of supply-voltage variations, component variations, equipment-control adjustment, load variations, and environmental conditions.

The characteristic data represent the characteristics of an average circuit. Individual circuits may have characteristics that range above or below the typical values listed for the specific circuit type.

CA3000 DC AMPLIFIER

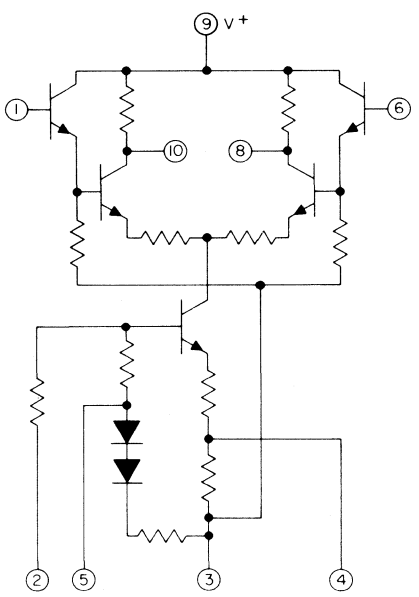
General-purpose amplifier used in Schmitt-trigger, RC-coupled feedback-amplifier, mixer, comparator, crystal-oscillator, sense-amplifier, and modulator applications. 10-lead JEDEC MO-006-AF package; Outline No. 1.

MAXIMUM RATINGS

Positive DC Supply Voltage	V^+	+10	V
Negative DC Supply Voltage	V^-	−10	V
Input Signal Voltage:			
Single-ended		±2	V
Common-mode		±2	V
Total Device Dissipation		300	mW
Temperature Range:			
Operating		−55 to +125	°C
Storage		−65 to +200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = +6V, V^- = −6V)

Static Characteristics			
Input Offset Voltage	V_{IO}	1.4 typ; 8 max	mV
Input Offset Current	I_{IO}	1.2 typ; 10 max	μA
Input Bias Current	I_I	23 typ; 36 max	μA
Quiescent Operating Voltage:			
Terminals 4 and 5 not connected	V_8 or V_{10}	2.6	V
Terminal 4 not connected, terminal 5 connected to V^-	V_8 or V_{10}	4.2	V
Terminal 4 connected to V^-, terminal 5 not connected	V_8 or V_{10}	−1.5	V
Terminals 4 and 5 connected to V^-	V_8 or V_{10}	0.6	V
Device Dissipation	P_T	30	mW



Dynamic Characteristics

Differential Voltage Gain (Single-Ended Input, f = 1 kHz):			
Single-ended output	A_{DIFF}	28 min; 32 typ	dB
Double-ended output	A_{DIFF}	37	dB
—3-dB Bandwidth	BW	650	kHz
Maximum Output-Voltage Swing (f = 1 kHz)	V_{out}(P-P)	6.4	V
Common-Mode Rejection Ratio (f = 1 kHz)	CMRR	80 min; 98 typ	dB
Single-Ended Input Impedance (f = 1 kHz)	Z_{in}	70 min; 195	kΩ
Single-Ended Output Impedance (f = 1 kHz)	Z_{out}	5.5 to 10.5	kΩ
Total Harmonic Distortion (f = 1 kHz)	THD	0.2 typ; 5 max	%
AGC Range (Maximum voltage gain to complete cutoff, f = 1 kHz)	AGC	80 min; 90 typ	dB

VIDEO AND WIDE-BAND AMPLIFIER — CA3001

General-purpose amplifier used in dc, if, and video amplifier, Schmitt-trigger, mixer, and modulation applications. 12-lead JEDEC MO-006-AG package; Outline No. 2.

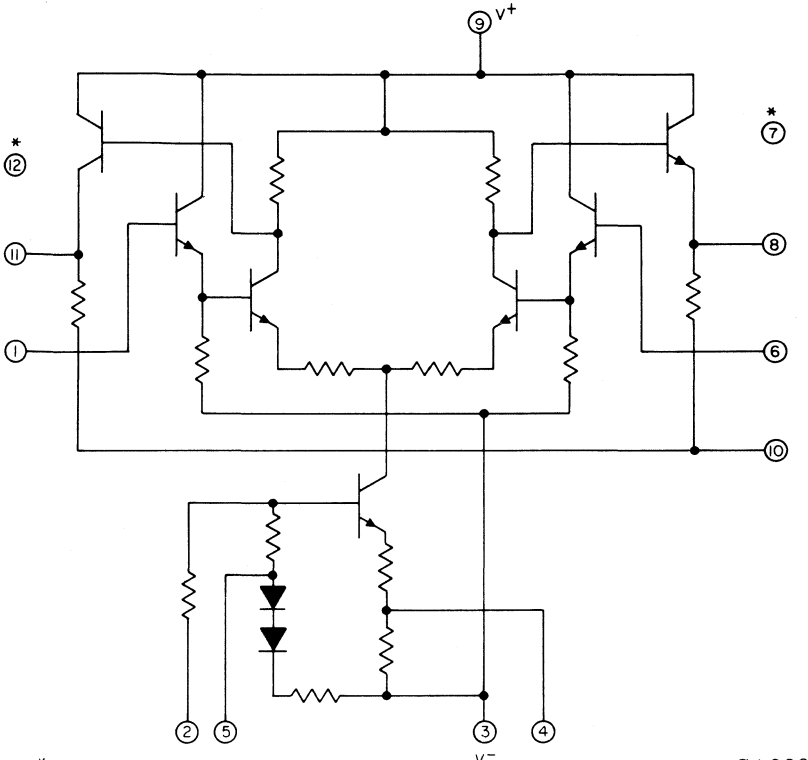
MAXIMUM RATINGS

Positive DC Supply Voltage	V^+	+10	V
Negative DC Supply Voltage	V^-	−10	V
Input Signal Voltage			
Single-ended		±2.5	V
Common-mode		±2.5	V
Total Device Dissipation		300	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = +6V, V^- = −6V)

Static Characteristics

Input Offset Voltage	V_{IO}	1.5	mV
Input Offset Current	I_{IO}	1 typ; 10 max	μA
Input Bias Current	I_I	16 typ; 36 max	μA
Output Offset Voltage	V_{OO}	54 typ; 300 max	mV
Quiescent Operating Voltage:			
Terminals 4 and 5 not connected	V_8 or V_{11}	3.8 to 5	V
Terminal 4 not connected, terminal 5 connected to V^-	V_8 or V_{11}	4.8	V
Terminal 4 connected to V^-, terminal 5 not connected	V_8 or V_{11}	2.7	V
Terminals 4 and 5 connected to V^-	V_8 or V_{11}	4	V
Device Dissipation:			
Terminals 4 and 5 not connected	P_T	60 to 120	mW
Terminal 4 not connected, terminal 5 connected to V^-	P_T	71	mW
Terminal 4 connected to V^-, terminal 5 not connected	P_T	110	mW
Terminals 4 and 5 connected to V^-	P_T	86	mW



* INTERNAL CONNECTION — DO NOT USE

CA3001

Dynamic Characteristics

Differential Voltage Gain (Single-ended input and output):			
f = 1.75 MHz	A_{DIFF}	16 min; 19 typ	dB
f = 20 MHz	A_{DIFF}	10 min; 14 typ	dB
—3-dB Bandwidth	BW	16 min; 29 typ	MHz
Maximum Output Voltage Swing (f = 1.75 MHz)	V_{out} (P-P)	5	V
Noise Figure:			
R_S = 1 kΩ, f = 1.75 MHz	NF	5	dB
R_S = 1 kΩ, f = 11.7 MHz	NF	7.7	dB
Common-Mode Rejection Ratio (f = 1 kHz)	CMRR	70 min; 88 typ	dB
Parallel Input Resistance (f = 1.75 MHz)	R_{in}	50 min; 140 typ	kΩ
Parallel Input Capacitance (f = 1.75 MHz)	C_{in}	3.4 typ; 7 max	pF
Output Resistance (f = 1.75 MHz)	R_{out}	45 typ; 70 max	Ω
AGC Range (Maximum voltage gain to complete cutoff, f = 1.75 MHz)	AGC	55 min; 60 typ	dB

CA3002 IF AMPLIFIER

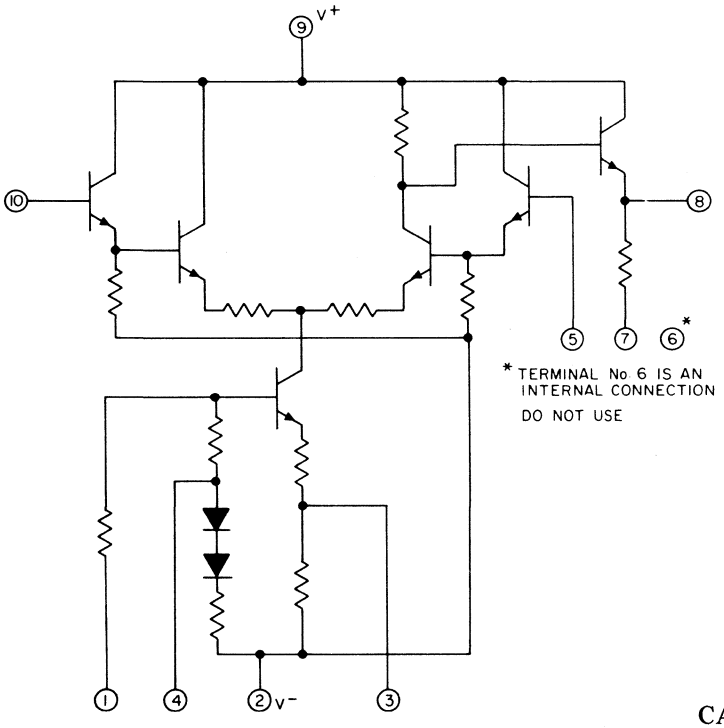
General-purpose amplifier used in video amplifier, product and AM detector applicatons. 10-lead JEDEC MO-006-AF package; Outline No. 1.

MAXIMUM RATINGS

Positive DC Supply Voltage	V^+	+10	V
Negative DC Supply Voltage	V^-	−10	V
Input Signal Voltage (Single-ended)		±3.5	V
Total Device Dissipation		300	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = +6V, V^- = −6V)

Static Characteristics			
Input Unbalance Voltage	V_{IU}	2.2	mV
Input Unbalance Current	I_{IU}	2.2typ; 10 max	μA
Input Bias Current	I_I	20 typ; 36 max	μA
Quiescent Operating Voltage:			
Terminal 2 connected to V^-, terminal 4 not connected		2.8	V
Terminals 2 and 4 connected to V^-		3.9	V
Device Dissipation	P_T	55	mW
Dynamic Characteristics			
Differential Voltage Gain (Single-Ended Input and Output, f = 1.75 MHz)	A_{DIFF}	19 min; 24 typ	dB
—3-dB Bandwidth	BW	11	MHz
Maximum Output Voltage Swing	V_{out}(P-P)	5.5	V
Noise Figure (R_S = 1 kΩ, f = 1.75 MHz)	NF	4 typ; 8 max	dB



CA3002

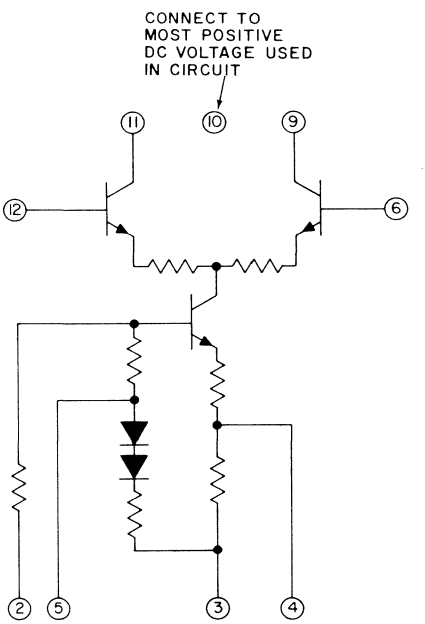
Parallel Input Resistance (f = 1.75 MHz)	R_{in}	100	kΩ
Parallen Input Capacitance (f = 1.75 MHz)	C_{in}	4	pF
Output Resistance (f = 1.75 MHz)	R_{out}	70	Ω
3rd Harmonic Intermodulation Distortion	IMD	−30 min; −40 typ	dB
AGC Range (Maximum Voltage Gain to Complete Cutoff, f = 1.75 MHz)	AGC	60 min; 80 typ	dB

CA3004 RF AMPLIFIER

General-purpose amplifier used in push-pull input and output, wide- and narrow-band amplifier, agc, detector, mixer, limiter, and modulator applications. 12-lead JEDEC MO-006-AG package; Outline No. 2.

MAXIMUM RATINGS

Positive DC Supply Voltage	V^+	+12	V
Negative DC Supply Voltage	V^-	−12	V
Input Signal Voltage:			
Single-ended		±3.5	V
Common-mode		−2.5 +3.5	V
Total Device Dissipation		300	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C



CA3004

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, $V^+ = +6V$, $V^- = -6V$)

Static Characteristics			
Input Offset Voltage	V_{IO}	1.7 typ; 5 max	mV
Input Offset Current	I_{IO}	0.125 typ; 5 max	μA
Input Bias Current	I_I	21 typ; 40 max	μA
Quiescent Operating Current:			
Terminals 4 and 5 not connected	I_9 or I_{11}	1	mA
Terminal 4 connected to V^-, terminal 5 not connected	I_9 or I_{11}	2.7	mA
Terminal 4 not connected, terminal 5 connected to V^-	I_9 or I_{11}	0.45	mA
Terminals 4 and 5 connected to V^-	I_9 or I_{11}	1.25	mA
Quiescent Operating Current Ratio	I_9/I_{11}	1.1	
Device Dissipation	P_T	26	mW
Dynamic Characteristics			
Power Gain (f = 100 MHz)	G_P	10 min; 12 typ	dB
Noise Figure (f = 100 MHz)	NF	6.3 typ; 9 max	dB
Common-Mode Rejecton Ratio (f = 1 kHz)	CMRR	98	dB
AGC Range (Maximum Voltage Gain to Complete Cutoff, f = 1.75 MHz)	AGC	−60 min	dB

RF AMPLIFIER CA3005

General-purpose amplifier used in push-pull input and output, wide- and narrow-band amplifier, agc, detector, mixer, limiter, modulator, and cascode amplifier applications. 12-lead JEDEC MO-006-AG package; Outline No. 2.

MAXIMUM RATINGS

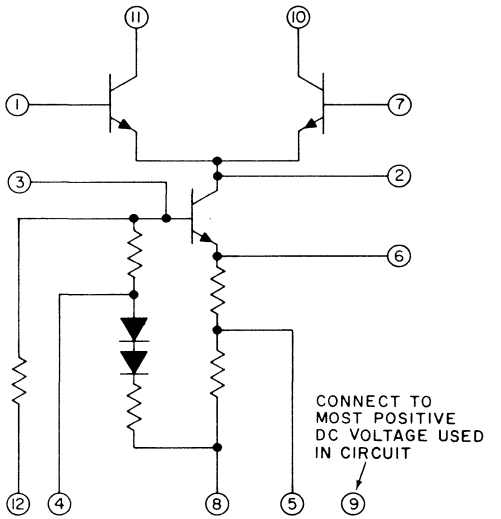
Positive DC Supply Voltage	V^+	+12	V
Negative DC Supply Voltage	V^-	−12	V
Input Signal Voltage:			
Single-ended		±3.5	V
Common-mode		−2.5 +3.5	V
Total Device Dissipation		300	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, $V^+ = +6V$, $V^- = -6V$)

Static Characteristics			
Input Offset Voltage	V_{IO}	2.6 typ; 5 max	mV
Input Offset Current	I_O	1.4	μA
Input Bias Current	I_I	19 typ; 40 max	μA
Quiescent Operating Current:			
Terminals 4 and 5 not connected	I_{10} or I_{11}	1	mA
Terminal 4 not connected, terminal 5 connected to V^-	I_{10} or I_{11}	2.7	mA
Terminal 4 connected to V^-, terminal 5 not connected	I_{10} or I_{11}	0.45	mA
Terminals 4 and 5 connected to V^-	I_{10} or I_{11}	1.25	mA
Quiescent Operating Current Ratio	I_{10}/I_{11}	1.05	
Device Dissipation	P_T	26	mW
Dynamic Characteristics			
Power Gain (f = 100 MHz):			
Cascode circuit	G_P	16 min; 20 typ	dB
Differential-amplifier circuit	G_P	14 min; 16 typ	dB

Noise Figure (f = 100 MHz):			
Cascode circuit	NF	7.8 typ; 9 max	dB
Differential-amplifier circuit	NF	7.8 typ; 9 max	dB
Common-Mode Rejection Ratio (f = 1 kHz)	CMRR	101	dB
AGC Range (Maximum Voltage Gain to Complete Cutoff, f = 1.75 MHz)	AGC	−60 min	dB

CA3005
OR
CA3006



CA3006 RF AMPLIFIER

General-purpose amplifier used in push-pull input and output, wide- and narrow-band amplifier, agc, detector, mixer, limiter, modulator, and cascode amplifier applications. 12-lead "TO-5" package; Outline No. 2. This type is identical with type CA3005 except for the following item:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, $V^+ = +6V$, $V^- = -6V$)

Static Characteristics			
Input Offset Voltage	V_{IO}	0.8 typ; 1 max	mV

CA3008 OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead ceramic-and-metal flat JEDEC MO-004-AF package; Outline No. 3.

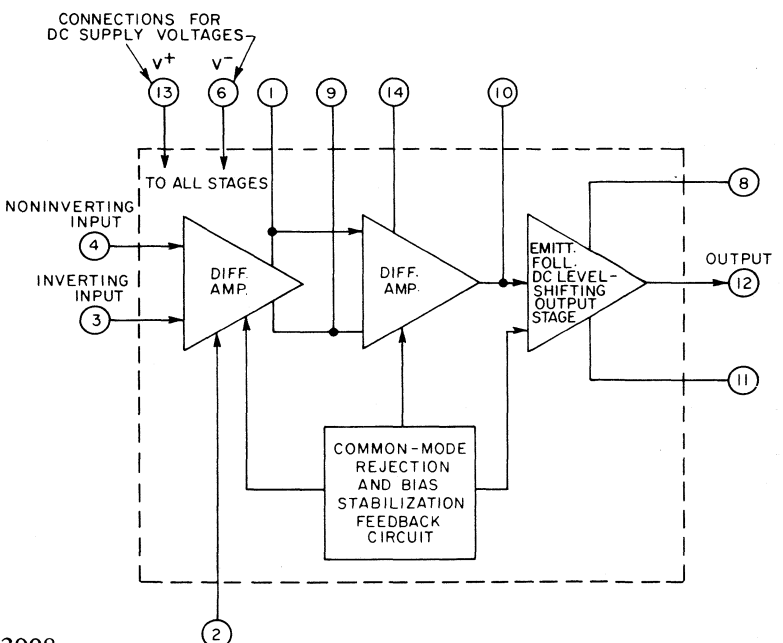
MAXIMUM RATINGS

Positive DC Supply Voltage	V^+	+10
Negative DC Supply Voltage	V^-	−10

Input Signal Voltage (Single-ended)	+1, −4	V
Total Device Dissipation	300	mW
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, $V^+ = +6V$, $V^- = -6V$)

Static Characteristics			
Input Offset Voltage	V_{IO}	1.08 typ; 5 max	mV
Input Offset Current	I_{IO}	0.54 typ; 5 max	μA
Input Bias Current	I_I	5.3 typ; 12 max	μA
Input Offset Voltage Sensitivity:			
Positive	$\Delta V_{IO}/\Delta V_{CC}$	0.10 typ; 1 max	mV/V
Negative	$\Delta V_{IO}/\Delta V_{EE}$	0.26 typ; 1 max	mV/V
Device Dissipation:			
Terminal 8 not connected	P_T	30	mW
Terminal 8 shorted to terminal 12	P_T	102	mW
Dynamic Characteristics			
Open-Loop Differential Voltage Gain (f = 1 kHz)	A_{OL}	57 min; 60 typ	dB
Open-Loop —3-dB Bandwidth	BW_{OL}	200 min; 300 typ	kHz
Common-Mode Rejection Ratio (f = 1 kHz)	CMRR	70 min; 94 typ	dB
Maximum Output-Voltage Swing (f = 1 kHz)	V_O(P-P)	4 min; 6.75 typ	V
Input Impedance (f = 1 kHz)	Z_{in}	10 min; 14 typ	kΩ
Output Impedance (f = 1 kHz)	Z_{out}	200	Ω
Common-Mode Input-Voltage Range (f = 1 kHz)	V_{CMR}	+0.5, −4	V



CA3008

CA3008A OPERATIONAL AMPLIFIER

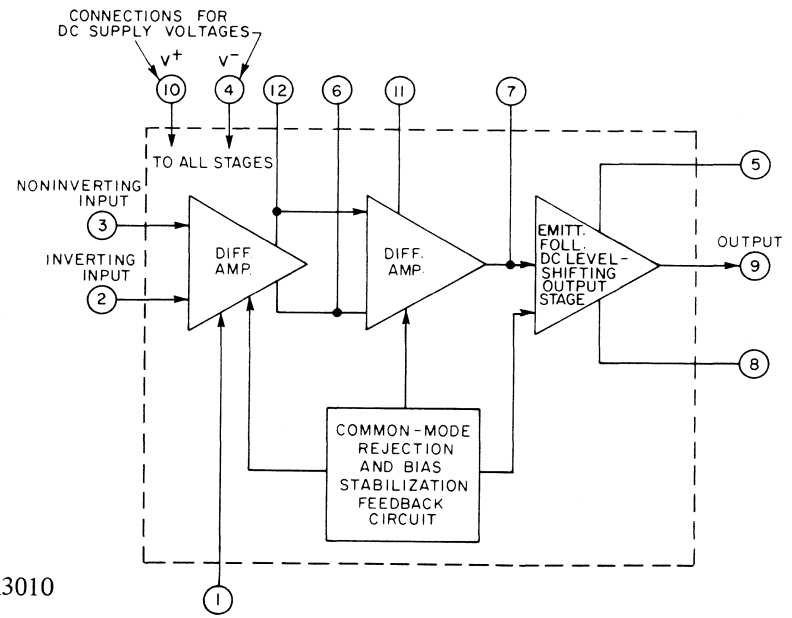
General-purpose amplifier used in narrow-band and bandpass amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead JEDEC MO-004-AF package; Outline No. 3. This type is identical with type CA3008 except for the following items:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, $V^+ = 6V$, $V^- = -6V$)

Static Characteristics			
Input Offset Voltage	V_{IO}	0.9 typ; 2 max	mV
Input Offset Current	I_{IO}	0.3 typ; 1.5 max	μA
Input Bias Current	I_I	2.5 typ; 4 max	μA
Device Dissipation	P_T	40	mW
Device Dissipation (Terminal 5 shorted to terminal 9)	P_T	102	mW
Dynamic Characteristics (f = 1 kHz except BW_{OL})			
Slew Rate (R_S = 1 kΩ)	SR	3	V/μs
Maximum Output-Voltage Swing	V_O(P-P)	6.75	V
Input Impedance	Z_{IN}	15 min; 20 typ	kΩ
Output Impedance	Z_{OUT}	160	Ω
Common-Mode Input-Voltage Range	V_{CMR}	0.5 to −4	V
Noise Figure (R_S = 1 kΩ):			
V = 3V, V = −3V	NF	6.3 typ; 9 max	dB
V = 6V, V = −6V	NF	8.3 typ; 12 max	dB

CA3010 OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, com-



CA3010

parator, and servo driver applications. 12-lead JEDEC MO-006-AG package; Outline No. 2. This type is electrically identical with type CA3008.

OPERATIONAL AMPLIFIER — CA3010A

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 12-lead JEDEC MO-006-AG package; Outline No. 2. This type is electrically identical with type CA3008A. The functional diagram for this type is identical to that of type CA3010.

FM IF AMPLIFIER — CA3011

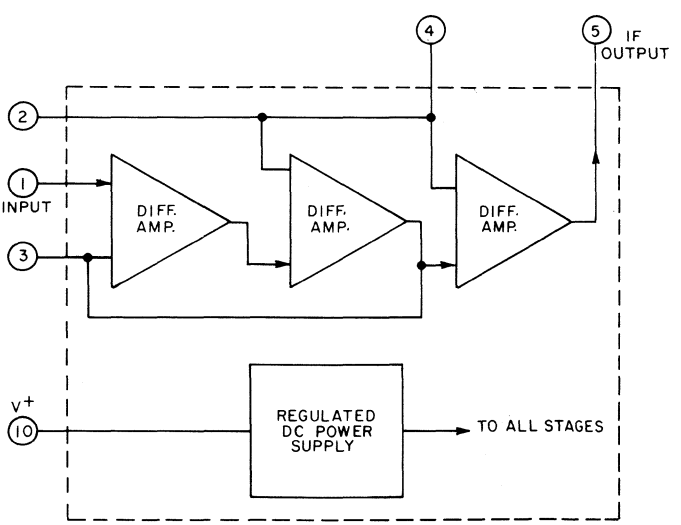
Special-purpose amplifier used in if amplifiers for FM broadcast and TV sound applications. 10-lead JEDEC MO-006-AF package; Outline No. 1.

MAXIMUM RATINGS

Positive DC Supply Voltage	V^+	+10	V
Recommended Minimum DC Supply Voltage (V^+)		5.5	V
Input Signal Voltage (Single-ended)		±3	V
Total Device Dissipation		300	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = +7.5V)

Device Dissipation*	P_T	95 to 187	mW
Voltage Gain:‡			
f = 1 MHz	A	65 min; 70 typ	dB
f = 4.5 MHz	A	60 min; 67 typ	dB
f = 10.7 MHz	A	55 min; 61 typ	dB



'A3011 OR 'A3012

Parallel Input Resistance (f = 4.5 MHz)	R_{in}	3	kΩ
Parallel Input Capacitance (f = 4.5 MHz)	C_{in}	7	pF
Parallel Output Resistance (f= 4.5 MHz)	R_{out}	31.5	kΩ
Parallel Output Capacitance (f = 4.5 MHz)	C_{out}	4.2	pF
Noise Figure (f = 4.5 MHz)	NF	8.7	dB
Input Limiting Voltage, Knee (f = 4.5 MHz)	V_i(lim)	300	μV

* The total current drain may be determined by dividing P_T by V^+.
‡ Recommended minimum dc supply voltage (V^+) is 5.5 V. Nominal load current flowing into terminal 5 is 1.5 mA at 7.5 V.

CA3012 FM IF AMPLIFIER

Special-purpose amplifier used in if amplifiers for FM broadcast and TV sound applications. 10-lead JEDEC MO-006-AF package; Outline No. 1. This type is electrically identical with type CA3011 except for the following items:

MAXIMUM RATINGS

Positive DC Supply Voltage	V^+	+13	V

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = +7.5V)

Device Dissipation*	P_T	97 to 167	mW

* The total current drain may be determined by dividing P_T by V^+.

CA3013 FM IF AMPLIFIER/ DISCRIMINATOR/AF AMPLIFIER

Special-purpose amplifier used in if amplifier, AM and noise limiter, FM detector, and af preamplifier applications. 10-lead JEDEC MO-006-AF package; Outline No. 1.

MAXIMUM RATINGS

Positive DC Supply Voltage	V^+	+10	V
Recommended Minimum DC Supply Voltage (V^+)		5.5	V
Input Signal Voltage (Between terminals 1 and 2)		±3	V
Total Device Dissipation		300	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

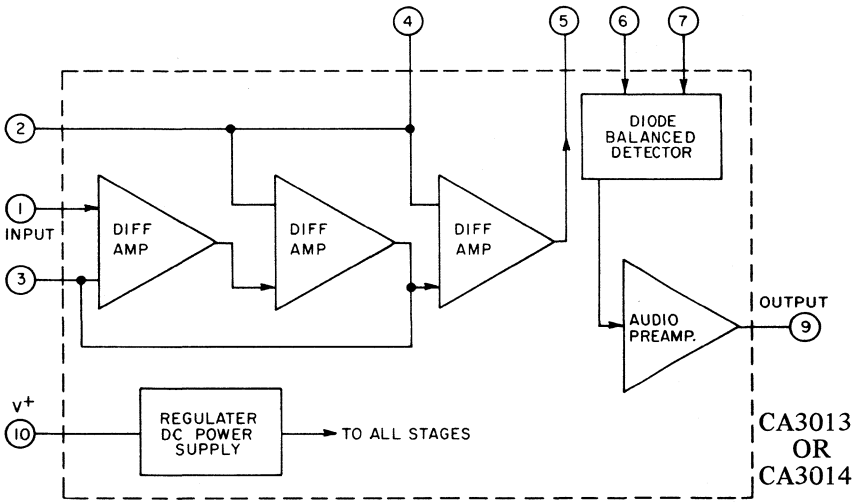
TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = +7.5V)

Device Dissipation*	P_T	87 to 187	mW
Voltage Gain:‡			
f = 1 MHz	A	65 min; 70 typ	dB
f = 4.5 MHz	A	60 min; 67 typ	dB
f = 10.7 MHz	A	55 min; 60 typ	dB
Parallel Input Resistance (f = 4.5 MHz)	R_{in}	3	kΩ

Parallel Input Capacitance (f = 4.5 MHz)	C_{in}	7	pF
Parallel Output Resistance (f = 4.5 MHz)	R_{out}	31.5	kΩ
Parallel Output Capacitance (f = 4.5 MHz)	C_{out}	4.2	pF
Noise Figure (f = 4.5 MHz)	NF	8.7	dB
Input Limiting Voltage, Knee (f = 4.5 MHz)	V_i(lim)	300 typ; 450 max	μV
Recovered AF Voltage (f = 4.5 MHz)	V_o(af)	128 min; 188 typ	mV
Amplitude Modulation Rejection (f = 4.5 MHz)	AMF	50	dB
Discriminator Output Resistance (f = 4.5 MHz)	R_o(disc)	60	Ω
Total Harmonic Distortion (f = 4.5 MHz)	THD	1.8	%

* The total current drain may be determined by dividing P_T by V^+.

‡ Recommended minimum dc supply voltage (V^+) is 5.5 V. Nominal load current flowing into terminal 5 is 1.5 mA at 7.5 V.



FM IF AMPLIFIER/ DISCRIMINATOR/AF AMPLIFIER — CA3014

Special-purpose amplifier used in if amplifier, AM and noise limiter, FM detector, and af preamplifier applications. 10-lead JEDEC MO-006-AF package; Outline No. 1. This type is identical with type CA3013 except for the following items:

MAXIMUM RATINGS

Positive DC Supply Voltage	V^+	+13	V

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = +7.5V)

Device Dissipation*	P_T	106 to 150	mW
Recovered AF Voltage (f = 4.5 MHz)	V_o(af)	135 min; 188 typ	mV

* The total current drain may be determined by dividing P_T by V^+.

CA3015 OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 12-lead JEDEC MO-006-AG package; Outline No. 2. The functional diagram for this type is identical to that of type CA3010.

MAXIMUM RATINGS

Positive DC Supply Voltage	V^+	+20	V
Negative DC Supply Voltage	V^-	−20	V
Input Signal Voltage (Single-ended)		+1, −8	V
Total Device Dissipation		600	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = 12V, V^- = −12V)

Static Characteristics			
Input Offset Voltage	V_{IO}	1.37 typ; 5 max	mV
Input Offset Current	I_{IO}	1.07 typ; 5 max	μA
Input Bias Current	I_I	9.6 typ; 24 max	μA
Input Offset Voltage Sensitivity:			
Positive	$\Delta V_{IO}/\Delta V_{CC}$	0.096 typ; 0.5 max	mV/V
Negative	$\Delta V_{IO}/\Delta V_{EE}$	0.156 typ; 0.5 max	mV/V
Device Dissipation:			
Terminal 5 not connected	P_T	175	mW
Terminal 5 shorted to terminal 9	P_T	500	mW
Dynamic Characteristics			
Open-Loop Differential Voltage Gain (f = 1 kHz)	A_{OL}	66 min; 70 typ	dB
Open-Loop —3-dB Bandwidth	BW_{OL}	200 min; 320 typ	kHz
Common-Mode Rejection Ratio (f = 1 kHz)	CMRR	80 min; 103 typ	dB
Maximum Output-Voltage Swing (f = 1 kHz)	V_O(P-P)	12 min; 14 typ	V
Input Impedance (f = 1 kHz)	Z_{in}	5 min; 7.8 typ	kΩ
Output Impedance (f = 1 kHz)	Z_{out}	92	Ω
Common-Mode Input-Voltage Range (f = 1 kHz)	V_{CMR}	+0.65, −8	V

CA3015A OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 12-lead JEDEC MO-006-AG package; Outline No. 2. The functional diagram for this type is identical to that of type CA3010.

MAXIMUM RATINGS

Signal Voltage	− 8 to 1	V
Device Dissipation	600	mW
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = 12V, V^- = −12V)

Static Characteristics			
Input Offset Voltage	V_{IO}	1 typ; 2 max	mV
Input Offset Current	I_{IO}	0.5 typ; 1.6 max	μA
Input Bias Current	I_I	4.7 typ; 6 max	μA
Input Offset Voltage Sensitivity:			
Positive	$\Delta V_{IO}/\Delta V_{CC}$	0.096 typ; 0.5 max	mV/V
Negative	$\Delta V_{IO}/\Delta V_{EE}$	0.156 typ; 0.5 max	mV/V
Device Dissipation	P_T	175	mW
Device Dissipation (Terminal 8 shorted to terminal 12)	P_T	500	mW
Dynamic Characteristics (f = 1 kHz except BW_{OL})			
Open-Loop Differential Voltage Gain	A_{OL}	66 min; 70 typ	dB
Open-Loop—3-dB Bandwidth	BW_{OL}	200 min; 320 typ	kHz
Slew Rate (R_S = 1 kΩ)	SR	7	V/μs
Common-Mode Rejection Ratio	CMRR	80 min; 103 typ	dB
Maximum Output-Voltage Swing	V_O(P-P)	14	V
Input Impedance	Z_{IN}	7.5 min; 10 typ	kΩ
Output Impedance	Z_{OUT}	85	Ω
Common-Mode Input-Voltage Range	V_{CMR}	0.65 to −8	V
Noise Figure (R_S = 1 kΩ):			
V^+ = 3V, V^- = − 3V	NF	6.3 typ; 9 max	dB
V^+ = 6V, V^- = − 6V	NF	8.3 typ; 12 max	dB
V^+ = 9V, V^- = − 9V	NF	10 typ; 14 max	dB
V^+ = 12V, V^- = −12V	NF	11 typ; 16 max	dB

OPERATIONAL AMPLIFIER — CA3016

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead ceramic-to-metal flat JEDEC MO-004-AF package; Outline No. 3. This type is electrically identical with type CA3015. The functional diagram for this type is identical to that of type CA3008.

OPERATIONAL AMPLIFIER — CA3016A

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applicatons. 14-lead ceramic-and-metal flat JEDEC MO-006-AF package; Outline No. 3. This type is electrically identical with type CA3015A. The functional diagram for this type is identical to that of type CA3008.

TRANSISTOR ARRAY — CA3018

General-purpose array with two isolated transistors and a Darlington-connected transistor pair used in low-power applications at frequencies from dc through the vhf range. 12-lead JEDEC MO-006-AG package; Outline No. 2.

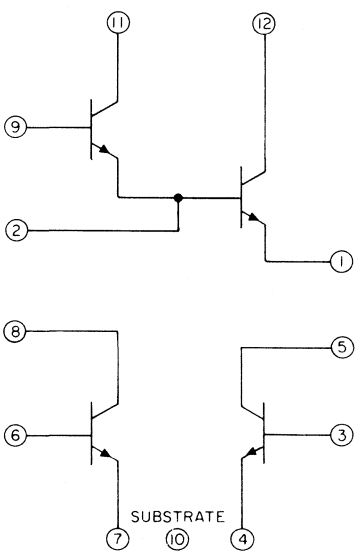
MAXIMUM RATINGS

Collector-to-Emitter Voltage	V_{CEO}	15	V
Collector-to-Base Voltage	V_{CBO}	20	V
Collector-to-Substrate Voltage	V_{CIO}	20	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	50	mA
Power Dissipation:			
Any one transistor	P_T	300	mW
Total package	P_T	450	mW
$T_A > 85°C$	P_T	Derate at 5	mW/°C
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Static Characteristics

Collector-to-Emitter Breakdown Voltage (I_C = 1mA, I_B = 0)	$V_{(BR)CEO}$	15 min; 24 typ	V
Collector-to-Base Breakdown Voltage (I_C = 10μA, I_E = 0)	$V_{(BR)CBO}$	20 min; 60 typ	V
Emitter-to-Base Breakdown Voltage (I_E = 10μA, I_C = 0)	$V_{(BR)EBO}$	5 min; 7 typ	V
Collector-to-Substrate Breakdown Voltage (I_C = 10μA, I_{C1} = 0)	$V_{(BR)CIO}$	20 min; 60 typ	V
Collector-to-Emitter Saturation Voltage (I_B = 1mA, I_C = 10mA)	V_{CES}	0.23	V
Collector-Cutoff Current (V_{CB} = 10V, I_E = 0)	I_{CBO}	0.002 typ; 100 max	nA
Collector-Cutoff Current (V_{CB} = 10V, I_B = 0)	I_{CEO}	5 max	μA
Static Forward-Current Transfer Ratio:			
V_{CE} = 3V, I_C = 10mA	h_{FE}	100	
V_{CE} = 3V, I_C = 1mA	h_{FE}	30 min; 100 typ	
V_{CE} = 3V, I_C = 10μA	h_{FE}	54	



CA3018
OR
CA3018A

Magnitude of Static-Beta Ratio, Isolated transistors Q_1 and Q_2 (V_{CE} = 3V, $I_{C1} = I_{C2}$ = 1mA)		0.9 min; 0.97 typ		
Static Forward-Current Transfer Ratio Darlington Pair, Q_3 and Q_4 (V_{CE} = 3V, I_C = 1mA)	h_{FED}	1500 min; 5400 typ		
Base-to-Emitter Voltage:				
V_{CE} = 3V, I_E = 1mA	V_{BE}		0.715	V
V_{CE} = 3V, I_E = 10mA	V_{BE}		0.800	V
Input Offset Voltage (V_{CE} = 3V, I_E = 1mA)	$\lvert V_{BE1}-V_{BE2}\rvert$	0.48 typ;	5 max	mV
Temperature Coefficient, Base-to-Emitter Voltage Q_1, Q_2 (V_{CE} = 3V, I_E = 1mA)	$\frac{\lvert\Delta V_{BE}\rvert}{\Delta T}$		1.9	mV/°C
Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair:				
V_{CE} = 3V, I_E = 10mA	$V_{BED(Q_{3-1})}$		1.46	V
V_{CE} = 3V, I_E = 1mA	$V_{BED(Q_{3-1})}$		1.32	V
Temperature Coefficient, Base-to-Emitter Voltage Darlington Pair Q_3, Q_4 (V_{CE} = 3V, I_E = 1mA)	$\frac{\lvert\Delta V_{BED}\rvert}{\Delta T}$		4.4	mV/°C
Temperature Coefficient, Magnitude of Input-Offset Voltage (V_{CC} = 6V, V_{EE} = −6V, $I_{C1} = I_{C2}$ = 1mA)	$\frac{\lvert V_{BE1}-V_{BE2}\rvert}{\Delta T}$		10	μV/°C
Dynamic Characteristics				
Low Frequency Noise Figure (V_{CE} = 3V, I_C = 100μA, source resistance = 1kΩ)	NF		3.25	dB
Low-Frequency Small-Signal Equivalent Circuit Characteristics (V_{CE} = 3V, I_C = 1mA, f = 1kHz):				
Forward Current-Transfer Ratio	h_{fe}		110	
Short-Circuit Input Impedance	h_{ie}		3.5	kΩ
Open-Circuit Output Impedance	h_{oe}		15.6	μmhos
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		1.8×10^{-4}	
Admittance Characteristics (V_{CE} = 3V, I_C = 1mA, f = 1MHz):				
Forward Transfer	Y_{fe}		31−j 1.5	mmhos
Input	Y_{ie}		0.3 + j 0.04	mmho
Output	Y_{oe}		0.001 + j 0.03	mmho
Gain-Bandwidth Product (V_{CE} = 3V, I_C = 3mA)	f_T	300 min; 500 typ		MHz
Emitter-to-Base Capacitance (V_{EB} = 3V, I_E = 0)	C_{EB}		0.6	pF
Collector-to-Base Capacitance (V_{CB} = 3V, I_C = 0)	C_{CI}		0.58	pF
Collector-to-Substrate Capacitance (V_{C1} = 3V, I_C = 0)	C_{CI}		2.8	pF

TRANSISTOR ARRAY

CA3018A

General-purpose array with two isolated transistors and a Darlington-connected transistor pair used in low-power applications at frequencies from dc through the vhf range. 12-lead JEDEC MO-006-AG package; Outline No. 2. This type is identical with type CA3018 except for the following items:

MAXIMUM RATINGS

Collector-to-Base Voltage	V_{CBO}	30	V
Collector-to-Substrate Voltage	V_{CIO}	40	V

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Static Characteristics

Collector-to-Base Breakdown Voltage ($I_C = 10\mu A$, $I_E = 0$)	$V_{(BR)CBO}$	30 min; 60 typ	V
Collector-to-Substrate Breakdown Voltage ($I_C = 10\mu A$, $I_{C_1} = 0$)	$V_{(BR)CIO}$	40 min; 60 typ	V
Collector-to-Emitter Saturation Voltage (I_B = 1mA, I_C = 10mA)	V_{CES}	0.23 typ; 0.5 max	V
Collector-Cutoff Current (V_{CB} = 10V, $I_E = 0$)	I_{CBO}	0.002 typ; 40 max	nA
Collector-Cutoff Current (V_{CE} = 10V, $I_B = 0$)	I_{CEO}	0.5 max	μA
Collector-Cutoff Current Darlington Pair (V_{CE} = 10V, $I_B = 0$)	I_{CEOD}	5 max	μA
Static Forward-Current Transfer Ratio			
V_{CE} = 3V, I_C = 10mA		50 min; 100 typ	
V_{CE} = 3V, I_C = 1mA		60 min; 100 typ	
V_{CE} = 3V, $I_C = 10\mu A$		30 min; 54 typ	
Static Forward-Current Transfer Ratio Darlington Pair, Q_3 and Q_4:			
V_{CE} = 3V, I_C = 1mA	h_{FED}	2000 min; 5400 typ	
V_{CE} = 3V, $I_C = 100\mu A$	h_{FED}	1000 min; 2800 typ	
Base-to-Emitter Voltage:			
V_{CE} = 3V, I_E = 1mA	V_{BE}	0.6 to 0.8	V
V_{CE} = 3V, I_E = 10mA	V_{BE}	0.8 typ; 0.9 max	V
Input Offset Voltage (V_{CE} = 3V, I_E = 1mA)	$\lvert V_{BE1} - V_{BE2} \rvert$	0.48 typ; 2 max	mV
Base (Q_3)-to-Emitter (Q_4) Voltage–Darlington Pair:			
V_{CE} = 3V, I_E = 10mA	$V_{BED}(V_{9-1})$	1.46 typ; 1.6 max	V
V_{CE} = 3V, I_E = 1mA	$V_{BED}(V_{9-1})$	1.1 to 1.5	V

CA3019 DIODE ARRAY

One diode "quad" and two isolated diodes on a common substrate used for modulator, mixer, balanced modulator, analog switch, and diode gate for chopper-modulator applications. 10-lead JEDEC MO-006-AF package; Outline No. 1.

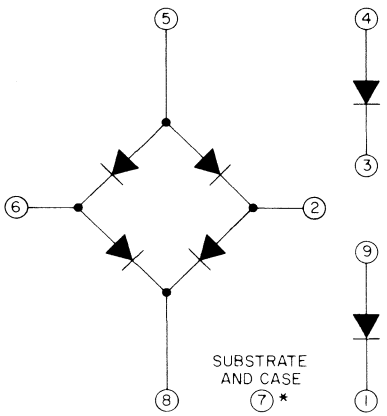
MAXIMUM RATINGS

Device Dissipation:		
Any one diode unit	20	mW
Total for device	120	mW
Diode Voltage Limits	−3 to +12	V
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

DC Forward Voltage Drop (I_F = 1 mA)	V_F	0.73 typ; 0.78 max	V
DC Reverse Breakdown Voltage ($I_R = -10\ \mu A$):			
Any diode	$V_{(BR)R}$	4 min; 6 typ	V
Any diode and substrate	$V_{(BR)R}$	25 min; 80 typ	V

DC Reverse Leakage Current (V_R = −4V):				
Any diode	I_R	0.0055 typ;	10 max	μA
Any diode and substrate	I_R	0.010 typ;	10 max	μA
Magnitude of Diode Offset (Difference in DC Forward Voltage Drops of any Two Units) (I_F = 1mA)	$\lvert V_{F1} - V_{F2} \rvert$	1 typ;	5 max	mV
Single Diode Capacitance (V_R = −2V, f = 1MHz)	C_D		1.8	pF
Diode Quad-to-Substrate Capacitance (V_R between terminals 2, 5, 6, or 8 of diode quad and terminal 7 (substrate) = −2V):				
Terminal 2 or 6 to terminal 7	C_{DQ-1}		4.4	pF
Terminal 5 or 8 to terminal 7	C_{DQ-1}		2.7	pF
Series Gate Switching Pedestal Voltage	V_S		10	mV



CA3019

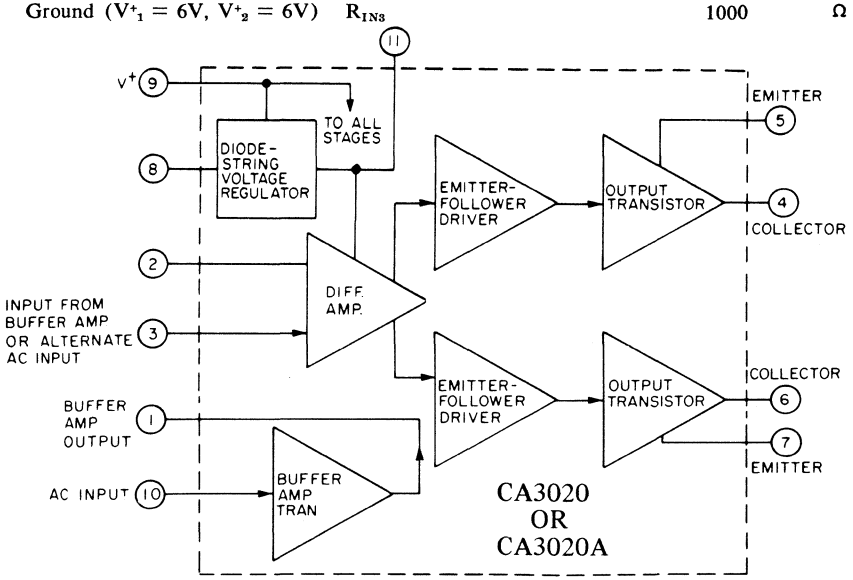
MULTIPURPOSE WIDE-BAND POWER AMPLIFIER CA3020

Multipurpose amplifier used in military, industrial, and commercial equipment at frequencies up to 8 MHz. 12-lead JEDEC MO-006-AG package; Outline No. 2.

MAXIMUM RATINGS	**Without Heat Sink**	**With Heat Sink**	
Device Dissipation:			
T_A = 25°C	1	2	W
T_A above 25°C	Derate linearly 6.7	—	mW/°C
T_A = 25 to 55°C	—	2	W
T_A = 55°C	—	Derate linearly 16.7	mW/°C
Temperature Range:			
Operating	−55 to 125		°C
Storage	−65 to 200		°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Collector-to-Emitter Breakdown Voltage (Q_6 and Q_7 at 10 mA)	$V_{(BR)CEO}$	18 min	V
Collector-to-Emitter Breakdown Voltage (Q_1 at 0.1 mA)	$V_{(BR)CEO}$	10 min	V
Idle Currents, Q_6 and Q_7 (V^+_1 = 9V, V^+_2 = 2V)	I_4 Idle, I_7 Idle	55	mA
Peak Output Currents, Q_6 and Q_7 (V^+_1 = 9V, V^+_2 = 2V)	I_4 Pk, I_7 Pk	140 min	mA
Cutoff Currents, Q_6 and Q_7 (V^+_1 = 9V, V^+_2 = 2V)	I_4 CUTOFF, I_7 CUTOFF	1 max	mA
Differential Amplifier Current Drain (V^+_1 = 9V, V^+_2 = 9)	I_{CC1}	6.3 to 12.5	mA
Total Current Drain (V^+_1 = 9V, V^+_2 = 9V)	$I_{CC1} + I_{CC2}$	8 to 35	mA
Differential Amplifier Input Terminal Voltages (V^+_1 = 9V, V^+_2 = 2V)	V_2, V_3	1.11	V
Regulator Terminal Voltage (V^+_1 = 9V, V^+_2 = 2V)	V_{11}	2.35	V
Q, Cutoff (Leakage) Currents: Collector-to-Emitter (V^+_1 = 10V)	I_{CEO}	100	μA
Emitter-to-Base (V^+_1 = 3V)	I_{EBO}	0.1	μA
Collector-to-Base (V^+_1 = 3V)	I_{CBO}	0.1	μA
Forward Current Transfer Ratio, Q_1 at 3 mA (V^+_1 = 6V)	h_{FE1}	30 min; 75 typ	
—3-dB Bandwidth (V^+_1 = 6V, V^+_2 = 6V)	BW	8	MHz
Maximum Power Output: V^+_1 = 6V, V^+_2 = 6V	$P_{O(MAX)}$	200 min; 300* typ	mW
V^+_1 = 9V, V^+_2 = 9V	$P_{O(MAX)}$	400 min; 550* typ	mW
Sensitivity for P_{OUT} = 400 mW (V^+_1 = 9V, V^+_2 = 9V)‡	e_{IN}	35* typ; 55 max	mV
Input Resistance, Terminal 3 to Ground (V^+_1 = 6V, V^+_2 = 6V)	R_{IN3}	1000	Ω



Junction-to-Case Thermal Resistance	θ_{J-C}	60 max	°C/W

* R_{CC} = 130 Ω
‡ This characteristics does not apply to type CA3020A.

MULTIPURPOSE WIDE-BAND POWER AMPLIFIER — CA3020A

Multipurpose amplifier used in military, industrial, and commercial equipment at frequencies up to 8 MHz. 12-lead JEDEC MO-006-AG package; Outline No. 2. This type is identical with type CA3020 except for the following items:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Collector-to-Emitter Breakdown Voltage (Q_6 and Q_7 at 10 mA)	$V_{(BR)CEO}$	25 min	V
Peak Output Currents, Q_6 and Q_7 (V^+_1 = 9V, V^+_2 = 2V)	I_4 Pk, I_7 Pk	180 min	mA
Total Current Drain (V^+_1 = 9V, V^+_2 = 9V)	$I_{CC1}+I_{CC2}$	14 to 30	mA
Maximum Power Output:			
V^+_1 = 6V, V^+_2 = 6V	$P_{O(MAX)}$	200 min; 300* typ	mW
V^+_1 = 9V, V^+_2 = 9V	$P_{O(MAX)}$	400 min; 550* typ	mW
V^+_1 = 9V, V^+_2 = 12V	$P_{O(MAX)}$	800 min; 1000‡ typ	mW
Sensitivity for P_{OUT} = 800 mW	e_{IN}	50‡ typ; 100 max	mV

* R_{CC} = 130 Ω
‡ R_{CC} = 200 Ω

VIDEO AND WIDE-BAND AMPLIFIER — CA3021

Multi-purpose amplifier used in gain-controlled linear amplifier, AM/FM if amplifier, video amplifier, and limiter applications. 12-lead JEDEC MO-006-AG package; Outline No. 2.

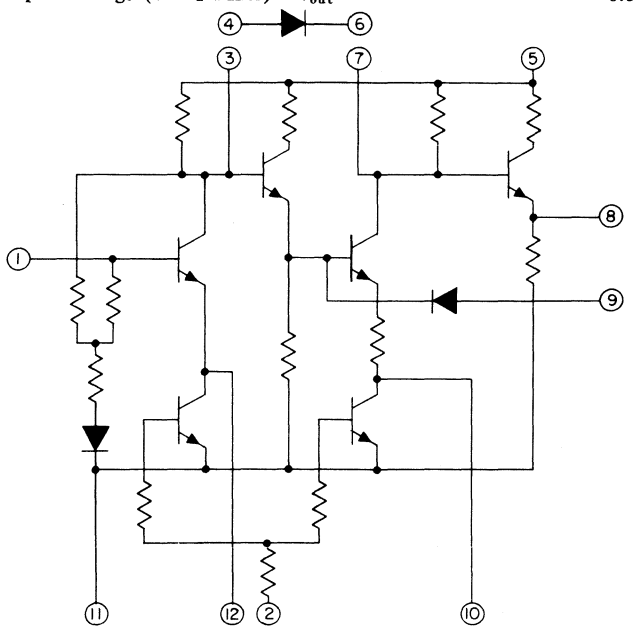
MAXIMUM RATINGS

Positive DC Supply Voltage	V^+	+18	V
Negative DC Supply Voltage	V^-	−6	V
Input Signal Voltage (Single-ended)		±3	V
Total Device Dissipation		120	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = +6V

Device Dissipation	P_T	1 to 8	mW
Quiescent Output Voltage	V_O	2.2	V
AGC Source Current (V_{AGC} = 6V)	I_{AGC}	0.8	mA
Voltage Gain:			
f = 0.5 MHz	A	50 min; 56 typ	dB
f = 0.8 MHz	A	40 min; 46 typ	dB
—3-dB Bandwidth	BW	0.8 min; 2.4 typ	MHz

Input Resistance (f = 1 MHz)	R_{in}	4	kΩ
Input Capacitance (f = 1 MHz)	C_{in}	11	pF
Output Resistance (f = 1 MHz)	R_{out}	300	Ω
Noise Figure (f = 1 MHz)	NF	4.2 typ; 8.5 max	dB
AGC Range (f = 1 MHz)	AGC	33	dB
Maximum Output Voltage (f = 1 MHz)	v_{out}	0.6	V_{rms}



CA3021
CA3022
OR
CA3023

CA3022

VIDEO AND WIDE-BAND AMPLIFIER

Multi-purpose amplifier used in gain-controlled linear amplifier, AM/FM if amplifier, video amplifier, and limiter applications. 12-lead JEDEC MO-006-AG package; Outline No. 2. For maximum ratings, refer to type CA3021.

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, $V^+ = +6V$

Device Dissipation	P_T	5 to 24	mW
Quiescent Output Voltage	V_O	1.9	V
AGC Source Current ($V_{AGC} = 6V$)	I_{AGC}	0.8	mA
Voltage Gain:			
f = 2.5 MHz	A	50 min; 57 typ	dB
f = 3 MHz	A	40 min; 44 typ	dB
—3-dB Bandwidth	BW	3 min; 7.5 typ	MHz
Input Resistance (f = 5 MHz)	R_{in}	1300	Ω
Input Capacitance (f = 5 MHz)	C_{in}	18	pF
Output Resistance (f = 5 MHz)	R_{out}	120	Ω
Noise Figure (f = 1 MHz)	NF	4.4 typ; 8.5 max	dB
AGC Range (f = 5 MHz)	AGC	33	dB
Maximum Output Voltage (f = 5 MHz)	v_{out}	0.7	V_{rms}

VIDEO AND WIDE-BAND AMPLIFIER — CA3023

Multi-purpose amplifier used in gain-controlled linear amplifier, AM/FM if amplifier, video amplifier, and limiter applications. 12-lead JEDEC MO-006-AG package; Outline No. 2. For maximum ratings, refer to type CA3021.

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, $V^+ = +6V$)

Device Dissipation	P_T	24 to 48	mW
Quiescent Output Voltage	V_O	1.3	V
AGC Source Current ($V_{AGC} = 6V$)	I_{AGC}	0.8	mA
Voltage Gain:			
f = 5 MHz	A	50 min; 53 typ	dB
f = 10 MHz	A	40 min; 44 typ	dB
—3-dB Bandwidth	BW	10 min; 16 typ	MHz
Input Resistance (f = 10 MHz)	R_{in}	300	Ω
Input Capacitance (f = 10 MHz)	C_{in}	13	pF
Output Resistance (f = 10 MHz)	R_{out}	100	Ω
Noise Figure (f = 1 MHz)	NF	6.5 typ; 8.5 max	dB
AGC Range (f = 10 MHz)	AGC	33	dB
Maximum Output Voltage (f = 10 MHz)	v_{out}	0.5	V_{rms}

INDEPENDENT DIFFERENTIAL AMPLIFIER — CA3026

General-purpose array consisting of two independent differential amplifiers with associated constant-current transistors used in low-power applications at frequencies from dc to 120 MHz. 12-lead JEDEC MO-006-AG package; Outline No. 2.

MAXIMUM RATINGS

Each Transistor:			
Collector-to-Emitter Voltage	V_{CEO}	15	V
Collector-to-Base Voltage	V_{CBO}	20	V
Collector-to-Substrate Voltage	V_{CIO}	20	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	50	mA
Power Dissipation:			
Any one transistor		300	mW
Total package		600	mW
$T_A > 55°C$		Derate at 5	mW/°C
Ambient Temperature:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Static Characteristics

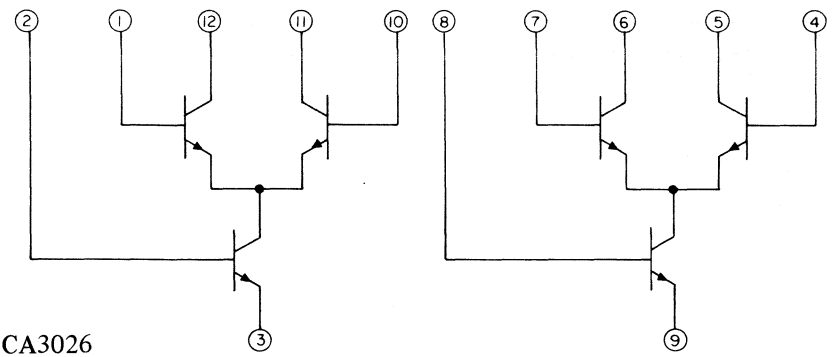
Each Differential Amplifier ($V_{CB} = 3V$, $I_{E(Q3)} = I_{E(Q4)} = 2mA$):			
Input Offset Voltage	V_{IO}	0.45 typ; 5 max	mV

Input Offset Current	I_{IO}	0.3 typ; 2 max	μA
Input Bias Current	I_I	10 typ; 24 max	μA
Quiescent Operating Current Ratio	$\frac{I_{C(Q1)}}{I_{C(Q2)}}$ or $\frac{I_{C(Q5)}}{I_{C(Q6)}}$	0.98 to 1.02	
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\Delta\lvert V_{IO}\rvert}{\Delta t}$	1.1	μV/°C
Each Transistor:			
Collector-to-Emitter Breakdown Voltage (I_C = 1mA, I_B = 0)	$V_{(BR)CEO}$	15 min; 24 typ	V
Collector-to-Base Breakdown Voltage (I_C = 10μA, I_E = 0)	$V_{(BR)CBO}$	20 min; 60 typ	V
Collector-to-Substrate Breakdown Voltage (I_C = 10μA, I_{C1} = 0)	$V_{(BR)CIO}$	20 min; 60 typ	V
Emitter-to-Base Breakdown Voltage (I_E = 10μA, I_C = 0)	$V_{(BR)EBO}$	5 min; 7 typ	V
Collector-Cutoff Current (V_{CB} = 10V, I_E = 0)	I_{CBO}	0.002 typ; 100 max	nA
DC Forward Base-to-Emitter Voltage:			
V_{CB} = 3V, I_C = 50μA	V_{BE}	0.63 typ; 0.7 max	V
V_{CB} = 3V, I_C = 1mA	V_{BE}	0.715 typ; 0.8 max	V
V_{CB} = 3V, I_C = 3mA	V_{BE}	0.75 typ; 0.85 max	V
V_{CB} = 3V, I_C = 10mA	V_{BE}	0.8 typ; 0.9 max	V
Temperature Coefficient of Base-to-Emitter Voltage (V_{CB} = 3V, I_C = 1mA)	$\frac{\Delta V_{BE}}{\Delta T}$	−1.9	mV/°C

Dynamic Characteristics

Common-Mode Rejection Ratio for Each Amplifier (V^+ = 12V, V^- = −6V, V_X = −3.3V, f = 1kHz)	CMRR	100	dB
AGC Range, One Stage (V^+ = 12V, V^- = −6V, V_X = −3.3V, f = 1kHz)	AGC	75	dB
Voltage Gain, Single Stage Double-Ended Output (V^+ = 12V, V^- = −6V, V_X = −3.3V, f = 1kHz)	A	32	dB
AGC Range, Two Stage (V^+ = 12V, V^- = −6V, V_X = −3.3V, f = 1kHz)	AGC	105	dB
Voltage Gain, Two Stage Double-Ended Output (V^+ = 12V, V^- = −6V, V_X = −3.3V, f = 1kHz)	A	60	dB
Low-Frequency Small-Signal Equivalent-Circuit Characteristics For Single Transistor (V_{CE} = 3V, I_C = 1mA, f = 1kHz):			
Forward Current-Transfer Ratio	h_{fe}	110	
Short-Circuit Input Impedance	h_{ie}	3.5	kΩ
Open-Circuit Output Impedance	h_{oe}	15.6	μmhos
Open-Circuit Reverse Voltage Transfer Ratio	h_{re}	1.8×10^{-4}	
1/f Noise Figure, Single Transistor (V_{CE} = 3V, f = 1kHz)	NF	3.25	dB
Gain-Bandwidth Product, Single Transistor (V_{CE} = 3V, I_C = 3mA)	f_T	550	MHz
Admittance Characteristics, Differential Circuit Configuration, Each Amplifier (V_{CB} = 3V each collector, $I_C \approx$ 1.25mA, f = 1MHz):			
Forward Transfer Admittance	y_{21}	−20 + j 0	mmhos
Input Admittance	y_{11}	0.22 + j 0.1	mmho
Output Admittance	y_{22}	0.01 + j 0	mmho
Reverse Transfer Admittance	y_{12}	−0.003 + j 0	mmho

Admittance Characteristics, Cascode Circuit Configuration, Each Amplifier (V_{CB} = 3V total stage, $I_C \approx$ 2.5mA, f = 1MHz):			
Forward Transfer Admittance	y_{21}	68 − j 0	mmhos
Input Admittance	y_{11}	0.55 + j 0	mmho
Output Admittance	y_{22}	0 + j 0.02	mmho
Reverse Transfer Admittance	y_{12}	0.004 − j 0.005	μmho
Noise Figure (f = 100 MHz)	NF	8	dB



CA3026

DIFFERENTIAL/ CASCODE AMPLIFIER

CA3028A

General-purpose amplifier used in communications and industrial equipment at frequencies from dc to 120 MHz. 8-lead JEDEC MO-002-AL package; Outline No. 4.

MAXIMUM RATINGS

Device Dissipation:		
T_A at 25°C	450	mW
T_A at 25 to 85°C	450	mW
T_A above 85°C	Derate linearly 5	mW/°C
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

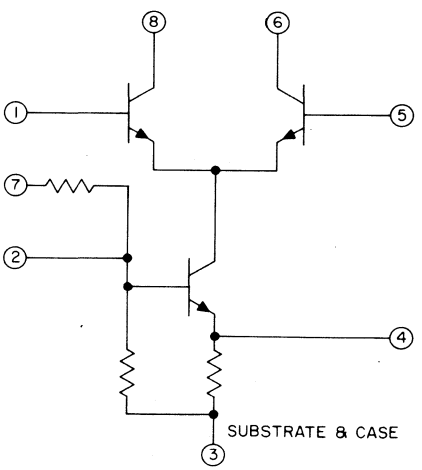
Static Characteristics

Input Bias Current:			
V^+ = 6V, V^- = − 6V	I_I	16.6 typ; 70 max	μA
V^+ = 12V, V^- = −12V	I_I	36 typ; 106 max	μA
Quiescent Operating Current			
V^+ = 6V, V^- = − 6V	I_6 or I_8	0.8 to 2	mA
V^+ = 12V, V^- = −12V	I_6 or I_8	2 to 5	mA
AGC Bias Current, Into Constant-Current Source Terminal No. 7:			
V^+ = 12V, V_{AGC} = 9V	I_7	1.28	mA
V^+ = 12V, V_{AGC} = 12V	I_7	1.65	mA

Input Current, Terminal No. 7*:			
$V^+ = 6V, V^- = -6V$	I_7	0.5 to 1	mA
$V^+ = 12V, V^- = -12V$	I_7	1 to 2.1	mA
Device Dissipation:			
$V^+ = 6V, V^- = -6V$	P_T	24 to 54	mW
$V^+ = 12V, V^- = -12V$	P_T	120 to 260	mW

Dynamic Characteristics		**Differential Amplifier**	**Cascode Amplifier**	
Power Gain:				
$V^+ = 9V$, f = 100 MHz*	G_P	14 min; 17 typ	16 min; 20 typ	dB
$V^+ = 9V$, f = 10.7 MHz	G_P	28 min; 32 typ	35 min; 39 typ	dB
Noise Figure* ($V^+ = 9V$, f = 100 MHz)	NF	6.7 typ; 9 max	7.2 typ; 9 max	dB
Input Admittance ($V^+ = 9V$, f = 10.7 MHz)	Y_{11}	$0.5 + j\,0.5$	$0.6 + j\,1.6$	mmhos
Reverse Transfer Admittance ($V^+ = 9V$, f = 10.7 MHz)	Y_{12}	$0.01 - j\,0.0002$	$0.0003 - j\,0$	mmhos
Forward Transfer Admittance ($V^+ = 9V$, f = 10.7 MHz)	Y_{21}	$-37 + j\,0.5$	$99 - j\,18$	mmhos
Output Admittance ($V^+ = 9V$, f = 10.7 MHz)	Y_{22}	$0.04 + j\,0.23$	$0 + j\,0.08$	mmho
Power Output, Untuned* ($V^+ = 9V$, f = 10.7 MHz)	P_o	5.7	—	μW
AGC Range, Maximum Power Gain to Full Cutoff* ($V^+ = 9V$, f = 10.7 MHz)	AGC	62	—	dB
Voltage Gain ($V^+ = 0V$, $R_L = 1\ k\Omega$, f = 10.7 MHz)	A	30	40	dB
Peak-to-Peak Output Current:				
$V^+ = 9V$, $e_{in} = 400$ mV, f = 10.7 MHz	I_{P-P}	2 to 7	—	mA
$V^+ = 12V$, $e_{in} = 400$ mV, f = 10.7 MHz	I_{P-P}	3.5 to 10	—	mA

* This characteristic does not apply to type CA3053.



CA3028A
OR
CA3028B

DIFFERENTIAL/ CASCODE AMPLIFIER — CA3028B

General-purpose amplifier used in communications and industrial equipment at frequencies from dc to 120 MHz. 8-lead JEDEC MO-002-AL package; Outline No. 4. This type is identical with type CA3028A except for the following items:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Static Characteristics			
Input Offset Voltage:			
$V^+ = 6V, V^- = -6V$	V_{IO}	0.98 typ; 5 max	mV
$V^+ = 12V, V^- = 12V$	V_{IO}	0.89 typ; 5 max	mV
Input Offset Current:			
$V^+ = 6V, V^- = -6V$	I_{IO}	0.56 typ; 5 max	μA
$V^+ = 12V, V^- = -12V$	I_{IO}	1.06 typ; 6 max	μA
Input Bias Current:			
$V^+ = 6V, V^- = -6V$	I_I	16.6 typ; 40 max	μA
$V^+ = 12V, V^- = -12V$	I_I	36 typ; 80 max	μA
Quiescent Operating Current:			
$V^+ = 6V, V^- = -6V$	I_6 or I_8	1 to 1.5	mA
$V^+ = 12V, V^- = -12V$	I_6 or I_8	2.5 to 4	mA
Device Dissipation:			
$V^+ = 6V, V^- = -6V$	P_T	24 to 42	mW
$V^+ = 12V, V^- = -12V$	P_T	120 to 220	mW
Dynamic Characteristics			
Voltage Gain, Differential at f = 1 kHz:			
$V^+ = 6V, V^- = -6V, R_L = 2 k\Omega$	P_o	35 to 42	dB
$V^+ = 12V, V^- = 12V, R_L = 1.6$	P_o	40 to 45	dB
Maximum Peak-to-Peak Output Voltage at f = 1 kHz:			
$V^+ = 6V, V^- = -6V, R_L = 2 k\Omega$	V_o(P-P)	7 min; 11.5 typ	V
$V^+ = 12V, V^- = -12V, R_L = 1.6 k\Omega$	V_o(P-P)	15 min; 23 typ	V
—3-dB Bandwidth:			
$V^+ = 6V, V^- = -6V, R_L = 2 k\Omega$	BW	7.3	MHz
$V^+ = 12V, V^- = -12V, R_L = 1.6 k\Omega$	BW	8	MHz
Common-Mode Input-Voltage Range:			
$V^+ = 6V, V^- = -6V$	V_{CMR}	−2.5 to 4	V
$V^+ = 12V, V^- = -12V$	V_{CMR}	−5 to 7	V
Common-Mode Rejection Ratio:			
$V^+ = 6V, V^- = -6V$	CMRR	60 min; 110 typ	dB
$V^+ = 12V, V^- = -12V$	CMRR	60 min; 90 typ	dB
Input Impedance at f = 1 kHz:			
$V^+ = 6V, V^- = -6V$	Z_{IN}	5.5	kΩ
$V^+ = 12V, V^- = -12V$	Z_{IN}	3	kΩ
Peak-to-Peak Output Current, Differential Amplifier:			
$V^+ = 9V, e_{in} = 400$ mV, f = 10.7 MHz	I_{P-P}	2.5 to 6	mA
$V^+ = 12V, e_{in} = 400$ mV, f = 10.7 MHz	I_{P-P}	4.5 to 8	mA

OPERATIONAL AMPLIFIER — CA3029

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, servo driver, scaling adder, and balanced modulator-driver appli-

cations. 14-lead JEDEC MO-001-AB package; Outline No. 6. This type is identical with type CA3008 except for the followings items:

MAXIMUM RATINGS

Temperature Range:		
Operating	0 to 70	°C
Storage	−25 to 85	°C

CA3029A OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead JEDEC MO-001-AB package; Outline No. 6. This type is identical with type CA3008A except for the following items:

MAXIMUM RATINGS

Temperature Range:		
Operating	0 to 70	°C
Storage	−25 to 85	°C

CA3030 OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, servo driver, scaling adder, and balanced modulator-driver applications. 14-lead JEDEC MO-001-AB package; Outline No. 6. This type is identical with type CA3015 except for the following items:

MAXIMUM RATINGS

Temperature Range:		
Operating	0 to 70	°C
Storage	−25 to 85	°C

CA3030A OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead JEDEC MO-001-AB package; Outline No. 6. This type is identical with type CA3015A except for the following items:

MAXIMUM RATINGS

Temperature Range:		
Operating	0 to 70	°C
Storage	−25 to 85	°C

OPERATIONAL AMPLIFIER CA3033

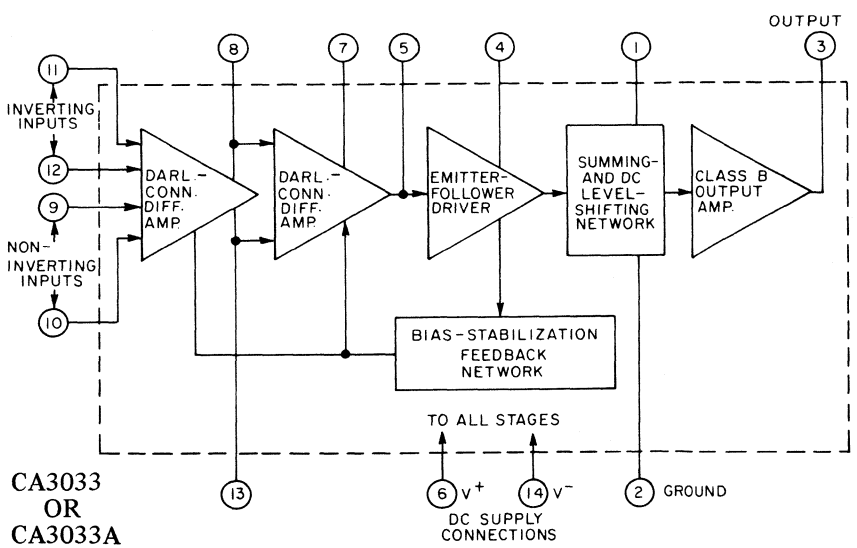
General-purpose amplifier used for critical applications requiring substantial output current. 14-lead JEDEC MO-001-AD package; Outline No. 7.

MAXIMUM RATINGS

Input Signal Voltage	±10	V
Device Dissipation:		
T_A up to 25°C	1.2	W
T_A above 25°C	Derate at 8	mW/°C
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = 12V, V^- = −12V)

Static Characteristics			
Input Offset Voltage	V_{IO}	2.6 typ; 5 max	mV
Input Offset Current	I_{IO}	5 typ; 35 max	nA
Input Bias Current	I_I	83 typ; 350 max	nA
Input Offset Voltage Drift (−55 to 125°C)	$V_{IO}/\Delta T$	6.6	μV/°C
Input Offset Current Drift:			
−55 to 25°C	$I_{IO}/\Delta T$	1	nA/°C
25 to 125°C	$I_{IO}/\Delta T$	0.08	nA/°C
Input Offset Voltage Sensitivity:			
Positive	$\Delta V_{IO}/\Delta V_{CC}$	0.3 typ; 0.5 max	mV/V
Negative	$\Delta V_{IO}/\Delta V_{EE}$	0.3 typ; 0.5 max	mV/V
Device Dissipation	P_T	60 to 180	mW
Dynamic Characteristics			
Open-Loop Differential Voltage Gain (f = 1 kHz)	A_{OL}	84 min; 90 typ	dB
60-dB-Amplifier Bandwidth (C_X, C_Y = 0.001 μF)	BW	230	kHz



Common-Mode Rejection Ratio (f = 1 kHz)	CMRR	84 min; 100 typ	dB
Common-Mode Input Voltage Range (f = 1 kHz)	V_{CMR}	−7.5 to 3.5	V
Maximum Output-Voltage Swing (R_L = 500 Ω, f = 1 kHz)	V_O(P-P)	18 min; 22 typ	V
Input Impedance (f = 1 kHz)	Z_{in}	0.15 min; 1.5 typ	MΩ
Output Current (R_L = 500 Ω, f = 1 kHz)	I_o(P-P)	36 min; 44 typ	mA
Slew Rate (f = 1 kHz)	SR	1.2	V/μs
Power Output (THD = 10%, R_L = 500 Ω, C_X, C_Y = 0.001 μF, f = 1 kHz)	P_o	80 min; 122 typ	mW

CA3033A OPERATIONAL AMPLIFIER

General-purpose amplifier used for critical applications requiring substantial output current. 14-lead JEDEC MO-001-AD package; Outline No. 7.

MAXIMUM RATINGS

Input Signal Voltage	−13, 10	V
Device Dissipation:		
T_A up to 25°C	1.2	W
T_A above 25°C	Derate at 8	mW/°C
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = 18V, V^- = −18V)

Static Characteristics			
Input Offset Voltage	V_{IO}	2.9 typ; 5 max	mV
Input Offset Current	I_{IO}	9 typ; 25 max	nA
Input Bias Current	I_I	103 typ; 200 max	nA
Input Offset Voltage Drift (−55 to 125°C)	$V_{IO}/\Delta T$	6.6	μV/°C
Input Offset Current Drift:			
−55 to 25°C	$I_{IO}/\Delta T$	1	nA/°C
25 to 125°C	$I_{IO}/\Delta T$	0.08	nA/°C
Input Offset Voltage Sensitivity:			
Positive	$\Delta V_{IO}/\Delta V_{CC}$	0.2 typ; 0.5 max	mV/V
Negative	$\Delta V_{IO}/\Delta V_{EE}$	0.2 typ; 0.5 max	mV/V
Device Dissipation	P_T	150 to 420	mW
Dynamic Characteristics			
Open-Loop Differential Voltage Gain (f = 1 kHz)	A_{OL}	90 min; 96 typ	dB
60-dB-Amplifier Bandwidth (C_X, C_Y = 0.001 μF)	BW	360	kHz
Common-Mode Rejection Ratio (f = 1 kHz)	CMRR	96 min; 108 typ	dB
Common-Mode Input Voltage Range (f = 1 kHz)	V_{CMR}	−12 to 6	V
Maximum Output-Voltage Swing (R_L = 500 Ω, f = 1 kHz)	V_O(P-P)	30 min; 32 typ	V
Input Impedance (f = 1 kHz)	Z_{in}	0.4 min; 1 typ	MΩ
Output Current (R_L = 500 Ω, f = 1 kHz)	I_o(P-P)	60 min; 64 typ	mA
Slew Rate (f = 1 kHz)	SR	2.5	V/μs
Power Output (THD = 10%, R_L = 500 Ω, C_X, C_Y = 0.001 μF, f = 1 kHz)	P_o	220 min; 255 typ	mW

HIGH FREQUENCY WIDE-BAND AMPLIFIER/ PHASE DETECTOR

CA3034

Special-purpose amplifier used in differential input amplifier, dual phase detector with differential output amplifier, and afc applicatons. 10-lead JEDEC MO-006-AF package; Outline No. 1.

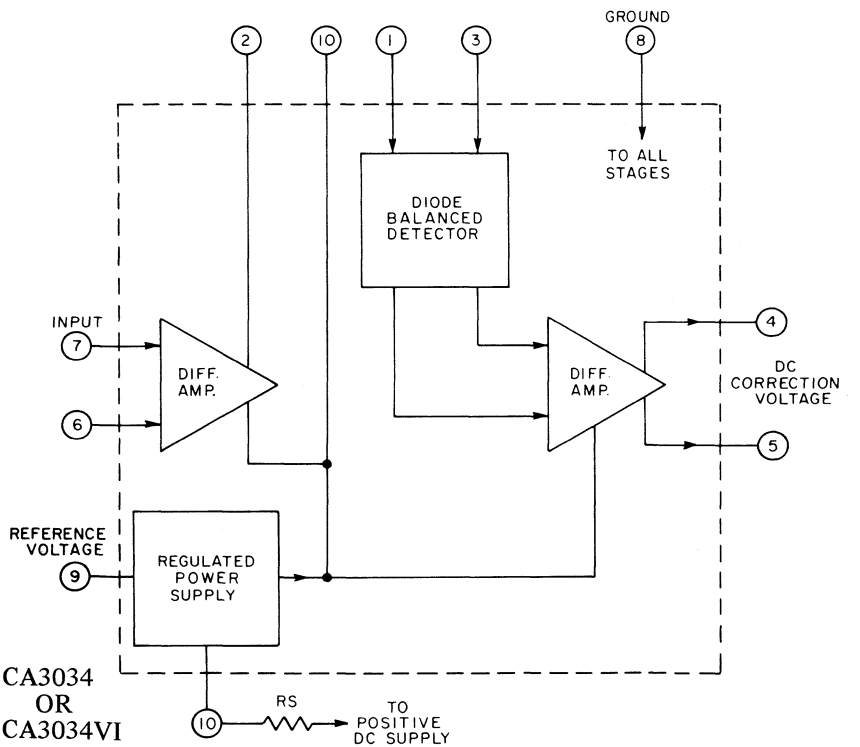
MAXIMUM RATINGS

Input Signal Voltage (Single-ended)	12	V
Supply Voltage	15	V
Total Device Dissipation	300	mW
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = 10V)

Static Characteristics

Total Current Drain	I_d	6.5 to 13	mA
Quiescent Operating Current into Terminal 2	I_2	1.3 to 2.6	mA
Reference Voltage at Terminal 9	V_9	5.3 to 5.7	V



Quiescent Operating Voltage at Terminal 4	V_4	4.5 to 6.5	V
Quiescent Operating Voltage at Terminal 5	V_5	4.5 to 6.5	V
Output Offset Voltage between Terminals 4 and 5	V_{4-5}	0 typ; 1.5 max	V
Dynamic Characteristics			
Input Impedance (Terminal 7)	Z_{in}	2	kΩ
Correction-Control Voltage at Terminal 4 (V_{in} = 100 mV RMS, f_0 in MHz):			
45.750 − 0.025	$V_{corr}(4)$	9 min	V
45.750 + 0.025	$V_{corr}(4)$	1.5 max	V
45.750 − 0.500	$V_{corr}(4)$	9.6 min	V
45.750 + 0.500	$V_{corr}(4)$	1.5 max	V
45.750 − 1.15	$V_{corr}(4)$	8 min	V
45.750 + 1.15	$V_{corr}(4)$	3 max	V
45.750 − 1.55	$V_{corr}(4)$	8 max	V
45.750 + 1.55	$V_{corr}(4)$	3 min	V
Correction-Control Voltage at Terminal 5 (V_{in} = 100 mV RMS, f_0 in MHz):			
45.750 − 0.025	$V_{corr}(5)$	1.5 max	V
45.750 + 0.025	$V_{corr}(5)$	9 min	V
45.750 − 0.500	$V_{corr}(5)$	1.5 max	V
45.750 + 0.500	$V_{corr}(5)$	9.6 min	V
45.750 − 1.15	$V_{corr}(5)$	3 max	V
45.750 + 1.15	$V_{corr}(5)$	8 min	V
45.750 − 1.55	$V_{corr}(5)$	3 min	V
45.750 + 1.55	$V_{corr}(5)$	8 max	V

CA3034V1 — HIGH FREQUENCY WIDE-BAND AMPLIFIER/ PHASE DETECTOR

Special-purpose amplifier used in differential input amplifier, dual phase detector with differential output amplifier, and afc applications. 10-formed-lead "TO-5" package; Outline No. 5. This type is electrically identical with type CA3034.

CA3035 — ULTRA-HIGH-GAIN WIDE-BAND AMPLIFIER ARRAY

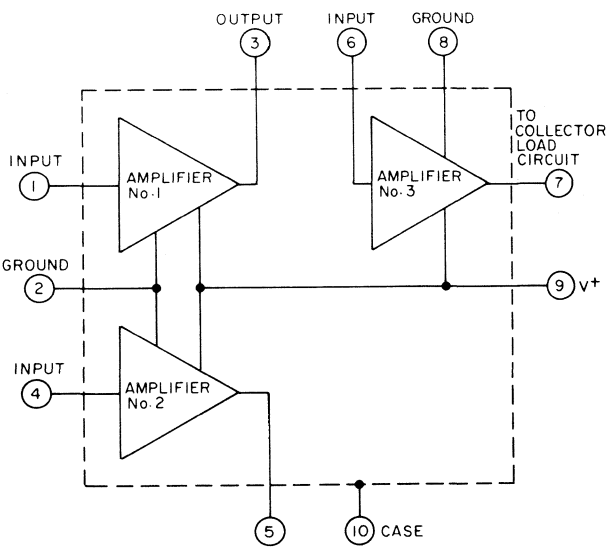
General-purpose amplifier with three individual amplifiers used in remote-control amplifier applications, such as TV receivers. 10-lead JEDEC MO-006-AF package; Outline No. 1.

MAXIMUM RATINGS

Input Signal Voltage (Single-ended)	1	V
Supply Voltage	15	V
Total Device Dissipation	300	mW
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Static Characteristics			
Quiescent Operating Voltage ($V^+ = 9V$)	V_3	2	V
Quiescent Operating Voltage ($V^+ = 9V$)	V_5	1.9	V
Quiescent Operating Voltage ($V^+ = 9V$)	V_7	4.9	V
Total Current Drain ($V^+ = 9V$, $R_{L3} = 5\ k\Omega$)	I_d	5	mA
Dynamic Characteristics			
Voltage Gain ($V^+ = 9V$, f = 40 kHz):			
Amplifier 1	A_1	44	dB
Amplifier 2	A_2	46	dB
Amplifier 3	A_3	42	dB
Cascade		132	dB
Output Voltage Swing:			
Amplifier 1, $V^+ = 9V$, $R_{L1} = 10\ k\Omega$	V_1out	2	V
Amplifier 2, $V^+ = 9V$, $R_{L2} = 10\ k\Omega$	V_2out	2.6	V
Amplifier 3, $V^+ = 9V$, $R_{L3} = 5\ k\Omega$	V_3out	8	V
Input Resistance (f = 40 kHz):			
Amplifier 1	R_1in	50	kΩ
Amplifier 2	R_2in	2	kΩ
Amplifier 3	R_3in	670	Ω
Output Resistance (f = 40 kHz):			
Amplifier 1	R_1out	270	Ω
Amplifier 2	R_2out	170	Ω
Amplifier 3	R_3out	100	kΩ
—3-dB Bandwidth ($V^+ = 9V$):			
Amplifier 1	BW_1	500	kHz
Amplifier 2	BW_2	2.5	MHz
Amplifier 3	BW_3	2.5	MHz
Noise Figure (Amplifier 1) ($R_S = 1\ k\Omega$, f = 1 kHz)	NF_1	6 typ; 7 max	dB
Sensitivity ($V^+ = +13V$, Relay Current = 7.5 mA)		100 typ; 150 max	μV



CA3035 OR CA3035VI

CA3035V1 ULTRA-HIGH-GAIN WIDE-BAND AMPLIFIER ARRAY

General-purpose amplifier with three individual amplifiers used in remote-control amplifier applications, such as TV receivers. 10-formed-lead "TO-5" package; Outline No. 5. This type is electrically identical with type CA3035.

CA3036 DUAL DARLINGTON ARRAY

General-purpose amplifier with two independent low-noise wide-band amplifier channels used in stereo phonograph preamplifier, low-level stereo and single-channel amplifier stages, low-noise emitter-follower differential amplifier, and operational-amplifier driver applications. 10-lead JEDEC MO-006-AF package; Outline No. 1.

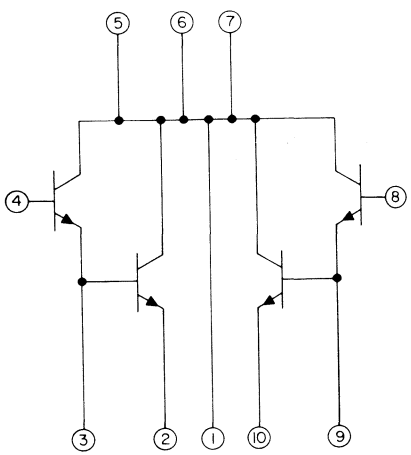
MAXIMUM RATINGS

Device Dissipation (Any one transistor or total for device)	300	mW
For Each Transistor In The Array:		
Collector-to-Emitter Voltage	15	V
Collector-to-Base Voltage	30	V
Emitter-to-Base Voltage	5	V
Collector Current	50	mA
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

For Each Transistor (Q_1, Q_2, Q_3, Q_4):			
Collector-to-Emitter Breakdown Voltage (I_C = 1 mA, I_B = 0)	$V_{(BR)CEO}$	15 min; 20 typ	V
Collector-to-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	$V_{(BR)CBO}$	30 min; 44 typ	V
Emitter-to-Base Breakdown Voltage (I_E = 10 μA, I_C = 0)	$V_{(BR)EBO}$	5 min; 6 typ	V
Collector-Cutoff Current:			
V_{CB} = 5 V, I_E = 0	I_{CBO}	0.5 max	μA
V_{CE} = 15V, I_B = 0	I_{CEO}	5 max	μA
For Either Input Transistor (Q_1 or Q_3):			
Static Forward Current-Transfer Ratio (I_{C1} or I_{C3} = 1 mA)	h_{FE}	30 min; 82 typ	
Forward Transfer Admittance (I_{C1} or I_{C3} = 2 mA, f = 50 MHz)	y_{fe}	0.68 + j 7.9	mmhos
Input Admittance (Output Short-Circuited) (I_{C1} or I_{C3} = 2 mA, f = 50 MHz)	y_{ie}	4.14 + j 5.95	mmhos
Output Admittance, Input Short-Circuited) (I_{C1} or I_{C3} = 2 mA, f = 50 MHz)	y_{oe}	1.94 + j 2.64	mmhos
Reverse Transfer Admittance (Input Short-Circuited) (I_{C1} or I_{C3} = 2 mA, f = 50 MHz)	y_{re}	Negligible	mmhos

For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4):			
Emitter-to-Base Breakdown Voltage (I_{E2} or I_{E4} = 10 μA)	$V_{(BR)EBO(D)}$	10 min; 12.6 typ	V
Static Forward Current-Transfer Ratio (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 1 mA)	$h_{FE(D)}$	1000 min; 4540 typ	
Small-Signal Forward-Current Transfer Ratio (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 1 mA, f = 1 kHz)	$h_{fe(D)}$	1300	
Small-Signal Input Impedance (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 1 mA, f = 1 kHz)	$h_{ie(D)}$	82	kΩ
Small-Signal Output Admittance (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 1 mA, f = 1 kHz)	$h_{oe(D)}$	108	μmhos
Small-Signal Reverse-Voltage Transfer Ratio (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 1 mA, f = 1 kHz)	$h_{re(D)}$	2.7×10^{-3}	
Voltage Gain (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 1 mA, f = 1 kHz)	$A_{(D)}$	26	dB
Power Gain (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 1 mA, f = 1 kHz)	$G_{p(D)}$	47	dB
Noise Voltage:			
f = 100 Hz	E_N	0.2 typ; 3 max	$\frac{\mu V_{(rms)}}{\sqrt{f(Hz)}}$
f = 1 kHz	E_N	0.05 typ; 0.3 max	$\frac{\mu V_{(rms)}}{\sqrt{f(Hz)}}$
f = 10 kHz	E_N	0.012 typ; 0.1 max	$\frac{\mu V_{(rms)}}{\sqrt{f(Hz)}}$
Input Admittance (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 2 mA, f = 50 MHz)	$y_{ie(D)}$	1.71 + j 2.8	mmhos



CA3036

Output Admittance (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 2 mA, f = 50 MHz)	$y_{oe(D)}$	3.96 + j 2.6	mmhos
Gain-Bandwidth Product (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 2 mA)	$f_{T(D)}$	200	MHz
For Each Input Transistor Q_1 or Q_3 (I_{C1} or I_{C3} = 1 mA, f = 1 kHz):			
Small-Signal Forward Current-Transfer Ratio	h_{fe}	82	
Small-Signal Input Impedance	h_{ie}	2.6	kΩ
Small-Signal Output Admittance	h_{oe}	7	μmhos
Small-Signal Reverse Voltage-Transfer Ratio	h_{re}	9.8×10^{-5}	

CA3037 OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead JEDEC MO-001-AD package; Outline No. 7. This type is electrically identical with type CA3008.

CA3037A OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier. multivibrator, oscillator, comparator, and servo driver applications. 14-lead JEDEC MO-001-AD package; Outline No. 7. This type is identical with type CA3037 except for the following items:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = +6V, V^- = −6V)

Input Offset Voltage	V_{IO}	0.9	mV
Input Offset Current	I_{IO}	0.3	μA
Input Bias Current	I_I	2.5	μA
Input Impedance	Z_{in}	20	kΩ
Output Impedance	Z_{out}	160	Ω
Noise Figure	NF	8.3	dB

CA3038 OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead JEDEC MO-001-AD package; Outline No. 7. This type is electrically identical with type CA3015.

OPERATIONAL AMPLIFIER CA3038A

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead JEDEC MO-001-AD package; Outline No. 7. This type is electrically identical with type CA3015A.

DIODE ARRAY CA3039

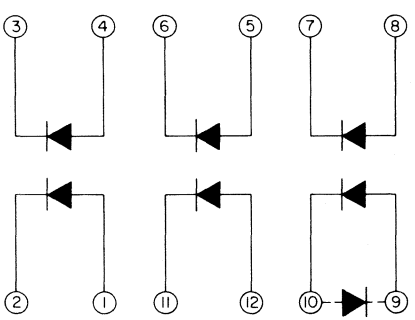
General-purpose diode array with six ultra-fast low capacitance matched diodes on a common monolithic substrate used for applications in communications and switching systems. 12-lead JEDEC MO-006-AG package; Outline No. 2.

MAXIMUM RATINGS

Peak Inverse Voltage:			
$D_1 - D_5$	PIV	5	V
D_6	PIV	0.5	V
Peak Diode-to-Substrate Voltage [$D_1 - D_5$ (terminals 1, 4, 5, 8, or 12 to terminal 10)]	V_{DI}	+20, −1	V
DC Forward Current	I_F	25	mA
Peak Recurrent Forward Current	I_f	100	mA
Peak Forward Surge Current	I_f (surge)	100	mA
Device Dissipation:			
Any one diode unit		100	mW
Total for device		600	mW
$T_A > 55°C$		Derate linearly 5.7	mW/°C
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

DC Forward Voltage Drop:			
$I_F = 50\ \mu A$	V_F	0.65 typ; 0.69 max	V
$I_F = 1\ \mu A$	V_F	0.73 typ; 0.78 max	V
$I_F = 3\ \mu A$	V_F	0.76 typ; 0.80 max	V
$I_F = 10\ \mu A$	V_F	0.81 typ; 0.90 max	V



CA3039

DC Reverse Breakdown Voltage ($I_R = -10\ \mu A$)	$V_{(BR)R}$	5 min; 7 typ	V
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate ($I_R = -10\ \mu A$)	$V_{(BR)R}$	20 min	V
Magnitude of Diode Offset Voltage Difference in DC Forward Voltage Drops of any Two Diode Units ($I_F = 1$ mA)	$\lvert V_{F1}-V_{F2}\rvert$	0.5 typ; 5 max	mV
DC Reverse (Leakage) Current ($V_R = -4V$)	I_R	0.016 typ; 100 max	nA
DC Reverse (Leakage) Current Between any Diode Unit and Substrate ($V_R = -10V$)	I_R	0.022 typ; 100 max	nA
Temperature Coefficient of $\lvert V_{F1}-V_{F2}\rvert$ ($I_F = 1$ mA)	$\frac{\Delta\lvert V_{F1}-V_{F2}\rvert}{\Delta T}$	1	$\mu V/°C$
Temperature Coefficient of Forward Drop ($I_F = 1$ mA)	$\frac{\Delta V_F}{\Delta T}$	−1.9	mV/°C
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S) ($I_F = 1$ mA)	V_F	0.65	V
Reverse Recovery Time ($I_F = 10$ mA, $I_R = 10$ mA)	t_{rr}	1	ns
Diode Resistance ($I_F = 1$ mA, $f = 1$ kHz)	R_D	25 to 45	Ω
Diode Capacitance ($V_R = -2V$, $I_F = 0$)	C_D	0.65	pF
Diode-to-Substrate Capacitance ($V_{DI} = 4V$, $I_F = 0$)	C_{DI}	3.2	pF

CA3040

VIDEO AND WIDE-BAND AMPLIFIER

General-purpose amplifier used for industrial and commercial equipment at frequencies up to 200 MHz. 12-lead JEDEC MO-006-AG package; Outline No. 2.

MAXIMUM RATINGS

Device Dissipation	450	mW
($T_A > 85°C$)	5	mW/°C
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

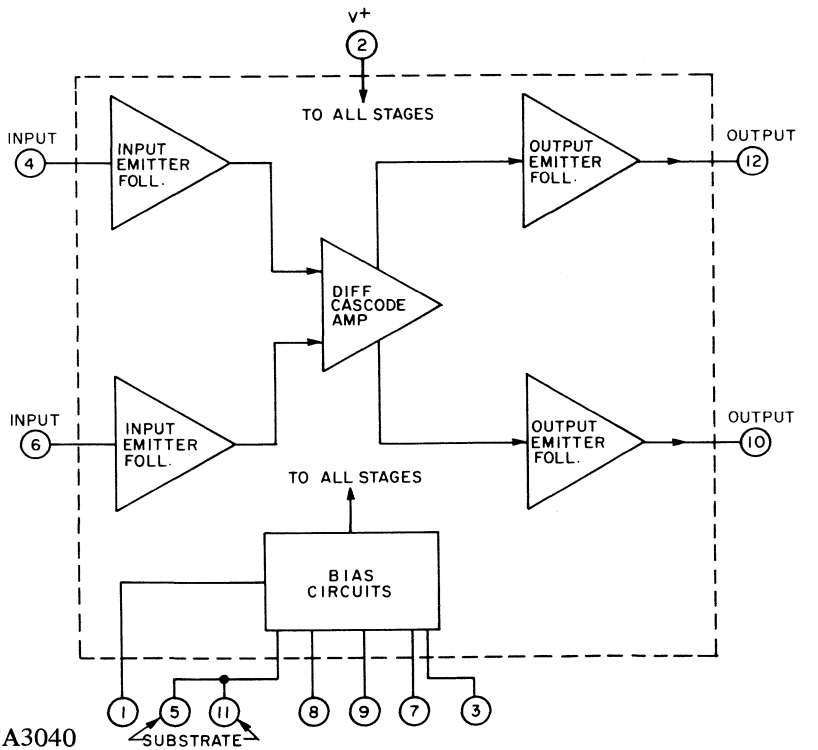
Static Characteristics ($V^+ = 6V$, $V^- = -6V$)

Output Voltage (Bias Mode A or B: Switch Closed)	V_{10} or V_{12}	1.4 to 3.7	V
Base Bias Voltage:			
Bias mode A switch closed	V_9	−1.7	V
Bias mode B switch	V_9	−4.7	V
Input Bias Reference Voltage (Bias Mode A or B: Switch Open)	V_1	−1 to 1	V
Input Bias Current (Bias Mode A or B: Switch Closed)	I_1, I_6	15 typ; 45 max	μA
Input Unbalance Current (Bias Mode A or B: Switch Closed)	I_6-I_1	−6 to 6	μA

Power Supply Current Drain:			
Mode A: Switch Open or Closed	I_2 or $I_5 + I_{11}$	4.7 to 15.5	mA
Mode B: Switch Open or Closed	I_2 or $I_5 + I_8 + I_{11}$	4.7 to 15.5	mA
Dynamic Characteristics			
($V^+ = 12V$, $V^- = 0$, Split Voltage Supply (Optional) = 6V)			
Differential Voltage Gain:			
Single-Ended Input Differential Output ($R_S = 50\ \Omega$, f = 1 MHz)	$A_{DIFF(DE)}$	34 min; 37 typ	dB
Single-Ended Input and Output ($R_S = 50\ \Omega$, f = 1 MHz)	$A_{DIFF(SE)}$	28 min; 31 typ	dB
−3-dB Bandwidth ($R_S = 50\ \Omega$)	BW	40 min; 55 typ	MHz
Differential Voltage Gain Balance (f = 1 MHz)	$A_{DIFF(SE)10}$ $-A_{DIFF(SE)12}$	−1 to 1	dB
Output Voltage Swing ($R_S = 50\ \Omega$, f = 1 MHz)	V_8 or V_{10} RMS	0.5	V_{RMS}
Noise Figure ($R_S = 400\ \Omega$, f = 30 MHz)	NF	9 typ; 11.5 max	dB
Parallel Input Resistance (f = 1 MHz)	R_I	150	kΩ
Parallel Input Capacitance (f = 1 MHz)	R_I	2.2	pF
Output Resistance (f = 1 MHz)	R_O	125	Ω

Temperature Dependent Characteristics (Temperature coefficients for T_A: $-55°C \leq T_A \leq 125°C$):

		Bias Mode A	Bias Mode B	
Output Voltage	$\frac{\Delta V_{10} \text{ or } \Delta V_{12}}{°C}$	0	6.4	mV/°C
Power Supply Current Drain	$\Delta I_2/°C$	5	—	μA/°C
Differential Voltage Gain	$A_{DIFF}/°C$	0.0166	0	dB/°C



CA3040

CA3041 WIDE-BAND AMPLIFIER, FM DETECTOR AF PREAMPLIFIER/DRIVER

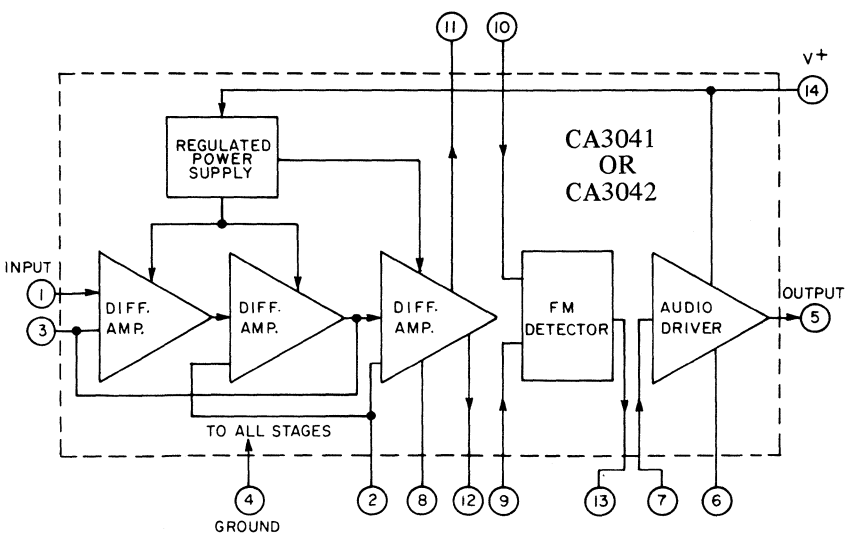
Special-purpose amplifier used for sound sections of television receivers using tube-type af output amplifiers. 14-lead JEDEC MO-001-AB package; Outline No. 9.

MAXIMUM RATINGS

Input Signal Voltage (Between terminals 1 and 3)	±3	V
Device Dissipation:		
T_A up to 25°C	950	mW
T_A above 25°C	Derate at 10.8	mW/°C
Temperature Range:		
Operating	0 to 85	°C
Storage	−25 to 85	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Total Device Dissipation:			
T_A = 0°C	P_T	220 to 270	mW
T_A = 25°C	P_T	225 to 275	mW
T_A = 85°C	P_T	230 to 280	mW
Zener Regulating Voltage, DC Supply Voltage at Terminal 14	V_{14}	10.6 to 11.8	V
Quiescent Operating Current, Into Terminal 11	I_{11}	0.25 to 1	mA
9-Volt Current Drain, Quiescent Operating Current into Terminal 14 (V^+ = 9V applied directly to terminal 14)	I_{14}	7 to 16	mA
Input-Impedance Components (f = 4.5 MHz):			
Parallel Input Resistance	R_i	11	kΩ
Parallel Input Capacitance	C_i	5	pF
Output-Impedance Components (f = 4.5 MHz):			
Parallel Output Resistance	R_o	100	kΩ
Parallel Output Capacitance	C_o	4	pF



Input Limiting Voltage, Knee (f = 4.5 MHz)	$V_{i(lim)}$	150 typ; 200 max	μV(rms)
Amplitude-Modulation Rejection (f = 4.5 MHz)	ARM	45 min; 58 typ	dB
IF-Amplifier Voltage Gain (f = 4.5 MHz)	$A_{(IF)}$	67	dB
Recovered AF Voltage: FM-Detector Output (R_L = 50 kΩ, Δ_f = ±25 kHz, THD = 0.7%typ., f = 4.5 MHz)	$V_o(af)$	250	mV(rms)
AF-Driver Output in Test Setup (THD < 5%, f = 4.5 MHz)	$V_o(af)$	8 min; 9 typ	V(rms)
Total Harmonic Distortion ($V_{o(af)}$ = $8V_{(rms)}$, f = 4.5 MHz)	THD	1.5 typ; 5 max	%
Discriminator Output Resistance (f = 1 kHz)	$R_{o(dis)}$	10	kΩ
AF-Amplifier Input Resistance (f = 1 kHz)	$R_{i(af)}$	100	kΩ
AF-Amplifier Output Resistance (f = 1 kHz)	$R_{o(af)}$	30	kΩ
AF-Driver Voltage Gain (f = 1 kHz)	A_{af}	41	dB

WIDE-BAND AMPLIFIER, FM DETECTOR AF PREAMPLIFIER/DRIVER CA3042

Special-purpose amplifier used for sound sections of television receivers using transistor-type af output amplifiers. 14-lead JEDEC MO-001-AB package; Outline No. 9. This type is identical with type CA3041 except for the following items:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

9-Volt Current Drain, Quiescent Operating Current into Terminal 14 (V^+ = 9V applied directly to terminal 14)	I_{14}	8 min; 18 typ	mA
Recovered AF Voltage (Δ_f = ±25 kHz, f = 4.5 MHz): FM-Detector Output (R_L = 50 kΩ, THD = 0.7% typ)	$V_o(af)$	250	mV(rms)
AF-Driver Output in TV-Receiver Sound System (R_L = 322 Ω, THD = 1.5% typ)	$V_o(af)$	3	V(rms)
AF-Driver Output in Test Setup (R_L = 322 Ω, THD < 5%)	$V_o(af)$	500 min; 800 typ	mV(rms)
Total Harmonic Distortion (Δf = ±25 kHz, f = 4.5 MHz): Test Setup ($V_o(af)$ = 500 mV(rms))	THD	1.5 typ; 5 max	%
TV Receiver Sound System ($V_o(af)$ = 1.3 V(rms))	THD	1	%
FM-Detector Output Resistance (f = 1 kHz)	$R_o(det)$	10	kΩ
AF-Driver Input Resistance (f = 1 kHz)	$R_i(af)$	100	kΩ
AF-Driver Output Resistance (f = 1 kHz)	$R_o(af)$	250	Ω
AF-Driver Voltage Gain (f = 1 kHz, R_S = 50 Ω, C_1 = 0)	A_{af}	30	dB

CA3043

FM IF AMPLIFIER, FM DETECTOR AF PREAMPLIFIER/DRIVER

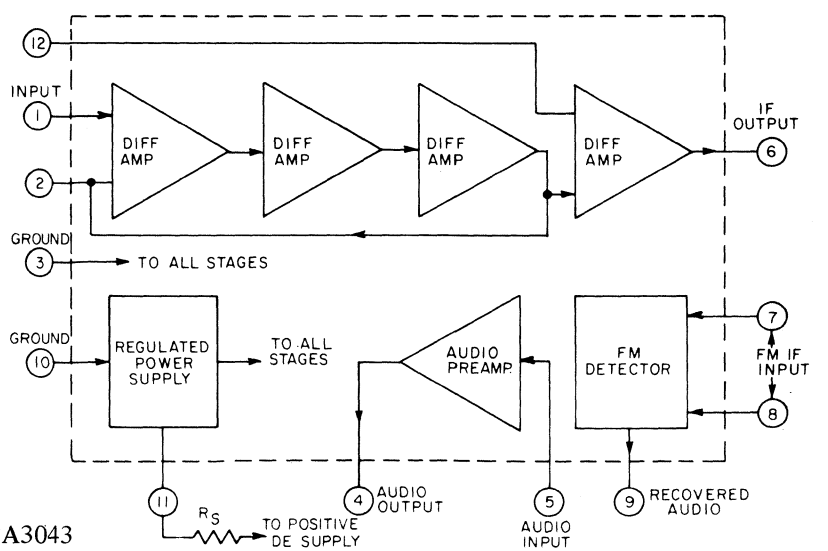
Special-purpose amplifier used in fm/if amplifier applications in communications receivers and high-fidelity fm receivers up to 20 MHz. 12-lead JEDEC MO-006-AG package; Outline No. 2.

MAXIMUM RATINGS

Device Dissipation:		
T_A = 25°C	300	mW
T_A above 25°C	Derate linearly 2	mW/°C
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Static Characteristics			
Current Drain at 6V into Pin No. 11 (V^+ = 6V)	I_{11}	10 to 20	mA
Regulator Voltage Pin No. 11	V_{11}	6.9 to 8	V
Total Device Dissipation	P_T	200 to 260	mW
Quiescent Operating Current into Pin No. 6 (V^+ = 30V, R_L = 750 Ω)	I_0	0.65	mA
Dynamic Characteristics			
(V^+ = 30V, R_L = 750 Ω, f = 10.7 MHz): Voltage Gain	A_v	72 min; 80 typ	dB
Input Limiting Voltage, Knee (v_o(af) at −3 dB point)	v_i(lim)	50	μV(RMS)
Limiting Current from Pin No. 6	I_o(lim)	0.42	mA(RMS)
Recovered AF Voltage (v_i = 1 mV(RMS), f (modulating) = 1 kHz, Deviation = ±75 MHz)	v_o(af)	75 to 150	mV(RMS)



CA3043

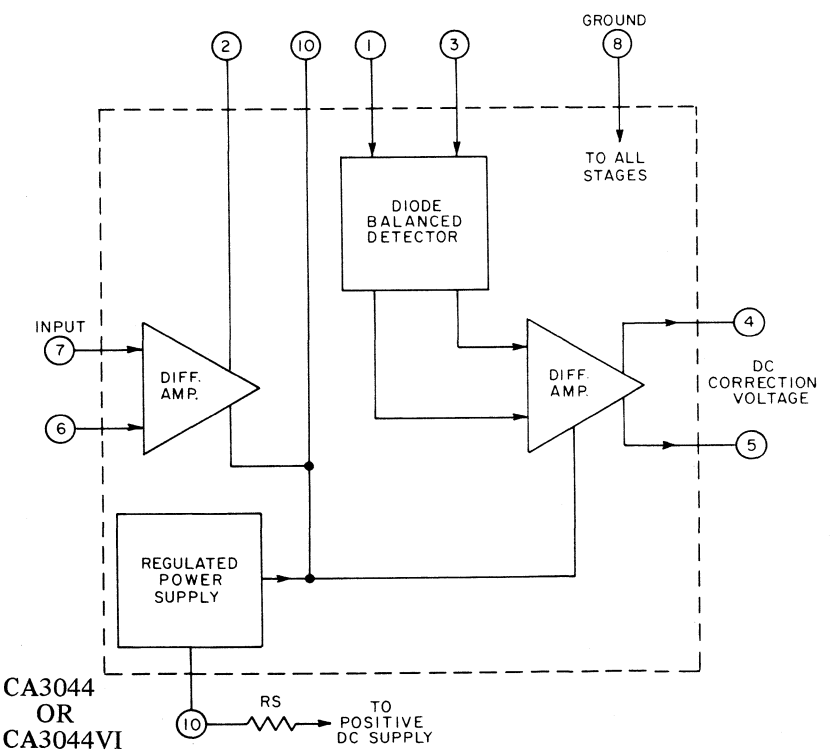
Amplitude-Modulation Rejection (v_i = 10 mV, f (modulating) = 1 kHz, % modulation = 50%)	AMR	58	dB
Total Harmonic Distortion (v_i = 1 mV(RMS))	THD	1	%
Input Impedance Components:			
Parallel Input Resistance	R_{IN}	7	kΩ
Parallel Input Capacitance	C_{IN}	5	pF

WIDE-BAND AMPLIFIER/ PHASE DETECTOR — CA3044

Special-purpose amplifier with internal zener diode voltage regulator used primarily for automatic frequency control applications. 10-lead JEDEC MO-006-AF package; Outline No. 1.

MAXIMUM RATINGS

Device Dissipation:		
T_A = 25°C	830	mW
T_A above 25°C	Derate linearly 5.6	mW/°C
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 200	°C



TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Static Characteristics			
Device Dissipation:			
$V^+ = 30$ V, $R_S = 1.5$ kΩ, $T_A = -55$°C	P_T	90 to 150	mW
$V^+ = 30$ V, $R_S = 1.5$ kΩ, $T_A = 125$°C	P_T	130 to 190	mW
$V^+ = 30$ V, $R_S = 1.5$ kΩ	P_T	110 to 170	mW
9-Volt Current Drain ($V_{10} = 9$V)	I_T	2.5 to 5.5	mA
Zener Regulating Voltage, DC Supply Voltage at Terminal 10 ($V^+ = 30$ V, $R_S = 1.5$ kΩ)	V_{10}	10.5 to 11.9	V
Quiescent Operating Current ($V^+ = 30$ V, $R_S = 1.5$ kΩ):			
Into terminal 2	I_2	1 to 4	mA
Terminal 4	V_4	5 to 8	V
Terminal 5	V_4	5 to 8	V
Between terminals 4 and 5	V_{4-5}	−1.5 to 1.5	V
Dynamic Characteristics (As RF Amplifier)			
Input Limiting Voltage, Knee ($f = 45.75$ MHz)	$V_{i(11m)}$	75	mV
Input Admittance ($V^+ = 30$ V, $R_S = 1.5$ kΩ, $f = 45.75$ MHz)	y_{11}	0.5 + j 1.1	mmhos
Reverse Transfer Admittance ($V^+ = 30$ V, $R_S = 1.5$ kΩ, $f = 45.75$ MHz)	y_{12}	3.8 + j 3.4	μmhos
Forward Transfer Admittance ($V^+ = 30$ V, $R_S = 1.5$ kΩ, $f = 45.75$ MHz)	y_{21}	−11.7 + 10.1	mmhos
Output Admittance ($V^+ = 30$ V, $R_S = 1.5$ kΩ, $f = 45.75$ MHz)	y_{22}	0.077 + j 0 + 9	mmhos
Output vs Frequency Deviation—AFC			
Correction-Control Voltage at Terminal 4 ($V^+ = 30$ V, $V_{in} = 200$ mV RMS, f_o = MHz as indicated):			
45.750 − 0.025	Vcorr.(4)	85% min of V_{10}	V
45.750 + 0.025	Vcorr.(4)	33% max of V_{10}	V
45.750 − 0.900	Vcorr.(4)	75% min of V_{10}	V
45.750 + 0.900	Vcorr.(4)	43% max of V_{10}	V
45.750 − 1.500	Vcorr.(4)	85% min of V_{10}	V
45.750 + 1.500	Vcorr.(4)	33% max of V_{10}	V
Correction-Control Voltage at Terminal 5 ($V^+ = 30$ V, $V_{in} = 200$ mV RMS, f_o = MHz as indicated):			
45.750 − 0.025	Vcorr.(5)	33% max of V_{10}	V
45.750 + 0.025	Vcorr.(5)	85% min of V_{10}	V
45.750 − 0.900	Vcorr.(5)	43% max of V_{10}	V
45.750 + 0.900	Vcorr.(5)	75% min of V_{10}	V
45.750 − 1.500	Vcorr.(5)	33% min of V_{10}	V
45.750 + 1.500	Vcorr.(5)	85% max of V_{10}	V

CA3044V1

WIDE-BAND AMPLIFIER/ PHASE DETECTOR

Special-purpose amplifier with internal zener diode voltage regulator used primarily for automatic frequency control applications. 10-formed-lead "TO-5" package; Outline No. 5. This type is electrically identical with type CA3044.

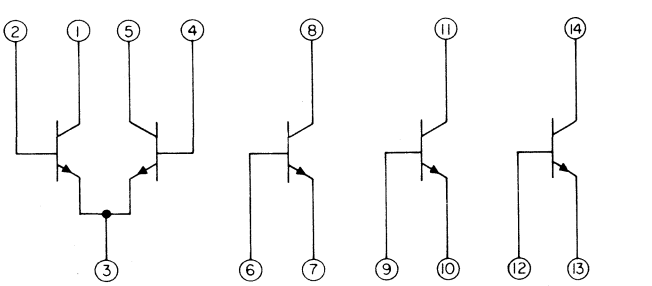
TRANSISTOR ARRAY CA3045

General-purpose array with three isolated transistors and one differentially-connected transistor pair used in low-power applications at frequencies from dc through the vhf range. 14-lead JEDEC MO-001-AD package; Outline No. 7.

MAXIMUM RATINGS		Each Transistor	Total Package	
Collector-to-Emitter Voltage	V_{CEO}	15	—	V
Collector-to-Base Voltage	V_{CBO}	20	—	V
Collector-to-Substrate Voltage	V_{CIO}	20	—	V
Emitter-to-Base Voltage	V_{EBO}	5	—	V
Collector Current	I_C	50	—	mA
Power Dissipation:				
T_A = 25°C		300	750	mW
T_A = 25 to 75°C		300	750	mW
T_A > 75°C		Derate at 8		mW/°C
Temperature Range:				
Operating		−55 to 125		°C
Storage		−65 to 200		°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Static Characteristics			
Collector-to-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	$V_{(BR)CBO}$	20 min; 60 typ	V
Collector-to-Emitter Breakdown Voltage (I_C = 1 mA, I_B = 0)	$V_{(BR)CEO}$	15 min; 24 typ	V
Collector-to-Substrate Breakdown Voltage (I_C = 10 μA, I_{CI} = 0)	$V_{(BR)CIO}$	20 min; 60 typ	V
Emitter-to-Base Breakdown Voltage (I_E = 10 μA, I_C = 0)	$V_{(BR)EBO}$	5 min; 7 typ	V
Collector-Cutoff Current (V_{CB} = 10 V, I_E = 0)	I_{CBO}	0.002 typ; 40 max	nA
Collector-Cutoff Current (V_{CE} = 10 V, I_B = 0)	I_{CEO}	0.5 max	μA
Static Forward Current-Transfer Ratio:			
V_{CE} = 3V, I_C = 10 mA	h_{FE}	100	
V_{CE} = 3V, I_C = 1 mA	h_{FE}	40 min; 100 typ	
V_{CE} = 3V, I_C = 10 μA	h_{FE}	54	



CA3045 OR CA3046

Input Offset Current for Matched Pair Q_1 and Q_2 $\lvert I_{IO1} - I_{IO2} \rvert$ (V_{CE} = 3V, I_C = 1 mA)		0.3 typ; 2 max	μA
Base-to-Emitter Voltage:			
V_{CE} = 3 V, I_E = 1 mA	V_{BE}	0.715	V
V_{CE} = 3V, I_E = 10 mA	V_{BE}	0.8	V
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE1} - V_{BE2} \rvert$ (V_{CE} = 3V, I_C = 1 mA)		0.45 typ; 5 max	mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE3} - V_{BE4} \rvert$, $\lvert V_{BE4} - V_{BE5} \rvert$, $\lvert V_{BE5} - V_{BE3} \rvert$ (V_{CE} = 3V, I_C = 1 mA)		0.45 typ; 5 max	mV
Temperature Coefficient of Base-to-Emitter Voltage (V_{CE} = 3V, I_C = 1 mA)	$\frac{\Delta V_{BE}}{\Delta T}$	−1.9	mV/°C
Collector-to-Emitter Saturation Voltage (I_B = 1 mA, I_C = 10 mA)	V_{CES}	0.23	V
Temperature Coefficient, Magnitude of Input-Offset Voltage (V_{CE} = 3V, I_C = 1 mA)	$\frac{\Delta V_{IO}}{\Delta T}$	1.1	μV/°C
Dynamic Characteristics			
Low-Frequency Noise Figure (V_{CE} = 3V, I_C = 100 μA, source resistance = 1 kΩ, f = 1 kHz)	NF	3.25	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics (V_{CE} = 3V, I_C = 1 mA, f = 1 kHz):			
Forward-current transfer ratio	h_{fe}	110	
Short-circuit input impedance	h_{ie}	3.5	kΩ
Open-circuit output impedance	h_{oe}	15.6	μmhos
Open-circuit reverse voltage-transfer ratio	h_{re}	1.8×10^{-4}	
Admittance Characteristics (V_{CE} = 3V, I_C = 1 mA, f = 1 MHz):			
Forward transfer admittance	Y_{fe}	31 − j 1.5	
Input admittance	Y_{ie}	0.3 + j 0.04	
Output admittance	Y_{oe}	0.001 + j 0.03	
Gain-Bandwidth Product (V_{CE} = 3V, I_C = 3 mA)	f_T	300 min; 550 typ	MHz
Emitter-to-Base Capacitance (V_{EB} = 3V, I_E = 0)	C_{EB}	0.6	pF
Collector-to-Base Capacitance (V_{CB} = 3V, I_C = 0)	C_{CB}	0.58	pF
Collector-to-Substrate Capacitance (V_{CS} = 3V, I_C = 0)	C_{CI}	2.8	pF

CA3046 TRANSISTOR ARRAY

General-purpose array with three isolated transistors and one differentially-connected transistor pair used in low-power applications at frequencies from dc through the vhf range. 14-lead JEDEC MO-001-AB package; Outline No. 6. This type is identical with type CA3045 except for the following items:

MAXIMUM RATINGS		Each Transistor	Total Package	
Collector-to-Emitter Voltage	V_{CEO}	15	—	V
Collector-to-Base Voltage	V_{CBO}	20	—	V
Collector-to-Substrate Voltage	V_{CIO}	20	—	V
Emitter-to-Base Voltage	V_{EBO}	5	—	V

Collector Current	I_C	50	—	mA
Power Dissipation:				
T_A = 25°C		300	750	mW
T_A = 25 to 55°C		300	750	mW
T_A > 55°C		Derate at 6.67		mW/°C
Temperature Range:				
Operating		0 to 85		°C
Storage		−25 to 85		°C

OPERATIONAL AMPLIFIER — CA3047

General-purpose amplifier used for critical applications requiring substantial output current. 14-lead JEDEC MO-001-AB package; Outline No. 8. This type is identical with type CA3033 except for the following items:

MAXIMUM RATINGS

Device Dissipation:		
T_A up to 25°C	750	mW
T_A above 25°C	Derate at 6.67	mW/°C
Temperature Range:		
Operating	0 to 70	°C
Storage	−25 to 85	°C

OPERATIONAL AMPLIFIER — CA3047A

General-purpose amplifier used for critical applications requiring substantial output current. 14-lead JEDEC MO-001-AB package; Outline No. 8. This type is identical with type CA3033A except for the following items:

MAXIMUM RATINGS

Device Dissipation:		
T_A up to 25°C	750	mW
T_A above 25°C	Derate at 6.67	mW/°C
Temperature Range:		
Operating	0 to 70	°C
Storage	−25 to 85	°C

AMPLIFIER ARRAY — CA3048

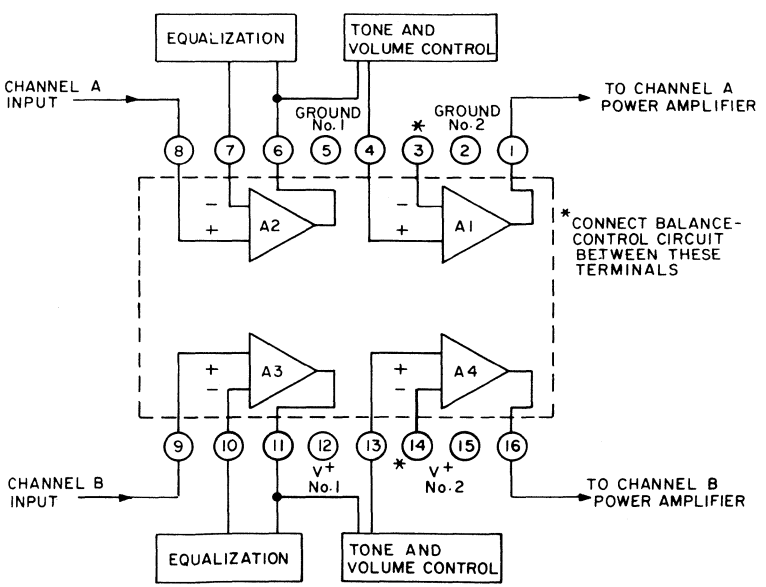
Special-purpose array with four independent ac amplifiers used in low-noise and general ac applications in industrial service. 16-lead JEDEC MO-001-AC package; Outline No. 10.

MAXIMUM RATINGS

Power Supply Voltage	16	V
AC Input Voltage	0.5	Vrms
Device Dissipation:		
T_A = 55°C	750	mW
T_A above 55°C	Derate linearly at 7.7	mW/°C
Temperature Range:		
Operating	−25 to 85	°C
Storage	−25 to 85	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Static Characteristics (V^+ = 12V)			
Current drain per amplifier drain	I_{12} or I_{15}	9.5 to 17.5	mA
DC Voltage at Output Terminals	V_1, V_6, V_{11}, V_{16}	6.1 to 8.1	V
DC Voltage at Feedback Terminals	V_3, V_7, V_{10}, V_{14}	1.7 to 2.3	V
DC Voltage at Input Terminals	V_4, V_8, V_9, V_{13}	2.2 to 2.8	V
Dynamic Characteristics (Each Amplifier with no AC feedback)			
Open-Loop Gain (V^+ = 12 V, E_{IN} = 2mV, f = 10 kHz)	A_{OL}	53 min; 58 typ	dB
Output Voltage Swing (V^+ = 12 V, THD = 5%, f = 1 kHz)	V_O(rms)	2 min; 2.4 typ	V
Open-Loop −3dB Bandwidth (V^+ = 12V, E_{IN} = 2 mV)	BW	250 min; 300 typ	kHz
Total Harmonic Distortion (V^+ = 12V, E_{OUT} = 2 Vrms, f = 1 kHz)	THD	0.65	%
Input Resistance (Open loop, terminals 3, 7, 10, and 14 are bypassed to ground, f = 1 kHz)	R_{IN}	90	kΩ
Input Capacitance (f = 1 MHz)	C_{IN}	9	pF
Ouput Resistance (Terminals 3, 7, 10, and 14 are bypassed to ground)	R_{OUT}	1	kΩ
Output Capacitance (f = 1 MHz)	C_{OUT}	18	pF
Feedback Capacitance, Output to Non-Inverting Input (V^+ = 12V, f = 1 MHz)	C_{FB}	<0.1	pF
Broad-Band Output Noise Voltage (V^+ = 12V, R_S = 10 kΩ, A = 40 dB, equivalent noise BW = 50 kHz)	E_N	0.3 typ; 1 max	mV
Output Noise Voltage, Weighted	$E_{N(WT)}$	0.5 typ; 2.2 max	mV



CA3048

Noise Figure (R_S = 10 kΩ):			
f = 10 Hz	NF	10	dB
f = 100 Hz	NF	5.8	dB
f = 1 kHz	NF	2	dB
f = 10 kHz	NF	1.1	dB
f = 100 kHz	NF	0.6	dB
Inter-Amplifier Audio Separation, "Cross Talk" (V^+ = 12V, 0dB = 0.78V, f = 1 kHz)		<−45	dB
Inter-Amplifier Capacitance, Any amplifier output to any other amplifier unit (V^+ = 12V, f = 1 MHz)	C	<0.02	pF

DUAL INDEPENDENT DIFFERENTIAL RF/IF AMPLIFIER — CA3049

General-purpose amplifier used in low-power applications at frequencies up to 500 MHz. 12-lead JEDEC MO-006-AG package; Outline No. 2.

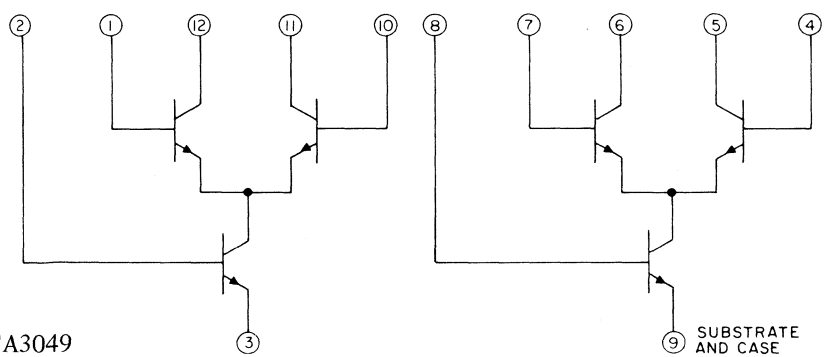
MAXIMUM RATINGS

Each Transistor:			
Collector-to-Emitter Voltage	V_{CEO}	15	V
Collector-to-Base Voltage	V_{CBO}	20	V
Collector-to-Substrate Voltage	V_{CIO}	20	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	50	mA
Device Dissipation:			
Any one transistor		300	mW
Total package		600	mW
T_A > 55°C		Derate at 5	mW/°C
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Static Characteristics (For each transistor)			
Collector-to-Emitter Breakdown Voltage (I_C = 1 mA, I_B = 0)	$V_{(BR)CEO}$	15 min	V
Collector-to-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	$V_{(BR)CBO}$	20 min	V
Collector-to-Substrate Breakdown Voltage (I_C = 10 μA, I_{CI} = 0)	$V_{(BR)CIO}$	20 min	V
Emitter-to-Base Breakdown Voltage (I_E = 10 μA, I_C = 0)	$V_{(BR)EBO}$	5 min	V
Input Bias Current (V_{CE} = 3V, I_C = 1 mA)	I_{IO}	10 typ; 33 max	μA
Collector-Cutoff Current (V_{CB} = 10V, I_E = 0)	I_{CBO}	100 max	nA
Dynamic Characteristics			
Gain-Bandwidth Product, Per Unit (V_{CE} = 6V, I_C = 2 mA)	f_T	1.3	GHz
Collector-Base Capacitance (V_{CB} = 6V, I_C = 0)	C_{CB}	0.86	pF
Collector-Substrate Capacitance (V_{CI} = 6V, I_C = 0)	C_{CI}	1.92	pF

		Differential Amplifier	Cascode Amplifier	
Insertion Power Gain (V^+ = 12V, $I_3 = I_9$ = 2mA, $I_C \cong$ 2mA, f = 200 MHz)	G_p	—	19 min; 23 typ	dB
Noise Figure (V^+ = 12V, $I_3 = I_9$ = 2mA, $I_C \cong$ 2mA, f = 200 MHz)	NF	—	4.6 typ; 6.5 max	dB
Input Admittance:				
V^+ = 12V, $I_3 = I_9$ = 2 mA, $I_C \cong$ 2 mA, f = 200 MHz	Y_{11}	—	1.5 + j 2.45	mmho
V^+ = 12V, $I_3 = I_9$ = 4 mA, $I_C \cong$ 2 mA, f = 200 MHz	Y_{11}	0.875 + j 1.3	—	mmho
Reverse Transfer Admittance:				
V^+ = 12V, $I_3 = I_9$ = 2 mA, $I_C \cong$ 2 mA, f = 200 MHz	Y_{12}	--	0 − j 0.008	mmho
V^+ = 12V, $I_3 = I_9$ = 4 mA, $I_C \cong$ 2 mA, f = 200 MHz	Y_{12}	0. − j 0.013	—	mmho
Forward Transfer Admittance:				
V^+ = 12V, $I_3 = I_9$ = 2 mA, $I_C \cong$ 2 mA, f = 200 MHz	Y_{21}	—	17.9 − j 30.7	mmho
V^+ = 12V, $I_3 = I_9$ = 4 mA, $I_C \cong$ 2 mA, f = 200 MHz	Y_{21}	−10.5 + j 13	—	mmho
Output Admittance:				
V^+ = 12V, $I_3 = I_9$ = 2 mA, $I_C \cong$ 2 mA, f = 200 MHz	Y_{22}	—	−0.503 − j 15	mmho
V^+ = 12V, $I_3 = I_9$ = 4 mA, $I_C \cong$ 2 mA, f = 200 MHz	Y_{22}	0.071 + j 0.62	—	mmho



CA3049

CA3050 DUAL DIFFERENTIAL AMPLIFIER

General-purpose amplifier with two Darlington connected differential amplifiers with diode bias string used in low-power applications at frequencies from dc to 20 MHz. 14-lead JEDEC MO-001-AD package; Outline No. 7.

MAXIMUM RATINGS

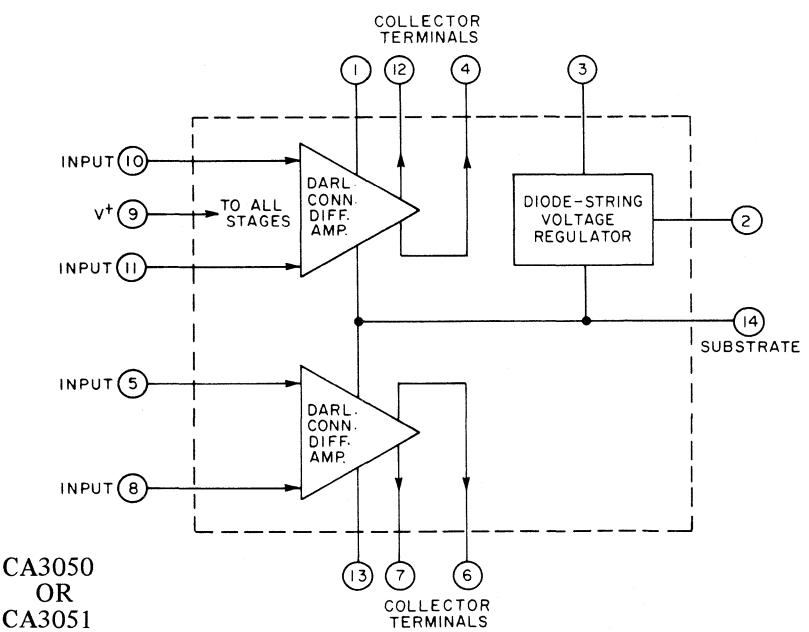
Collector-to-Emitter Voltage	V_{CEO}	15	V
Collector-to-Base Voltage	V_{CBO}	20	V
Collector-to-Substrate Voltage	V_{CIO}	20	V

Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	50	mA
Device Dissipation:			
Any one transistor		150	mW
Total package		900	mW
$T_A > 55°C$		Derate at 8	mW/°C
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Static Characteristics

Input Offset Voltage ($V^+ = 6V$, $I_8 = 2$ mA)	V_{IO}	1.5 typ; 5 max	mV
Input Offset Current ($V^+ = 6V$, $I_3 = 2$ mA)	I_{IO}	7 typ; 70 max	nA
Input Bias Current ($V^+ = 6V$, $I_3 = 2$ mA)	I_I	200 typ; 500 max	nA
Quiescent Operating Current Ratio ($V^+ = 6V$, $I_3 = 2$ mA)	$\left\lvert \frac{I_4 + I_{12}}{I_3} \text{ or } \frac{I_6 + I_7}{I_3} \right\rvert$	0.9 to 1.13	
DC Forward Base-to-Emitter Voltage:			
$V_{CE} = 3V$, $I_C = 50\ \mu A$	V_{BE}	0.645 typ; 0.7 max	V
$V_{CE} = 3V$, $I_C = 1$ mA	V_{BE}	0.725 typ; 0.8 max	V
$V_{CE} = 3V$, $I_C = 3$ mA	V_{BE}	0.76 typ; 0.85 max	V
$V_{CE} = 3V$, $I_C = 10$ mA	V_{BE}	0.805 typ; 0.9 max	V
Temperature Coefficient of Base-to-Emitter Voltage ($V_{CE} = 3V$, $I_C = 1$ mA)	$\frac{\Delta V_{BE}}{\Delta T}$	−1.9	mV/°C



CA3050
OR
CA3051

Collector-to-Emitter Breakdown Voltage (I_C = 1 mA, I_B = 0)	$V_{(BR)CEO}$	15 min; 24 typ	V
Collector-to-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	$V_{(BR)CBO}$	20 min; 60 typ	V
Collector-to-Substrate Breakdown Voltage (I_C = 10 μA, I_{CI} = 0)	$V_{(BR)CIO}$	20 min; 60 typ	V
Dynamic Characteristics			
Emitter-to-Base Breakdown Voltage (I_E = 10 μA, I_C = 0)	$V_{(BR)EBO}$	5 min; 7 typ	V
Collector-Cutoff Current (V_{CB} = 10 V, I_E = 0)	I_{CBO}	0.002 typ; 100 max	nA
Emitter-to-Base Capacitance (V_{EB} = 3V, I_E = 0)	C_{EB}	0.78	pF
Collector-to-Base Capacitance (V_{CB} = 3V, I_C = 0)	C_{CB}	0.47	pF
Collector-to-Substrate Capacitance (V_{CS} = 3V, I_C = 0)	C_{CI}	1.92	pF
Gain-Bandwidth Product, For Single Transistor (V_{CE} = 5V, I_C = 3 mA)	f_T	600	MHz
Forward Transadmittance, With Single-Ended Input and Output (V^+ = 10 V, I_3 = 2 mA, f = 1 MHz)	$\|y_{21}\|$	7 to 11	mmhos
−3-dB Bandwidth (V^+ = 10 V, I_3 = 2 mA)	BW	4.3	MHz
Input Impedance (V^+ = 10 V, I_3 = 2 mA, f = 1 kHz)	Z_{IN}	460	kΩ
Output Impedance (I_3 = 2 mA, f = 1 kHz)	Z_{OUT}	170	kΩ
Common-Mode Rejection Ratio (I_3 = 2 mA, f = 1 kHz)	CMRR	65	dB
AGC Range (I_3 = 2 mA, f = 1 kHz, terminal No. 3 grounded)	AGC	60	dB

CA3051 DUAL DIFFERENTIAL AMPLIFIER

General-purpose amplifier with two Darlington connected differential amplifiers with diode bias string used in low-power applications at frequencies from dc to 20 MHz. 14-lead JEDEC MO-001-AB package; Outline No. 8. This type is identical with type CA3050 except for the following items:

MAXIMUM RATINGS

Device Dissipation:		
Total package	750	mW
T_A > 55°C	Derate at 6.67	mW/°C
Temperature Range:		
Operating	−25 to 85	°C
Storage	−25 to 85	°C

CA3052 STEREO PREAMPLIFIER

Special-purpose array with four independent ac amplifiers used in stereo preamplifiers, magnetic pickups, tape heads, and tone generators. 16-lead JEDEC MO-001-AC package; Outline No. 10. The functional diagram for this type is identical to that of type CA3048.

MAXIMUM RATINGS

Power Supply Voltage	16	V
AC Input Voltage	0.5	Vrms
Device Dissipation:		
T_A = 55°C	750	mW
T_A above 55°C	Derate linearly at 7.7	mW/°C
Temperature Range:		
Operating	−25 to 85	°C
Storage	−25 to 85	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Static Characteristics (V^+ = 12V)			
Current drain per amplifier pair	I_{12} or I_{15}	9.5 to 17.5	mA
DC Voltage at Output Terminals	V_1, V_6, V_{11}, V_{16}	6.1 to 8.1	V
DC Voltage at Feedback Terminals	V_3, V_7, V_{10}, V_{14}	1.7 to 2.3	V
DC Voltage at Input Terminals	V_4, V_8, V_9, V_{13}	2.2 to 2.8	V
Dynamic Characteristics, Each amplifier with no feedback; terminals 3, 7, 10, and 14 bypassed to ground:			
Open-Loop Gain (V^+ = 12V, E_{IN} = 2 mV, f = 10 kHz)	A_{OL}	53 min; 58 typ	dB
Open-Loop Output Voltage Swing (V^+ = 12V, THD = 5%, f = 1 kHz)	V_O(rms)	2 min; 2.4 typ	V
Open-Loop—3-dB Bandwidth (V^+ = 12V, E_{IN} = 2 mV)	BW	300	kHz
Open-Loop Total Harmonic Distortion (V^+ = 12V, E_{OUT} = 2 Vrms, f = 1 kHz)	THD	0.65	%
Input Resistance (V^+ = 12V, f = 1 kHz)	R_{IN}	90	kΩ
Input Capacitance (V^+ = 12V, f = 1 MHz)	C_{IN}	9	pF
Output Resistance (V^+ = 12V, f = 1 kHz)	R_{OUT}	1	kΩ
Feedback Capacitance, Output to non-inverting input (V^+ = 12V, f = 1 MHz)	C_{FB}	<0.1	pF
Equivalent Input Noise Voltage, Amplifiers 1 and 4, "C" filter at output (V^+ = 10 V, R_S = 5 kΩ, A = 45 dB)	E_N	1.7 typ; 6.4 max	μV
Equivalent Input Noise Voltage, Amplifiers 2 and 3, RIAA compensated (V^+ = 10 V, R_S = 5 kΩ, A = 64 dB (1 kHz))	E_{N2}	4 typ; 15 max	μV
Inter-Amplifier Audio Separation, Cross Talk (V^+ = 12 V, 0dB = 0.78 V, f = 1 kHz)		<−45	dB
Inter-Amplifier Capacitance, Any amplifier output to any other amplifier input (V^+ = 12 V, f = 1 MHz)	C	<0.02	pF

DIFFERENTIAL/ CASCODE AMPLIFIER — CA3053

General-purpose amplifier used in communications and industrial equipment at frequencies from dc to 120 MHz. 8-lead JEDEC MO-002-AL package; Outline No. 4. This type is identical with type CA3028A except for the following items:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

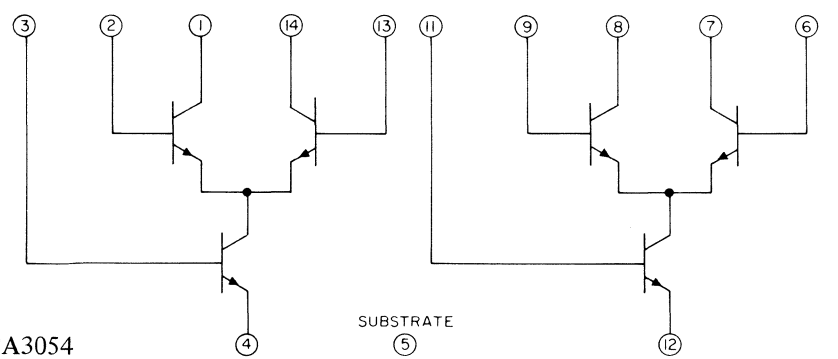
Static Characteristics			
Input Bias Current:			
$V^+ = 9V$	I_I	29 typ; 85 max	μA
$V^+ = 12V$	I_I	36 typ; 125 max	μA
Quiescent Operating Current:			
$V^+ = 9V$	I_6 or I_8	1.2 to 3.5	mA
$V^+ = 12V$	I_6 or I_8	2 to 5	mA
AGC Bias Current, Into Constant-Current Source Terminal No. 7:			
$V^+ = 9V$	I_7	1.15	mA
$V^+ = 12V$	I_7	1.55	mA
Device Dissipation:			
$V^+ = 9V$	P_T	50 typ; 80 max	mW
$V^+ = 12V$	P_T	100 typ; 150 max	mW

CA3054 DIFFERENTIAL AMPLIFIER

General-purpose array consisting of two independent differential amplifiers with associated constant-current transistors used in low-power applications at frequencies from dc to 120 MHz. 14-lead JEDEC MO-001-AB package; Outline No. 8. This type is identical with type CA3026 except for the following items:

MAXIMUM RATINGS

Power Dissipation:		
Total package	750	mW
$T_A > 55°C$	6.67	mW/°C
Temperature Range:		
Operating	0 to 85	°C
Storage	−25 to 85	°C



CA3054

CA3055 VOLTAGE REGULATOR

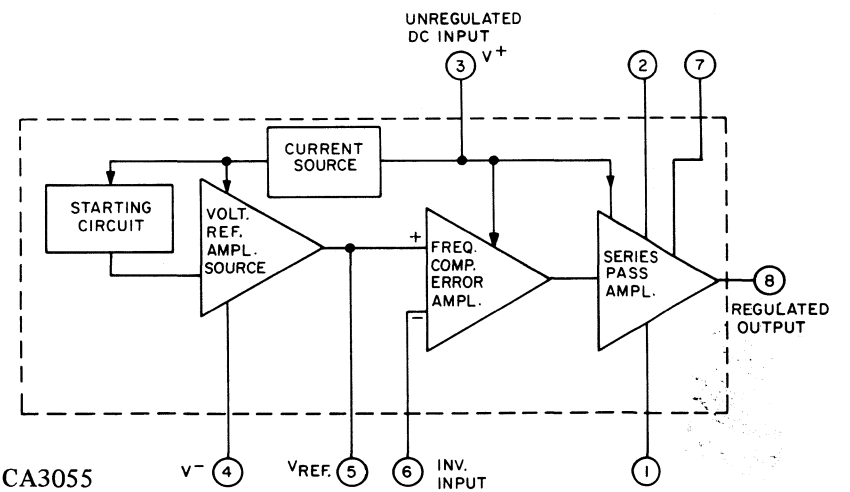
Special-purpose device used in shunt voltage, current, switching voltage, and high-current voltage regulators. 8-lead JEDEC MO-002-AL package; Outline No. 4.

MAXIMUM RATINGS

	Without Heat Sink	With Heat Sink	
Power Dissipation:			
T_A up to 55°C	630	0.0016	mW
T_A above 55°C	Derate linearly at 6.67	Derate linearly at 16.7	mW/°C
Temperature Range:			
Operating	−55 to 125		°C
Storage	−65 to 150		°C
Unregulated Input Voltage	40		V

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Static Characteristics			
Reference Voltage (V_{IN} = 15 V)	V_{ref}	1.4 to 1.8	V
Quiescent Regulator Current (V_{IN} = 15 V)	$I_{quiescent}$	7 typ; 10 max	mA
Input Voltage Range	V_{IR}	7.5 to 40	V
Maximum Output Voltage (V_{IN} = 40 V, R_L = 365 Ω, terminal No. 6 to ground)	V_O(max)	34 min; 36 typ	V
Minimum Output Voltage (V_{IN} = 7.5 V, terminal No. 6 connected to terminal No. 1)	V_O(min)	1.6 typ; 1.8 max	V
Limiting Current (V_{IN} = 7.5 V)	I_{limit}	115	mA
Dynamic Characteristics			
Equivalent Noise Output Voltage:			
Reference capacitance = 0	V_{noise}	0.7	mV
Reference capacitance = 0.22 μF	V_{noise}	0.45	mV
Input Regulation, Line Regulation (V_{IN} = 22V, f = 1 kHz):			
Reference capacitance = 0	Reg_l	45 min; 50 typ	dB
Reference capacitance = 2 μF	Reg_l	50 min; 56 typ	dB
Output Resistance (V_{IN} = 27V, f = 1 kHz)	r_o	0.075 typ; 0.3 max	Ω
Temperature Coefficient of Reference and Output Voltages	$\Delta V_{ref}, \Delta V_o$	0.075 typ; 0.3 max	Ω
Recovery Time:			
Turn-On (V_{IN} = 22V + 50 mA step)	t_r(on)	1	μs
Turn-Off (V_{IN} = 22V − 50 mA step)	t_r(off)	3	μs



OPERATIONAL AMPLIFIER CA3056A

General-purpose amplifier with internal phase compensation used in military, industrial and consumer applications. 8-lead JEDEC MO-002-AL package; Outline No. 4.

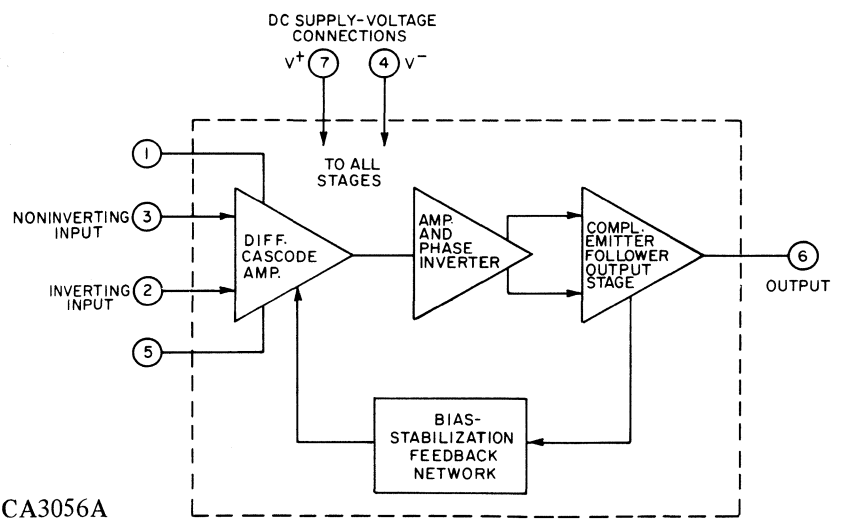
MAXIMUM RATINGS

Supply Voltage	±22	V
Input-Signal Voltage	±15	V
Device Dissipation:		
T_A up to 75°C	500	mW
T_A above 75°C	Derate at 6.5	mW/°C
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 150	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Static Characteristics

Input Offset Voltage:			
$R_S \geq 10$ kΩ, $T_A = 25°C$	V_{IO}	1 typ; 5 max	mV
$R_S \geq 10$ kΩ, $T_A = -55$ to 125°C	V_{IO}	6 max	mV
Input Offset Current:			
$T_A = 25°C$	I_{IO}	30 typ; 200 max	nA
$T_A = -55$ to 125°C	I_{IO}	500 max	μA
Input Bias Current:			
$T_A = 25°C$	I_I	200 typ; 500 max	nA
$T_A = -55$ to 125°C	I_I	1.5 max	μA
Input Offset Voltage Sensitivity:			
Positive, $R_S \leq 10$ kΩ	$\Delta V_{IO}/\Delta V_{CC}$	30 typ; 150 max	μV/V
Negative, $R_S \leq 10$ kΩ	$\Delta V_{IO}/\Delta V_{EE}$	30 typ; 150 max	μV/V
Device Dissipation	P_T	50 typ; 85 max	mW



CA3056A

Dynamic Characteristics

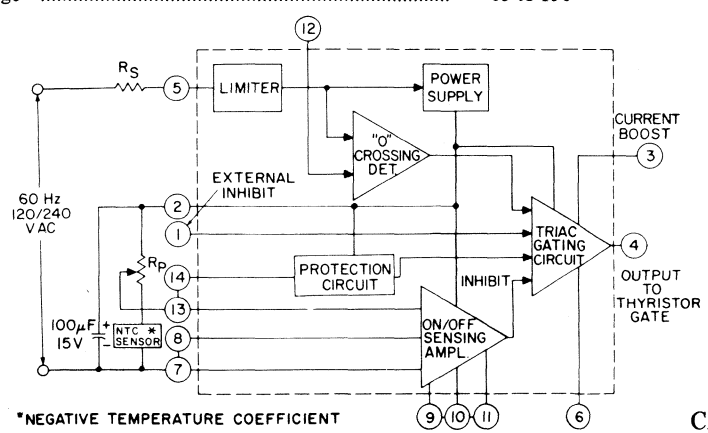
Open-Loop Differential Voltage Gain:			
V_{OUT} = 10V, $R_L \geq$ 2 kΩ, T_A = 25°C	A_{OL}	50000 min; 200000 typ	
V_{OUT} = 10V, $R_L \geq$ 2 kΩ, T_A = −55 to 125°C	A_{OL}	25000 min	
Transient Response (Unity gain, V_{in} = 20 mV, R_L = 2 kΩ, $C_L \leq$ 100 pF):			
Rise time		0.3	μs
Overshoot		5	%
Common-Mode Rejection Ratio ($R_S \leq$ 10 kΩ)	CMRR	70 min; 90 typ	dB
Common-Mode Input-Voltage Range	V_{CMR}	−12 to 12	V
Maximum Output-Voltage Swing:			
$R_L \geq$ 10 kΩ, T_A = 25°C	V_O(P-P)	24 min; 28 typ	V
$R_L \geq$ 2 kΩ, T_A = 25°C	V_O(P-P)	20 min; 26 typ	V
$R_L \geq$ 2 kΩ, T_A = −55 to 125°C	V_O(P-P)	20 min	V
Input Resistance	R_{in}	0.3 min; 1 typ	mΩ
Slew Rate (Unity Gain, $R_L \geq$ 2 kΩ)	SR	0.5	V/μs

INTEGRAL-CYCLE ZERO-VOLTAGE SWITCH — CA3059

Special-purpose switch used to control a thyristor in a variety of ac power switching applications. 14-lead JEDEC MO-001-AB package; Outline No. 11.

MAXIMUM RATINGS

DC Supply Voltage, between terminals 2 and 7	14	V
DC Supply Voltage, between terminals 2 and 8	14	V
Peak Supply Current, terminals 5 and 7	±50	mA
Ouput Pulse Current, terminal 4	150	mA
Power Dissipation:		
T_A up to 55°C	700	
T_A above 55°C	Derate linearly 6.67	mW/°C
Temperature Range:		
Operating	−40 to 85	°C
Storage	−65 to 150	°C



CA3059

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Following conditions at 120 Vrms, 50-60 Hz (AC Line Voltage):			
DC Supply Voltage (R_S = 10 kΩ, I_L = 0):			
Inhibit Mode	V_S	6.1 to 7	V
Pulse Mode	V_S	6 to 7	V
DC Supply Voltage (R_S = 5 kΩ, I_L = 2 mA):			
Inhibit Mode	V_S	6.4	V
Pulse Mode	V_S	6.3	V
Peak Output Current (Pulsed) with Internal Power Supply:			
Terminal 3 open, V_{GT} = 0	$I_{OM(4)}$	50 min; 84 typ	mA
Terminal 3 connected to terminal 2, V_{GT} = 0	$I_{OM(4)}$	90 min; 124 typ	mA
Peak Output Current (Pulsed) with External Power Supply:			
Terminal 3 open, V^+ = 12V, V_{GT} = 0	$I_{OM(4)}$	170	mA
Terminal 3 connected to terminal 2, V_{GT} = 1V	$I_{OM(4)}$	240	mA
Gate Trigger Current (Terminal 3 connected to terminal 2, V_{GT} = 1V)	$I_{GT(4)}$	105	mA
Output Leakage Current Inhibit Mode	I_4	10 max	μA
Input Bias Current	I_I	220 typ; 1000 max	nA
Inhibit Input Ratio (Voltage ratio of terminal 9 to terminal 2)	V_9/V_2	0.465 to 0.520	
Total Gate Pule Duration (External capacitance $C_{(EXT)}$ = 0, R = ∞):			
Positive dv/dt	t_P	70 to 140	μs
Negative dv/dt	t_N	70 to 140	μs
Pulse Duration, After zero crossing ($C_{(EXT)}$ = 0, R = ∞):			
Positive dv/dt	t_{P1}	50	μs
Negative dv/dt	t_{P1}	60	μs
Following conditions at 120 Vrms, 400 Hz:			
DC Supply Voltage (R_S = 10 kΩ, I_L = 0):			
Inhibit Mode	V_S	6.8	V
Pulse Mode	V_S	6.7	V
Total Gate Pulse Duration ($C_{(EXT)}$ = 0):			
Positive dv/dt	t_P	12	μs
Negative dv/dt	t_N	11	μs

CA3060 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER ARRAY

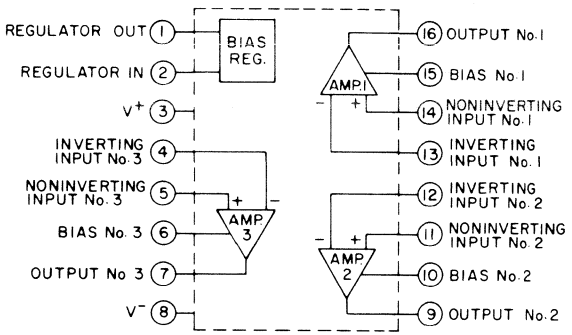
General-purpose array with three independent operational transconductance amplifiers and independent bias regulator used in low-power conventional operational amplifier applications. 16-lead JEDEC MO-001-AE package; Outline No. 12.

MAXIMUM RATINGS

DC Supply Voltage, Between V^+ and V^- terminals	14	V
Differential Input Voltage, Each amplifier	±5	V
DC Input Voltage	V^+ to V^-	
Input Signal Current, Each amplifier	±1	mA

Amplifier Bias Current, Each amplifier	2	mA
Bias Regulator Input Current	−5	mA
Output Short-Circuit Duration*	No limitation	
Device Dissipation (T_A up to 125°C)	200	mW
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 150	°C
Lead-Soldering Temperature (10 s max)	300	°C

* Short circuit may be applied to ground or to either supply.



CA3060

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = 6V, V^- = −6V, I_{ABC} = 1μA)

Static Characteristics			
Input Offset Voltage	V_{IO}	1 typ; 5 max	mV
Input Offset Current	I_{IO}	3 typ; 10 max	nA
Input Bias Current	I_I	33 typ; 65 max	nA
Peak Output Current	I_{OM}	1.3 min; 2.3 typ	μA
Peak Output Voltage, Positive	$V_{OM}+$	4.8 min; 5 typ	V
Peak Output Voltage, Negative	$V_{OM}-$	5.8 min; 5.96 typ	V
Amplifier Supply Current, Each amplifier	I_A	8.5 typ; 14 max	μA
Power Consumption, Each amplifier	P	0.10 typ; 0.17 max	mW
Input Offset-Voltage Sensitivity, Positive■	$\Delta V_{IO}/\Delta V+$	1.5 typ; 50 max	μV/V
Input Offset-Voltage Sensitivity, Negative■	$\Delta V_{IO}/\Delta V-$	20 typ; 80 max	μV/V
Amplifier Bias Voltage‡	V_{ABC}	0.54	V
Dynamic Characteristics (at 1 kHz)			
Forward Transconductance, Large Signal	g_2	0.15 min; 0.38 typ	mmho
Common-Mode Rejection Ratio	CMRR	80 min; 110 typ	dB
		4.4 to −5.1 min	V
Common-Mode Input Voltage Range	V_{CMR}	4.7 to −5.3 typ	V
Slew Rate	SR	0.1	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	160	kHz
Input Impedance Components, Resistance	R_I	800 min; 1600 typ	kΩ
Input Impedance Components, Capacitance at 1 MHz	C_I	2.7	pF
Output Impedance Components, Resistance	R_O	200	MΩ
Output Impedance Components, Capacitance at 1 MHz	C_O	4.5	pF
Bias Regulator Characteristics (I_2 = 1 mA)			
Bias Regulator Voltage●	V_{REG}	6.4 to 7.2	V
Zener Impedance	Z_{ZENER}	125 typ; 200 max	Ω

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, $V^+ = 6V$, $V^- = -6V$, $I_{ABC} = 10\mu A$)

Static Characteristics			
Input Offset Voltage	V_{IO}	1 typ; 5 max	mV
Input Offset Current	I_{IO}	30 typ; 100 max	nA
Input Bias Current	I_I	300 typ; 550 max	nA
Peak Output Current	I_{OM}	17 min; 26 typ	μA
Peak Output Voltage, Positive	$V_{OM}+$	4.5 min; 4.8 typ	V
Peak Output Voltage, Negative	$V_{OM}-$	5.8 min; 5.95 typ	V
Amplifier Supply Current, Each amplifier	I_A	85 typ; 120 max	μA
Power Consumption, Each amplifier	P	1 typ; 1.45 max	mW
Input Offset-Voltage Sensitivity, Positive■	$\Delta V_{IO}/\Delta V+$	2 typ; 50 max	μV/V
Input Offset-Voltage Sensitivity, Negative■	$\Delta V_{IO}/\Delta V-$	20 typ; 80 max	μV/V
Amplifier Bias Voltage‡	V_{ABC}	0.6	V
Dynamic Characteristics (At 1 kHz)			
Forward Transconductance, Large Signal	g_2	2 min; 4.5 typ	mmhos
Common-Mode Rejection Ratio	CMRR	80 min; 110 typ	dB
Common-Mode Input Voltage Range	V_{CMR}	4.3 to −5 min; 4.6 to −5.2 typ	V
Slew Rate	SR	1	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	270	kHz
Input Impedance Components, Resistance	R_I	90 min; 170 typ	kΩ
Input Impedance Components, Capacitance at 1 MHz	C_I	2.7	pF
Output Impedance Components, Resistance	R_O	20	MΩ
Output Imepedance Components, Capacitance at 1 MHz	C_O	4.5	pF
Bias Regulator Characteristics ($I_2 = 1$ mA)			
Bias Regulator Voltage●	V_{REG}	6.4 to 7.2	V
Zener Impedance	Z_{ZENER}	125 typ; 200 max	Ω

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, $V^+ = 6V$, $V^- = -6V$, $I_{ABC} = 100\mu A$)

Static Characteristics			
Input Offset Voltage	V_{IO}	1 typ; 5 max	mV
Input Offset Current	I_{IO}	250 typ; 1000 max	nA
Input Bias Current	I_I	2500 typ; 5000 max	nA
Peak Output Current	I_{OM}	150 min; 240 typ	μA
Peak Output Voltage, Positive	$V_{OM}+$	4.5 min; 4.7 typ	V
Peak Output Voltage, Negative	$V_{OM}-$	5.7 min; 5.9 typ	V
Amplifier Supply Current, Each amplifier	I_A	850 typ; 1200 max	μA
Power Consumption, Each amplifier	P	10 typ; 14.5	mW
Input Offset-Voltage Sensitivity, Positive	$\Delta V_{IO}/\Delta V+$	2 typ; 50 max	μV/V
Input Offset-Voltage Sensitivity, Negative	$\Delta V_{IO}/\Delta V-$	30 typ; 120 max	μV/V
Amplifier Bias Voltage‡	V_{ABC}	0.66	V
Dynamic Characteristics (At 1 kHz)			
Forward Transconductance, Large Signal	g_2	15 min; 35 typ	mmhos
Common-Mode Rejection Ratio	CMRR	70 min; 90 typ	dB
Common-Mode Input Voltage Range	V_{CMR}	4.3 to −5 min 4.6 to −5.2 typ	V

Slew Rate	SR	8	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	330	kHz
Input Impedance Components, Resistance	R_I	10 min; 20 typ	kΩ
Input Impedance Components, Capacitance at 1 MHz	C_I	2.7	pF
Output Impedance Components, Resistance	R_O	2	MΩ
Output Impedance Components, Capacitance at 1 MHz	C_O	4.5	pF
Bias Regulator Characteristics (I_2 = 1 mA)			
Bias Regulator Voltage•	V_{REG}	6.4 to 7.2	V
Zener Impedance	Z_{ZENER}	125 typ; 200 max	Ω

■ Conditions for Input Offset Voltage and Supply Sensitivity:
(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test—
V^+ is reduced to 5 volts for V^+ sensitivity
V^- is reduced to −5 volts for V^- sensitivity

(b) V^+ sensitivity in $\mu V/V = \frac{\text{V offset} - \text{V offset for 5 V and } -6 \text{ V supplies}}{1 \text{ Volt}}$

V^- sensitivity in $\mu V/V = \frac{\text{V offset} - \text{V offset for } -5 \text{ V and 6 V supplies}}{1 \text{ Volt}}$

‡ Temperature-Coefficient; −2.2 mV/°C (At V_{ABC} = 0.54 V, I_{ABC} = 1 μA); −2.1 mV/°C (At V_{ABC} = 0.6 V, I_{ABC} = 10 μA); −1.9 mV/°C (At V_{ABC} = 0.66 V, I_{ABC} = 100 μA
• Temperature-Coefficient = 3 mV/°C

PHOTODETECTOR/ POWER AMPLIFIER

CA3062

Special-purpose amplifier used in photoelectric control applications utilizing IR emitters and visible-light sources. Modified 12-lead JEDEC MO-004-AF package; Outline No. 3.

MAXIMUM RATINGS

Transistor Dissipation:		
T_A = 25°C	700	mW
T_A above 25°C	Derate linearly 5.6	mW/°C
$T_C \leq$ 55°C	1.5	W
T_C above 55°C	Derate linearly 16	mW/°C
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 150	°C
Lead-Soldering Temperature (10 s max)	300	°C

CHARACTERISTICS

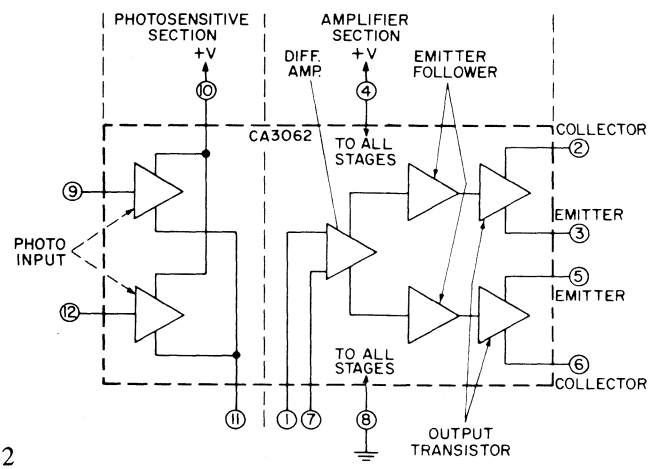
Static Characteristics			
Photo Darlington Section:			
Collector-to-Emitter Breakdown Voltage (E = 0 lumens/ft², I_C = 1 mA)	$V_{(BR)CBO}$	10 min	V
Emitter-to-Base Breakdown Voltage (I_E = 0.1 mA, E = 0)	$V_{(BR)EBO}$	10 min	V
Dark Current (V_{CE} = 7.5 V, E = 0)	I_{DARK}	0.1 typ; 30 max	μA
Photo Current (V_{CE} = 7.5 V, E = 8 lumens/ft²)	I_P	60	μA

Wavelength of Maximum Sensitivity	λmax	725	nm*
Relative Angular Sensitivity		—	
Area of Each Photo Transistor		1.3×10^{-4}	cm^2
Amplifier Section Output Transistor:			
Collector-to-Emitter Breakdown Voltage (I_C = 1 mA)	$V_{(BR)CEO\ 6}$ $V_{(BR)CEO\ 7}$	15 min	V
Emitter-to-Base Breakdown Voltage (I_E = 1 mA)	$V_{(BR)EBO\ 6}$ $V_{(BR)EBO\ 7}$	5 min	V
DC Supply Current (V_4 = 7.5 V)	I_{SUPPLY}	5.5 typ; 10 max	mA
Sensitivity:			
Illumination for Normal "OFF" Output (Set light input for I_6 = 70 mA)	E_{ON}	8 typ; 70 max	lumens/ft²■‡
Illumination for Normal "ON" Output (Set light input for I_2 = 5 mA)	E_{OFF}	10	lumens/ft²■‡
Dynamic Characteristics			
Overall Response Time (E = 700 μW/cm² at λ = 930 nm):			
Turn-On Time	t_{on}	38	μs
Rise Time	t_r	125	μs
Turn-Off Time	t_{off}	43	μs
Fall Time	t_f	20	μs

* One (1) nanometer = 10 Angstrom units.

■ Tungsten filament light source at a color temperature of 2854 K.

‡ A radiant flux density of 7.5 μW/cm² at 725 nm produces the same photocurrent as 1 lumen/ft² from a tungsten filament lamp at a color temperature of 2854 K.



CA3062

AUTOMATIC FINE-TUNING CIRCUIT CA3064

Special-purpose multiple function integrated circuit used primarily for automatic frequency control applications. 10-formed-lead "TO-5" package; Outline No. 5.

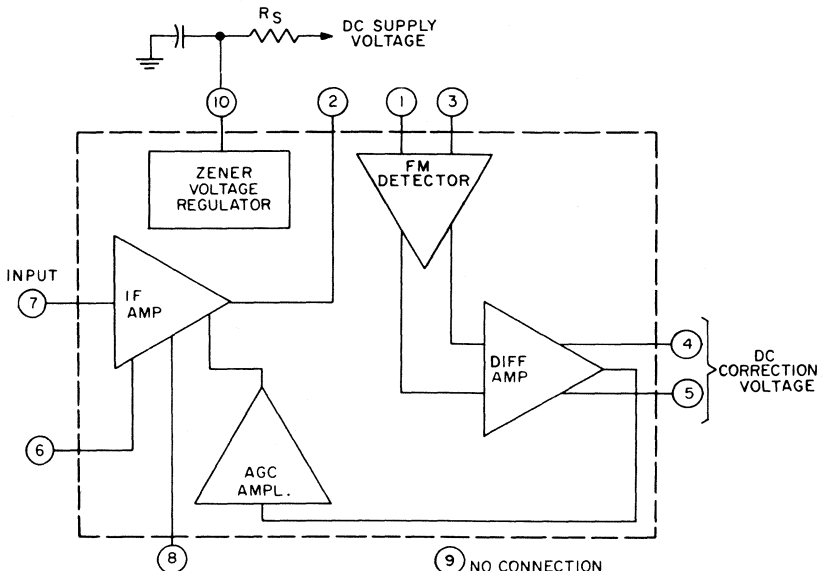
MAXIMUM RATINGS

Device Dissipation:		
T_A = 25°C	700	mW
T_A above 25°C	Derate linearly 5.6	mW/°C
Temperature Range:		
Operating	−40 to 8	°C
Storage	−65 to 150	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Static Characteristics			
Device Dissipation:			
V^+ = 30 V, R_S = 1.5 kΩ, T_A = −25°C	P_T	135 typ; 150 max	mW
V^+ = 30 V, R_S = 1.5 kΩ, T_A = 25°C	P_T	130 to 150	mW
V^+ = 30 V, R_S = 1.5 kΩ, T_A = 85°C	P_T	145 typ; 150 max	mW
Current Drain at 10.5 Volts (V_{10} = 10.5 V)	I_T	4 to 9.5	mA
Zener Regulating Voltage, DC Supply Voltage at Terminal 10 (V^+ = 30 V, R_S = 1.5 kΩ)	V_{10}	10.9 to 12.8	V
Quiescent Operating Current into Terminal 2 (V^+ = 30 V, R_S = 1.5 kΩ)	I_2	1 to 4	mA
Quiescent Operating Voltage at Terminal 4 (V^+ = 30 V, R_S = 1.5 kΩ)	V_4	5 to 8	V
Quiescent Operating Voltage at Terminal 5 (V^+ = 30 V, R_S = 1.5 kΩ)	V_5	5 to 8	V
Output Offset Voltage between Terminals 4 and 5 (V^+ = 30 V, R_S = 1.5 kΩ)	V_{4-5}	−1 to 1	V
Dynamic Characteristics			
Input Voltage Sensitivity (V^+ = 30 V, V_i = 18 mV)	$V_i$sensitivity	Correction Voltage Output for Terminals 4 and 5 as shown below	
Input Admittance (V^+ = 30 V, R_S = 1.5 kΩ, f = 45.75 MHz)	y_{11}	0.41 + j 1	mmhos
Reverse Transfer Admittance (V^+ = 30 V, R_S = 1.5 kΩ, f = 45.75 MHz)	y_{12}	0 + j 3.4	μmhos
Forward Transfer Admittance (V^+ = 30 V, R_S = 1.5 kΩ, f = 45.75 MHz)	y_{21}	24.5 − j 29	mmhos
Output Admittance (V^+ = 30 V, R_S = 1.5 kΩ, f = 45.75 MHz)	y_{22}	0.04 + j 0.9	mmho
Output vs Frequency Deviation—AFC			
Corrector-Control Voltage at Terminal 4 (V^+ = 30 V, V_{in} = 18 mV RMS, f_o = MHz as indicated):			
45.750 − 0.030	$V_{corr}(4)$	85% min of V_{10}	V
45.750 + 0.030	$V_{corr}(4)$	25% max of V_{10}	V
45.750 − 0.900	$V_{corr}(4)$	80% min of V_{10}	V
45.750 + 0.900	$V_{corr}(4)$	35% max of V_{10}	V
45.750 − 1.500	$V_{corr}(4)$	80% max of V_{10}	V
45.750 + 1.500	$V_{corr}(4)$	35% min of V_{10}	V

Correction-Control Voltage at Terminal 5 (V^+ = 30 V, V_{in} = 18 mV RMS, f_o = MHz as indicated):			
45.750 − 0.030	$V_{corr}(5)$	25% max of V_{10}	V
45.750 + 0.030	$V_{corr}(5)$	85% min of V_{10}	V
45.750 − 0.900	$V_{corr}(5)$	35% max of V_{10}	V
45.750 + 0.900	$V_{corr}(5)$	80% min of V_{10}	V
45.750 − 1.500	$V_{corr}(5)$	35% min of V_{10}	V
45.750 + 1.500	$V_{corr}(5)$	80% max of V_{10}	V



CA3064

CA3065 FM IF AMPLIFIER DISCRIMINATOR/AF AMPLIFIER

Special-purpose multiple function integrated circuit used in television sound-system applications. 14-lead JEDEC MO-001-AB package; Outline No. 9.

MAXIMUM RATINGS

Input Signal Voltage, Between Terminals 1 and 2	±3	V
Power Supply Current, Terminal 5	50	mA
Power Dissipation:		
T_A up to 25°C	850	mW
T_A above 25°C	Derate linearly 6.67	mW/°C
Temperature Range:		
Operating	−40 to 85	°C
Storage	−65 to 150	°C

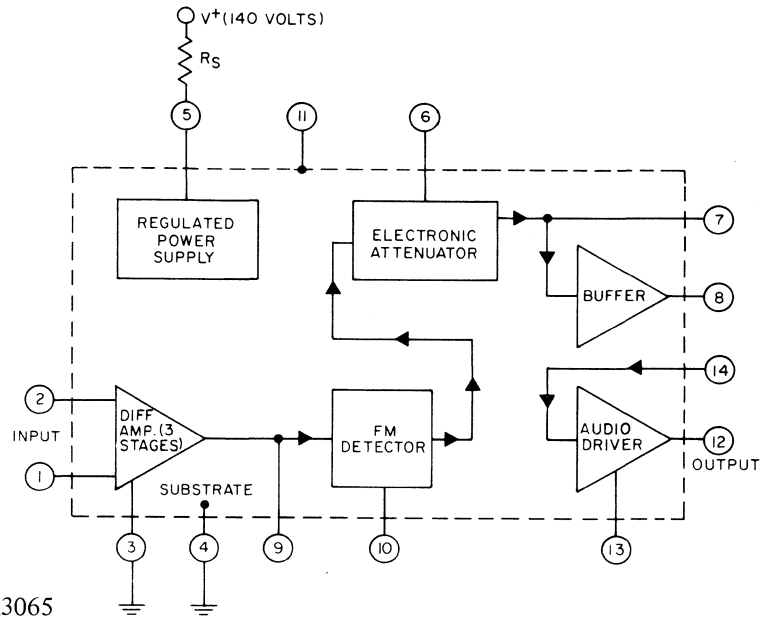
TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V^+ = 140V applied to terminal 5 through R_S = 3.9 kΩ, and DC Volume Control (R_X) = 0)

Static Characteristics

Zener Regulating Voltage, Terminal No. 5	V_5	10.3 to 12.2	V

Current into Terminal 5 (Connect terminal 5 to +9V)	I_5	10 to 24	mA
Total Device Dissipation	P_T	343 to 400	mW
Terminal Voltages:			
1	V_1	2	V
6	V_6	4.8	V
7	V_7	6.1	V
9	V_9	3.7	V
12	V_{12}	4 to 5.8	V
Dynamic Characteristics			
IF Amplifier			
Input Limiting Voltage, −3-dB (f_o = 4.5 MHz, f_m = 400 Hz, deviation = ±25 kHz)	$V_{i(lim)}$	200 typ; 400 max	μV
AM Rejection (Amplitude modulation = 30%, f = 4.5 MHz)	AMR	40 min; 50 typ	dB
Transconductance, Magnitude (IF input terminals: 2, 1, IF output terminals: 9, 3; f = 4.5 MHz)	$\|G_m\|$ (IF)	500	mmhos
Transconductance, Phase Angle (IF input terminals): 2, 1; IF output terminals: 9, 3; f = 4.5 MHz)	θ(IF)	46	degrees
Feedback Capacitance (Terminals 2 and 9, f = 1 MHz)	C_{fb}	<0.02	pF
Parallel Input Resistance (Measured between terminals 1 and 2, f = 4.5 MHz)	R_i(IF)	17	kΩ
Parallel Input Capacitance (Measured between terminals 1 and 2, f = 4.5 MHz)	C_i(IF)	4	pF
Parallel Output Resistance (Measured between terminal 9 and ground, f = 4.5 MHz)	R_o(IF)	3.25	kΩ
Parallel Output Capacitance (Measured between terminal 9 and ground, f = 4.5 MHz)	C_o(IF)	75	pF
Detector			
Recovered AF Voltage (V_i = 100 mV, Δf = ±25 kHz, f_m = 400 Hz, f = 4.5 MHz)	V_o(af)	0.5 min; 0.75 typ	V(rms)
Total Harmonic Distortion (V_i = 100 mV, Δf = ±25 kHz, f_m = 400 kHz, f = 4.5 MHz)	THD	0.9 typ; 2 max	%
Output Resistance, Terminal 7	R_o	7.5	kΩ
Output Resistance, Terminal 8	R_o	300	Ω
Attenuator			
Maximum Attenuation (R_X = ∞)		60 min; 80 typ	dB
Maximum Play-through Voltage* (R_X = ∞)		0.075 typ; 1 max	mV
Audio Amplifier			
Voltage Gain (V_i = 0.1 V(rms), f = 400 Hz)	A(af)	17.5 min; 20 typ	dB
Total Harmonic Distortion V_O = 2 V(rms), f = 400 Hz)	THD	1.5	%
Undistorted Output Voltage (THD = 5%, f = 400 Hz)		2 min; 2.5 typ	V(rms)
Input Resistance (f = 400 Hz)	R_i(af)	70	kΩ
Output Resistance (f = 400 Hz)	R_o(af)	270	Ω

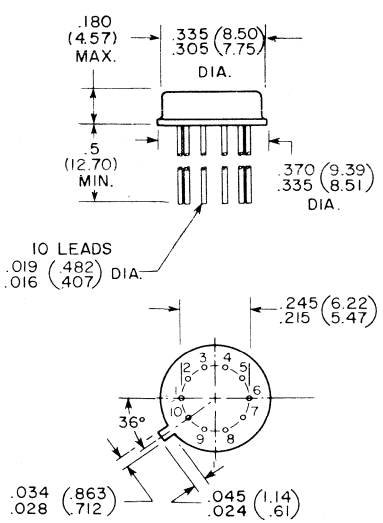
* Playthrough voltage is the unwanted signal, measured at terminal 8, when the volume control is set for minimum output.


V+(140 VOLTS)
RS
5
11
6
REGULATED POWER SUPPLY
ELECTRONIC ATTENUATOR
7
BUFFER
8
14
2
INPUT
1
DIFF AMP. (3 STAGES)
FM DETECTOR
AUDIO DRIVER
12
OUTPUT
SUBSTRATE
3
4
9
10
13

CA3065

Outlines

Dimensions shown in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.



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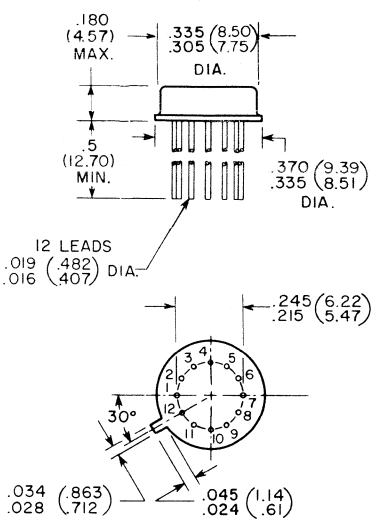

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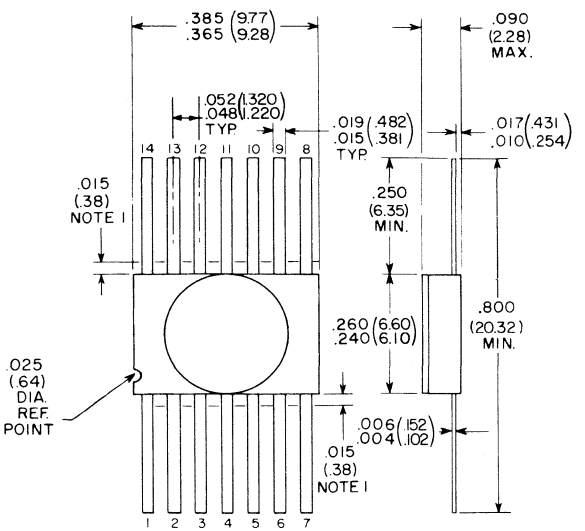

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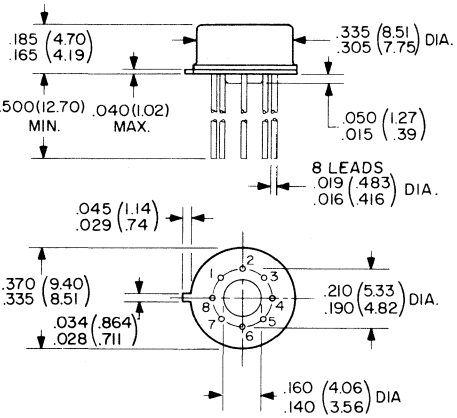
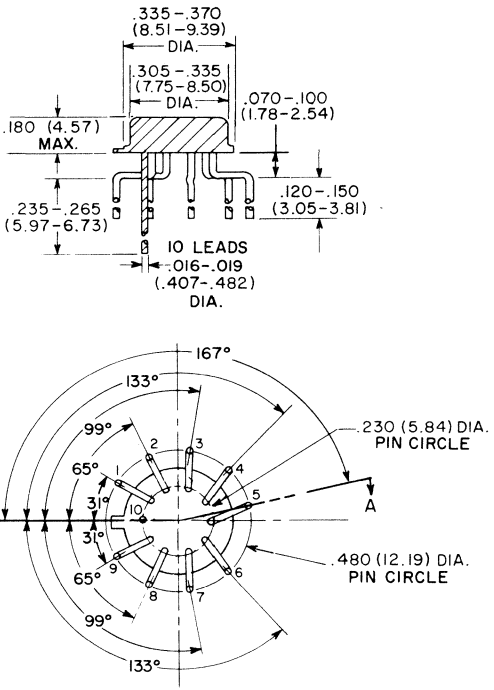
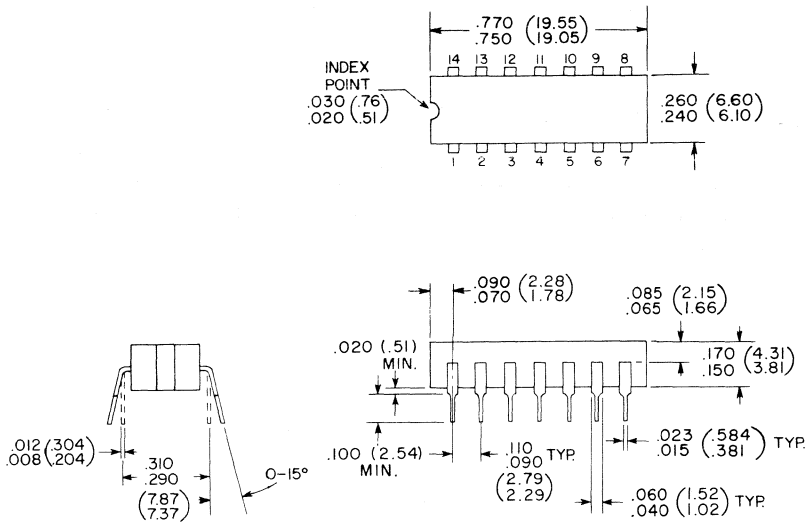

.185 (4.70)
.165 (4.19)
.335 (8.51) DIA.
.305 (7.75) DIA.
.500(12.70) MIN.
.040(1.02) MAX.
.050 (1.27)
.015 (.39)
8 LEADS
.019 (.483)
.016 (.416) DIA.
.045 (1.14)
.029 (.74)
.370 (9.40)
.335 (8.51)
.034 (.864)
.028 (.711)
.210 (5.33)
.190 (4.82) DIA.
.160 (4.06)
.140 (3.56) DIA

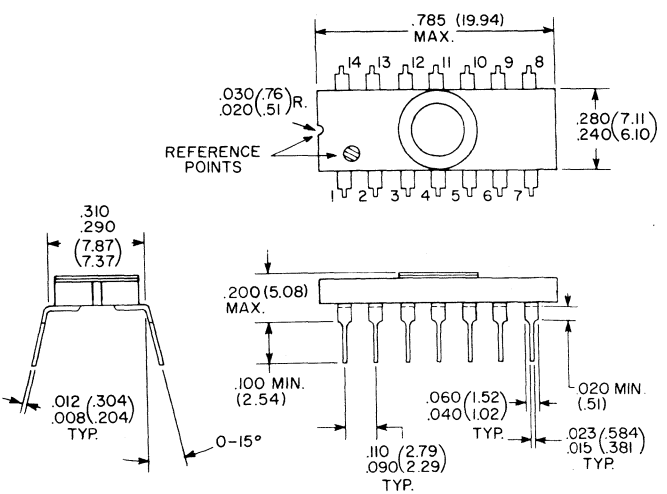
4


.335-.370
(8.51-9.39)
DIA.
.305-.335
(7.75-8.50)
DIA.
.070-.100
(1.78-2.54)
.180 (4.57)
MAX.
.120-.150
(3.05-3.81)
.235-.265
(5.97-6.73)
10 LEADS
.016-.019
(.407-.482)
DIA.
167°
133°
99°
65°
31°
.230 (5.84) DIA.
PIN CIRCLE
.480 (12.19) DIA.
PIN CIRCLE
A
A

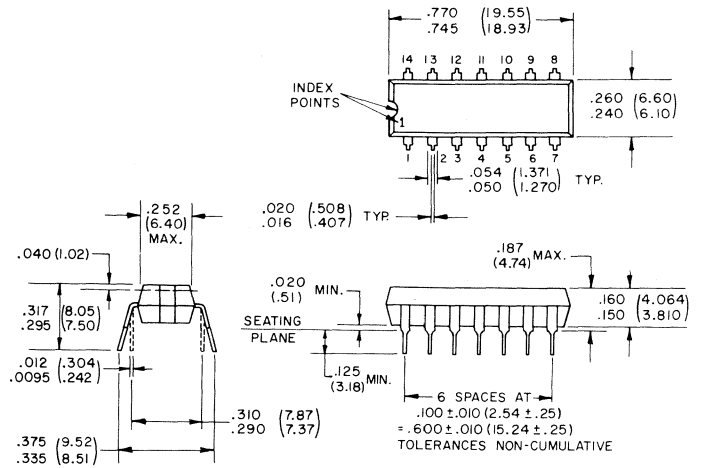
5


.770 (19.55)
.750 (19.05)
14 13 12 11 10 9 8
INDEX
POINT
.030 (.76)
.020 (.51)
.260 (6.60)
.240 (6.10)
1 2 3 4 5 6 7
.090 (2.28)
.070 (1.78)
.085 (2.15)
.065 (1.66)
.020 (.51)
MIN.
.170 (4.31)
.150 (3.81)
.012 (.304)
.008 (.204)
.310
.290
(7.87)
(7.37)
0-15°
.100 (2.54)
MIN.
.110
.090 TYP.
(2.79)
(2.29)
.023 (.584)
.015 (.381) TYP.
.060 (1.52)
.040 (1.02) TYP.

6


.785 (19.94)
MAX.
14 13 12 11 10 9 8
.030(.76)R.
.020(.51)
REFERENCE
POINTS
.280(7.11)
.240(6.10)
1 2 3 4 5 6 7
.310
.290
(7.87)
(7.37)
.200(5.08)
MAX.
.100 MIN.
(2.54)
.012 (.304)
.008(.204)
TYP.
0-15°
.060(1.52)
.040(1.02)
TYP.
.020 MIN.
(.51)
.023(.584)
.015 (.381)
TYP.
.110 (2.79)
.090(2.29)
TYP.

7


.770 (19.55)
.745 (18.93)
14 13 12 11 10 9 8
INDEX POINTS
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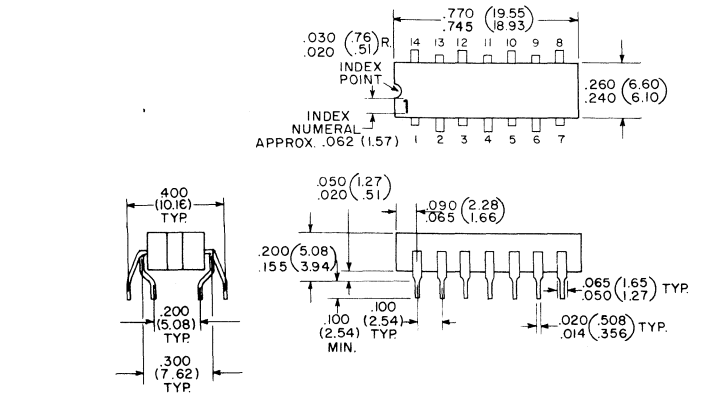
.240 (6.10)
1 2 3 4 5 6 7
.054 (1.371)
.050 (1.270) TYP.
.020 (.508)
.016 (.407) TYP.
.252 (6.40) MAX.
.040 (1.02)
.317 (8.05)
.295 (7.50)
.012 (.304)
.0095 (.242)
.310 (7.87)
.290 (7.37)
.375 (9.52)
.335 (8.51)
.187 (4.74) MAX.
.020 (.51) MIN.
SEATING PLANE
.160 (4.064)
.150 (3.810)
.125 (3.18) MIN.
6 SPACES AT .100 ±.010 (2.54 ±.25) = .600 ±.010 (15.24 ±.25)
TOLERANCES NON-CUMULATIVE

8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.745 (18.93)
.030 (.76) R.
.020 (.51)
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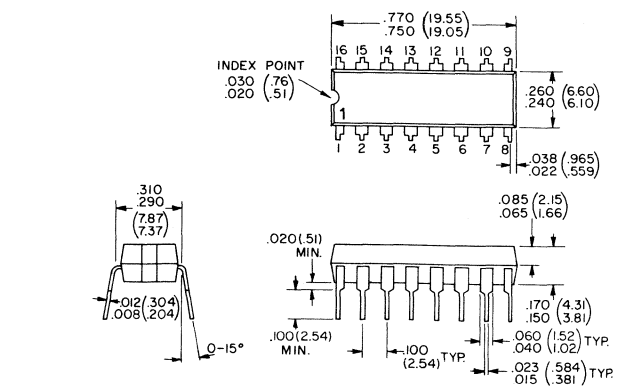
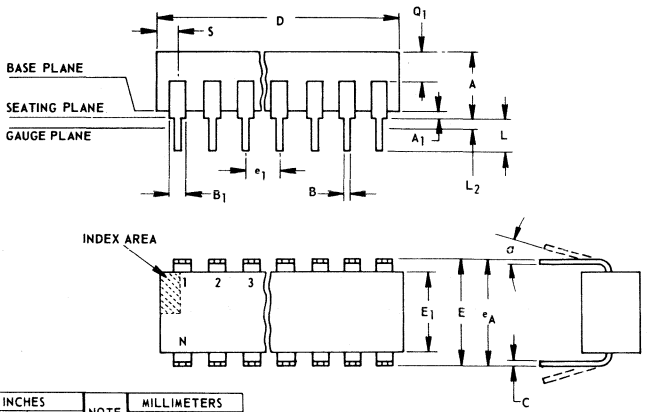
INDEX POINT
1
.260 (6.60)
.240 (6.10)
INDEX NUMERAL
APPROX. .062 (1.57)
1 2 3 4 5 6 7
.400 (10.16) TYP.
.200 (5.08) TYP.
.300 (7.62) TYP.
.050 (1.27)
.020 (.51)
.090 (2.28)
.065 (1.66)
.200 (5.08)
.155 (3.94)
.065 (1.65)
.050 (1.27) TYP.
.100 (2.54) TYP.
.100 (2.54) MIN.
.020 (.508)
.014 (.356) TYP.

9


.770 (19.55)
.750 (19.05)
INDEX POINT
.030 (.76)
.020 (.51)
16 15 14 13 12 11 10 9
1
.260 (6.60)
.240 (6.10)
1 2 3 4 5 6 7 8
.038 (.965)
.022 (.559)
.310
.290
(7.87)
(7.37)
.012 (.304)
.008 (.204)
0-15°
.085 (2.15)
.065 (1.66)
.020 (.51) MIN.
.170 (4.31)
.150 (3.81)
.100 (2.54) MIN.
.100 (2.54) TYP.
.060 (1.52)
.040 (1.02) TYP.
.023 (.584)
.015 (.381) TYP.

10



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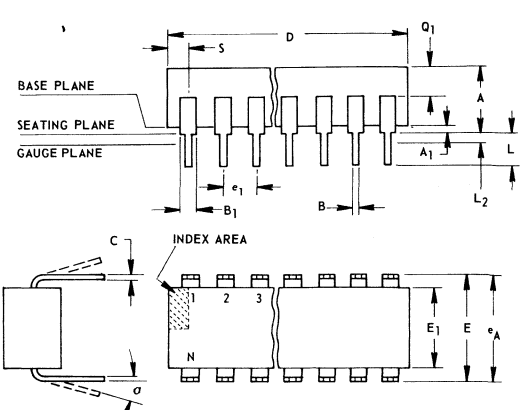
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN	MAX		MIN	MAX
A	.155	.200		3.94	5.08
A_1	.020	.050		.51	1.27
B	.014	.020		.356	.508
B_1	.050	.065		1.27	1.65
C	.008	.012		.204	.304
D	.745	.770		18.93	19.55
E	.300	.325		7.62	8.25
E_1	.240	.260		6.10	6.60
e_1	.100 TP		2	2.54 TP	
e_A	.300 TP		2, 3	7.62 TP	
L	.125	.150		3.18	3.81
L_2	.000	.030		.000	.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	.040	.075		1.02	1.90
S	.065	.090		1.66	2.28

NOTES:
1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads within .005" (.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN	MAX		MIN	MAX
A	.120	.160		3.05	4.06
A_1	.020	.065		.51	1.65
B	.014	.020		.356	.508
B_1	.035	.065		.89	1.65
C	.008	.012		.204	.304
D	.745	.785		18.93	19.93
E	.300	.325		7.62	8.25
E_1	.240	.260		6.10	6.60
e_1	.100 TP		2	2.54 TP	
e_A	.300 TP		2, 3	7.62 TP	
L	.125	.150		3.18	3.81
L_2	.000	.030		.000	.76
α	0°	15°	4	0°	15°
N	16		5	16	
N_1	0		6	0	
Q_1	.050	.085		1.27	2.15
S	.015	.060		.39	1.52

NOTES:
1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads within .005" (.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.



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Index

ther RCA Technical Manuals

● **RCA POWER CIRCUITS**—SP-51—(8" x 5¼")—448 pages. Contains design information for a broad range of power circuits using RCA silicon transistors, rectifiers, and thyristors (SCR's, triacs, and diacs). Gives design criteria and procedures for applications involving rectification, supply filtering, power conversion and regulation, ac line-voltage controls, rf power amplifiers, and control and low frequency amplifiers. Shows design examples and practical circuits. Price $2.00.*†

● **RCA TRANSISTOR, THYSISTOR & DIODE MANUAL**—SC-14 (8" x 5¼")—656 pages. Contains up-to-date definitive data on over 700 semiconductor devices including tunnel diodes, silicon controlled rectifiers, varactor diodes, conventional rectifiers, and many classes of transistors. Features easy-to-understand text chapters, as well as tabular data on RCA discontinued transistors. Contains 38 practical circuits, complete with parts lists, highlighting semiconductor- device applications. Price $2.50.*†

● **RCA HIGH-SPEED, HIGH-VOLTAGE, HIGH-CURRENT POWER TRANSISTORS**—PM-80 (8" x 5¼")—96 pages. Provides a basic understanding of the theory and application of the RCA line of medium-frequency power transistors. Covers physical theory, structures, geometries, packaging, critical application-limiting factors, and the operation and requirements of power transistors in amplifier, switching, and control applications. Typical circuits illustrate the use of transistors in series voltage regulators, linear amplifiers, switching regulators, and inverters and converters, and the application of complementary transistor pairs. Selection charts are included to facilitate choice of the optimum type of power transistor for a variety of military, industrial, and commercial applications. Price $2.00.*†

● **RCA SOLID-STATE HOBBY CIRCUITS MANUAL**—HM-90 (8⅜" x 5⅜")—224 pages. Contains complete construction information on 35 circuits of general interest to all experimenters. Circuits use diodes, transistors, SCR's, triacs, MOS transistors, integrated circuits, and light and heat detectors. Circuit operation is described in detail; construction layouts, photographs, schematic diagrams, and parts lists are given; and full-size drilling templates are included for most circuits to simplify construction. Price $1.75.*†

● **RCA SILICON CONTROLLED RECTIFIER EXPERIMENTER'S MANUAL**—KM-71 (8⅜" x 5⅜")—136 pages. Contains 24 practical and interesting control circuits that can be built with a complement of active devices available in kit form. Includes photographs, schematic diagrams, and descriptive writeups. Also includes brief descriptions of solid-state components used (rectifiers, transistors, SCR's) and short section on troubleshooting. Price 95 cents.*†

● **RCA RECEIVING TUBE MANUAL**—RC-27 (8" x 5¼")—672 pages. Contains technical data on more than 1400 receiving tubes for home-entertainment use. Includes six easy-to-read text chapters that provide basic information on electron-tube operation, ratings and characteristics, and applications. Also features a detailed application guide for receiving tubes; quick-reference charts for replacement and discontinued RCA receiving tubes, black-and-white and color picture tubes, and voltage-reference tubes; and a Circuits section that includes schematic diagrams, descriptive writeups, and complete parts lists for 36 practical electron-tube circuits for a wide variety of applications. Price $2.00.*†

● **RCA TRANSMITTING TUBES**—TT-5 (8⅜" x 5⅜")—320 pages. Gives data on over 180 power tubes having plate-input ratings up to 4 kW and on associated rectifier tubes. Provides basic information on generic types, parts and materials, installation and application, and interpretation of data. Contains circuit diagrams for transmitting and industrial applications. Features lie-flat binding. Price $1.00*†

● **RCA PHOTOTUBE AND PHOTOCELL MANUAL**—PT-60 (8⅜" x 5⅜")—192 pages. Well-illustrated informative manual covering fundamentals and operating considerations for vacuum and gas phototubes, multiplier phototubes, and photocells. Also describes basic applications for these devices. Features easy-to-use selection chart for multiplier phototubes. Data and performance curves given for over 90 photo-sensitive devices. Price $1.50.*†

* Prices shown apply in U.S.A. and are subject to change without notice.
† Optional price.